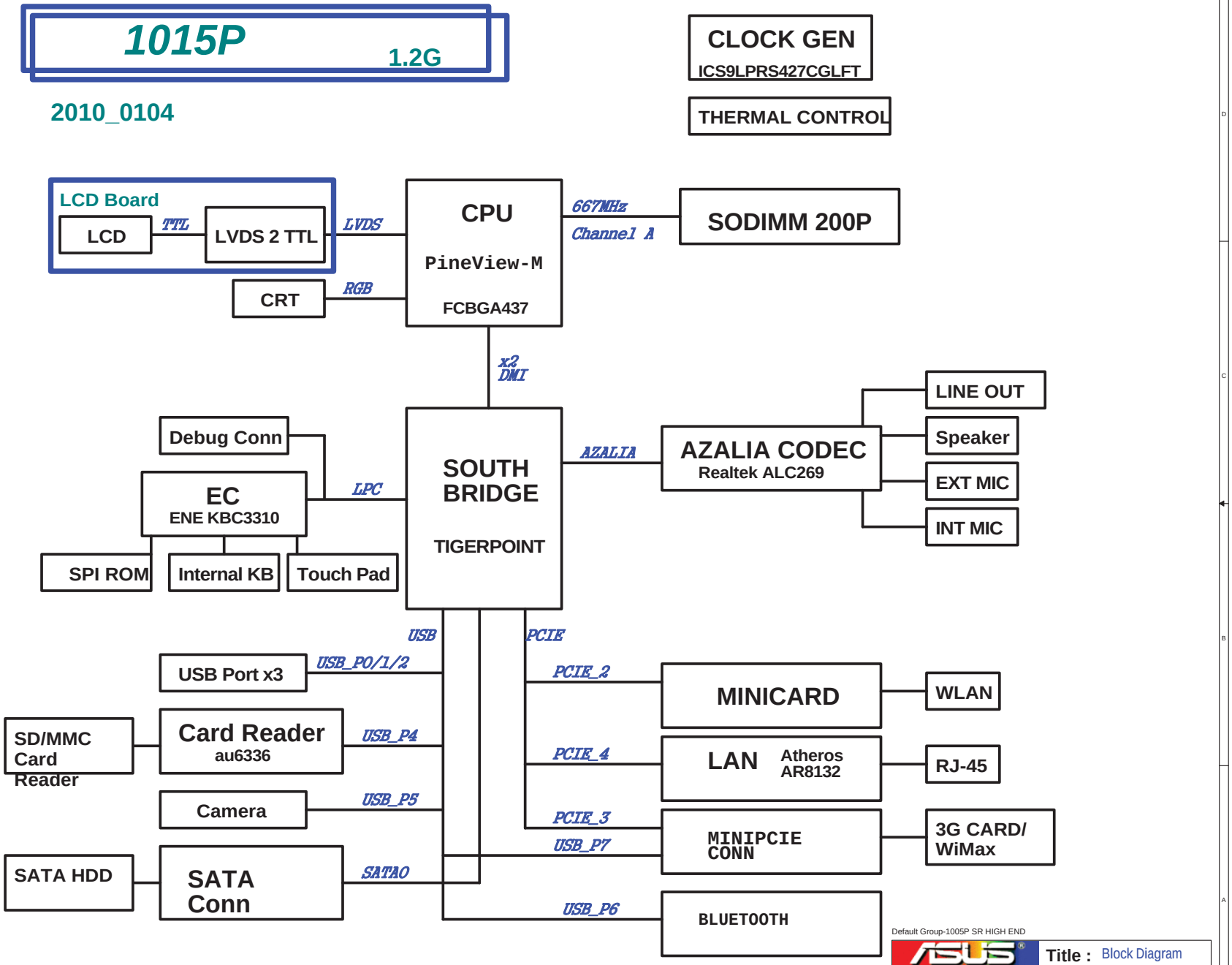
01_Block Diagram
02_Power Sequence
03_Clock Gen_ICS9LPRS427C
04.PineView-M_1 (LVDS_DMI_CPU)
05.PineView-M_2 (DDR2_XDP_CRT)
06.PineView-M_3 (PWR&GND)
07.XDP
08.Tigerpoint_DMI_USB
09.Tigerpoint_SYS
10.Tigerpoint_PWR
11.DDR2 SODIMM
12.DDR2-Termination
13.Onboard VGA
14.LCD Conn_LID
15.WIFI&SMART33SW
16.LAN_AR8132
17.WLAN
18.USIN&3G_CON
19.Bluetooth
20.HDD_CON
21.
22.
23.USB Port1
24.EC_ENE KB3310
25.KB_TP
26.Fan_debug
27.SPI_ROM
28.DUA_CON
29.PWR Jack
30_Discharge
31.
32.Srew Hole&EMI
33.Power Flow
34.Power_Charger
35.Vcore
36.Power _+1.8V&VTTDDR&+1.8VS
37.Power_VCCP
38.Power_+0.89VS
39.Power_+1.5VS
40.Power Latch
41.Power System
42.power swich

1015P 1.2G

2010_0104



Default Group-1005P SR HIGH END

ASUSTek Computer INC.

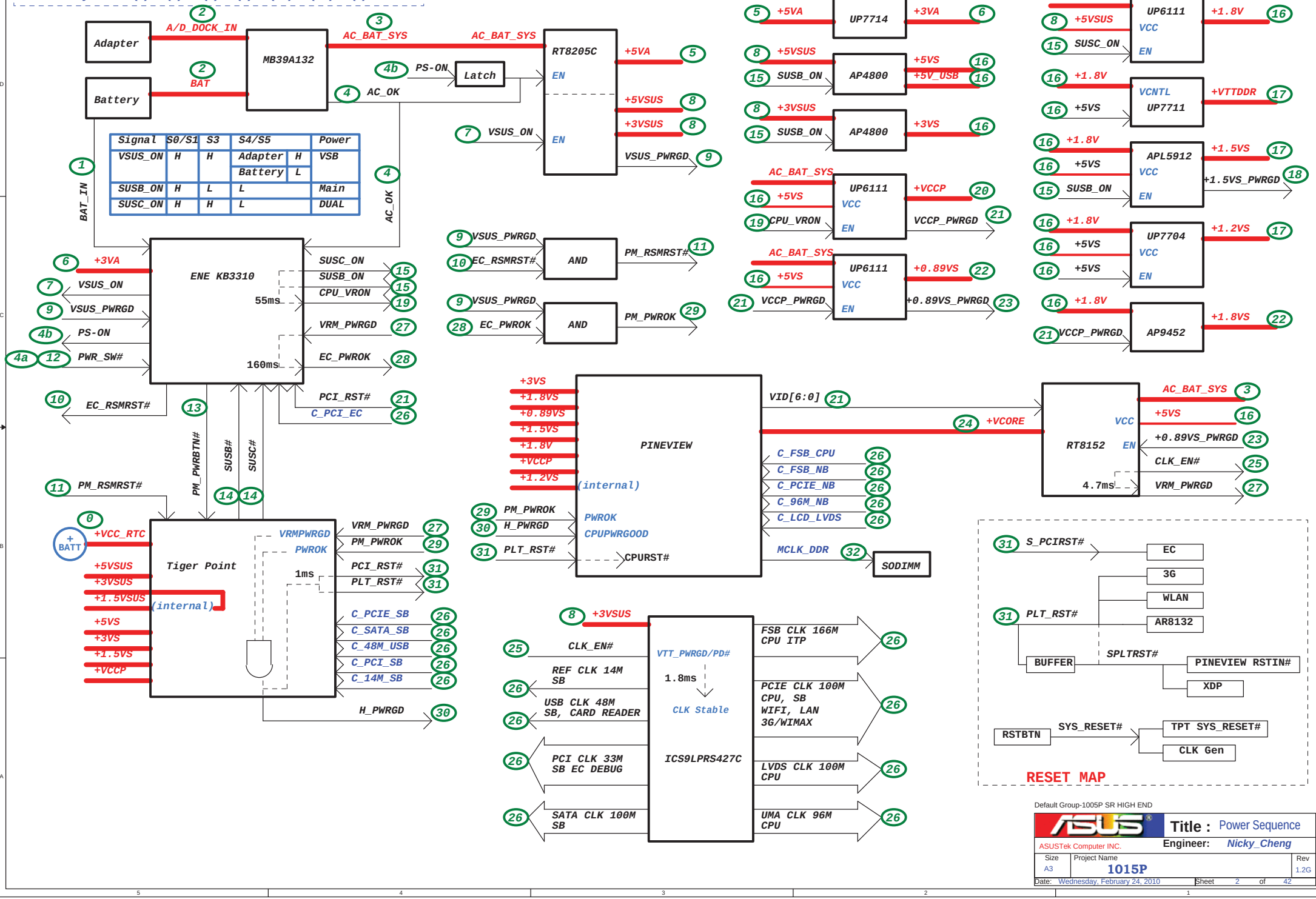
Title : Block Diagram

Engineer: Nicky_Cheng

Size	Project Name	Rev
Custom	1015P	1.2G

Date: Wednesday, February 24, 2010 Sheet 1 of 42

For Adapter Mode: (1) -> (2) -> (3) -> (4) -> (5) -> ...
For Battery Mode: (1) -> (2) - > (3) -> (4) -> (4a) -> (4b) -> (5) -> ...



Default Group-1005P SR HIGH END

ASUSTek Computer INC.	Title : Power Sequence		
	Engineer: Nicky_Cheng		
Size A3	Project Name 1015P		Rev 1.2G
Date: Wednesday, February 24, 2010	Sheet 2 of 42		

1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FS4	Function
H	FIXED PLL (Asynchronous)
L	PCI/PCIEX PLL(synchronize)

CR1 Do Not Stuff /X
CX1 14.31818Mhz
C_XIN
C_XOUT
CC12 15PF/50V
CC13 15PF/50V
GND

+3VSUS
CL1 120Ohm/100Mhz N/A
+3V_CLK
+3VS
CL2 Do Not Stuff /X
CC1 10UF/6.3V c0603
CC58 0.1UF/16V
CC2 CC3 CC4 CC5 CC6 CC7 CC8 CC9 0.1UF/16V
CC10 120Ohm/100Mhz N/A
CL4
+3V_CLK_VDDA
CC48 0.1UF/16V

CC58 for RF , close to pin 42

CU1
ICS9LPRS427CGLFT

1	VDD1	25MHz/FREERUN	56
2	GND1	PCI&PCIEX_STOP#	55
3	PEREQ1#	CPU_STOP#	54
4	PEREQ2#	REF0/FSLC	53
5	FS4/PCICLK0	DOC_PEREQ3#	52
6	GND2	GND4	51
7	VDDPCI	X1	50
8	ITP_EN/PCICLK_F0	X2	49
9	SEL12_48#/12_48MHz	VDDREF	48
10	Vtt_PwrGd/PD#	SDATA	47
11	VDD2	SCLK	46
12	FSLA/USB_48MHz	GND5	45
13	GND3	CPUT_LR0	44
14	DOTT_96MHzLR	CPUC_LR0	43
15	DOTC_96MHzLR	VDDCPU	42
16	FSLB	CPUT_LR1	41
17	PCIeT_LR0	CPUC_LR1	40
18	PCIeC_LR0	RESET#	39
19	PCIeT_LR1	GNDA	38
20	PCIeC_LR1	VDDA	37
21	VDDPCIEX1	CPUITPT_LR2/PCIeT_LR6	36
22	PCIeT_LR2	CPUITPC_LR2/PCIeC_LR6	35
23	PCIeC_LR2	VDDPCIEX3	34
24	PCIeT_LR3	PCIeT_LR5	33
25	PCIeC_LR3	PCIeC_LR5	32
26	SATACLKT_LR	PCIeT_LR4	31
27	SATACLKC_LR	PCIeC_LR4	30
28	VDDPCIEX2	GND6	29

+3V_CLK
+3V_CLK_VDDA
PEREQ1#
C_REQ#_WLAN
CR8 33Ohm/DEBUG_FS4
CR6 CR7 33Ohm
CR12 33Ohm
C_PCI_SB_R
C_48M_R
CLK_EN
CR3 33Ohm
C_FSLA
C_FSLB
PCIE2
PCIE2#
C_LAN_25M_R 47Ohm CR10 C_LAN_25M
/LAN_CLK
C_FSLC 33Ohm CR4
C_DOC_REQ Do Not Stuff CR23
C_XIN
C_XOUT
/LAN_REQ
S_SMBDATA
S_SMBCLK
C_RESET# CR21 /X Do Not Stuff
0Ohm CR19 /XDP
0Ohm CR20 /XDP

26	C_PCI_DEBUG
24	C_LPC_EC
8	C_PCI_SB
28	C_48M_CARD_READER
8	C_48M_USB
5	C_96M_NB
5	C_96M_NB#
5	C_LCD_LVDS
5	C_LCD_LVDS#
4	C_PCIE_NB
4	C_PCIE_NB#
18	C_PCIE_WIMAX
18	C_PCIE_WIMAX#
17	C_PCIE_WLAN
17	C_PCIE_WLAN#
9	C_SATA_SB
9	C_SATA_SB#

C_LAN_25M	16
STP_PCI#	9
STP_CPU#	9
C_14M_SB	9
L_REQ#_LAN	16
S_SMBDATA	9
S_SMBCLK	9
C_FSB_CPU	4
C_FSB_CPU#	4
C_FSB_NB	5
C_FSB_NB#	5
SYS_RESET#	7,9
H_ITP_CLK	7
H_ITP_CLK#	7
C_PCIE_LAN	16
C_PCIE_LAN#	16
C_PCIE_SB	8
C_PCIE_SB#	8

C_SATA_SB CC50 Do Not Stuff /X
C_SATA_SB# CC51 10PF/50V /X
PCIE2 CC52 Do Not Stuff /X
PCIE2# CC53 Do Not Stuff /X
C_LCD_LVDS# CC54 Do Not Stuff /X
C_LCD_LVDS CC55 Do Not Stuff /X
STP_PCI# EC7 Do Not Stuff /EMI/X
STP_CPU# EC10 Do Not Stuff /EMI/X
C_PCI_SB_R CC36 Do Not Stuff /RF
FS4 CC37 Do Not Stuff /X
S_SMBDATA EC14 22PF/50V /RF
S_SMBCLK EC15 22PF/50V /RF
C_DOC_REQ EC16 Do Not Stuff /EMI/X
C_FSLC CC39 22PF/50V /RF
C_FSLA CC40 Do Not Stuff /RF
C_48M_R CC35 Do Not Stuff /RF
C_LAN_25M_R CC11 22PF/50V /RF
C_PCIE_LAN EC17 10PF/50V /EMI/X
C_PCIE_LAN# EC18 10PF/50V /EMI/X
C_PCI_DEBUG EC19 10PF/50V /EMI/X
C_LPC_EC EC20 10PF/50V /EMI/X
C_14M_SB EC21 10PF/50V /EMI/X
GND

For RF,EMI

+3V_CLK
C_FSLB CR5 10KOhm CR32 8.2KOhm /X GND
C_FSLA 8.2KOHM CRN2B
C_FSLC 8.2KOHM CRN2A
C_48M_R 8.2KOHM CRN2D
8.2KOHM CRN2C GND

FSLC	FSLB	FSLA	CPU(MHZ)
0	1	1	166
0	0	1	133

8.2KOHM CRN1D
C_REQ#_WLAN 8.2KOHM CRN1B
PEREQ1# 8.2KOHM CRN1C
C_PCI_SB_R 8.2KOHM CRN1A

FS4 CR2 /X Do Not Stuff
CR9 8.25kOhm GND
FOR 合料

+3V_CLK
CR36 Do Not Stuff 1% N/A
C_DOC_REQ
CR37 Do Not Stuff 1% /DOC
CQ2A Do Not Stuff /DOC
CR38 39KOHM /X
CQ2B Do Not Stuff /DOC
24 DOC1
DOC2 24
GND

+3VS
CR44 10KOhm
CLK_EN
CR13 Do Not Stuff /X
CC34 Do Not Stuff /X
CQ4 2N7002 /X
35 CLK_EN#
GND

CR17 Do Not Stuff
CLK_EN
+3V_CLK
CR16 10KOhm
VCCP_OK_R#
CQ1B UM6K1N
CQ1A UM6K1N
37,38,42 VCCP_PWRGD
Clock enable.
GND

O_DOC1	O_DOC2	Voltage	Status
L	L	2.4-3.3V	Super
L	H	0.5-2.36V	Normal
H	*	0-0.35V	Power saving

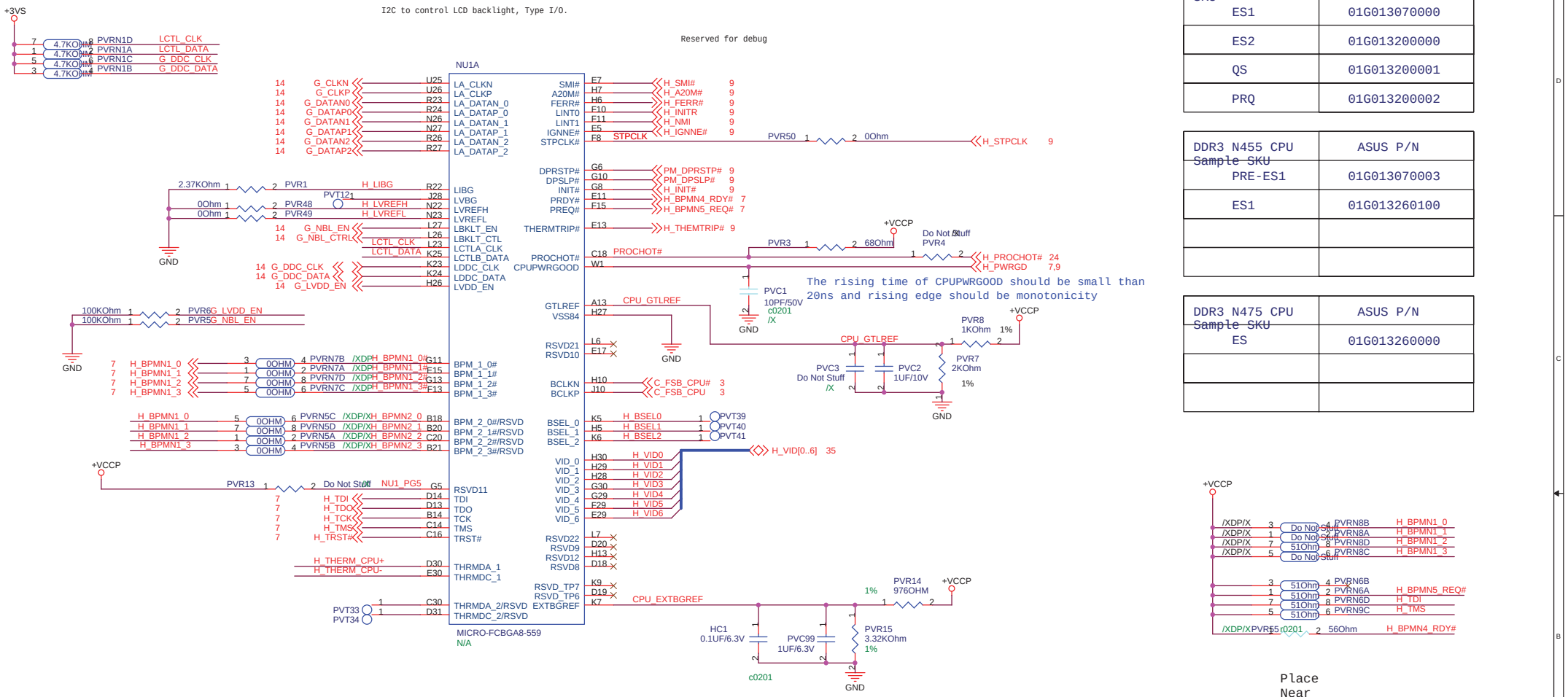
Default Group-1005P SR HIGH END

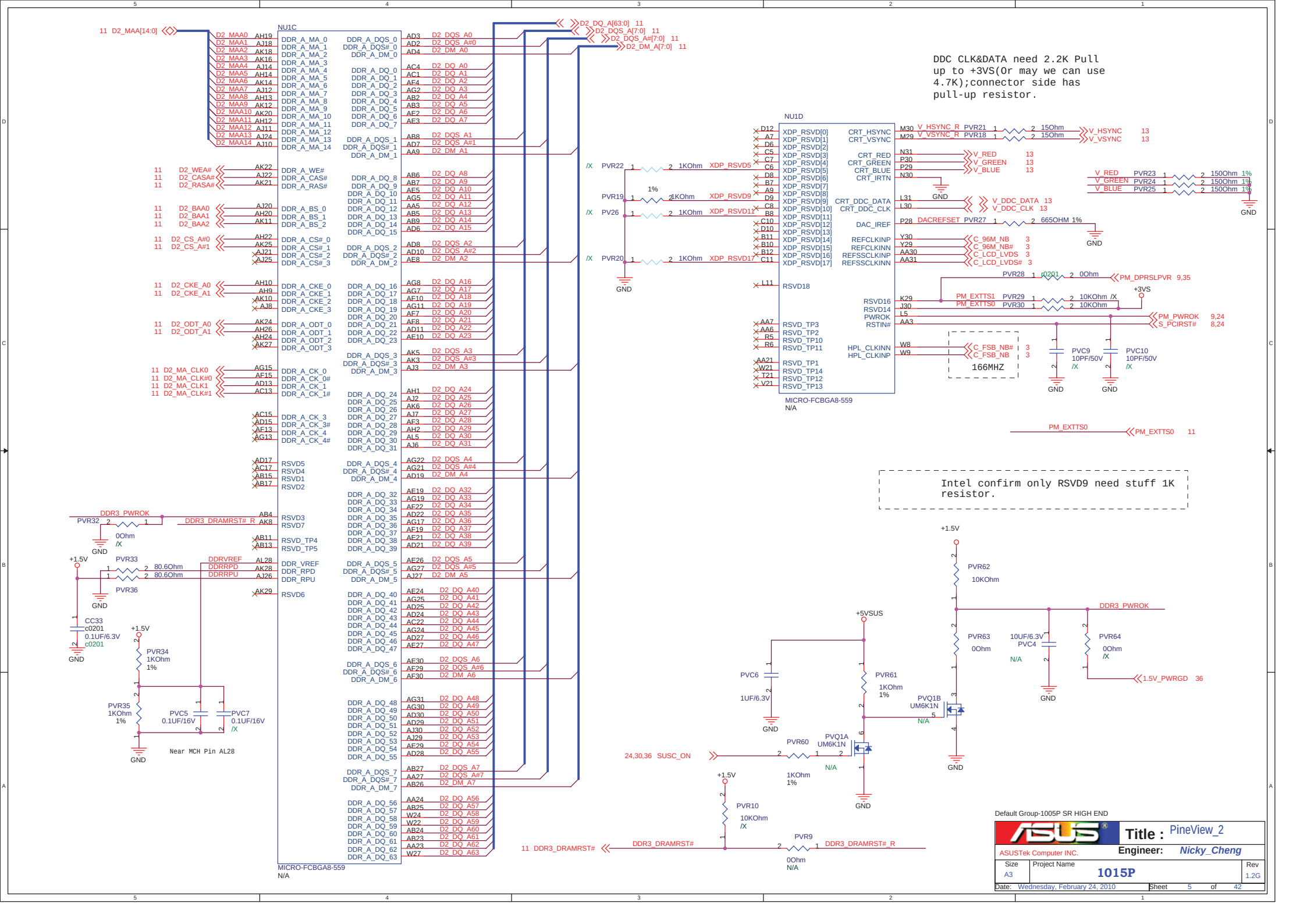
ASUSTek Computer INC.
Title : ICS9LPRS427C
Engineer: Nicky_Cheng
Size A3
Project Name 1015P
Rev 1.2G
Date: Wednesday, February 24, 2010
Sheet 3 of 42

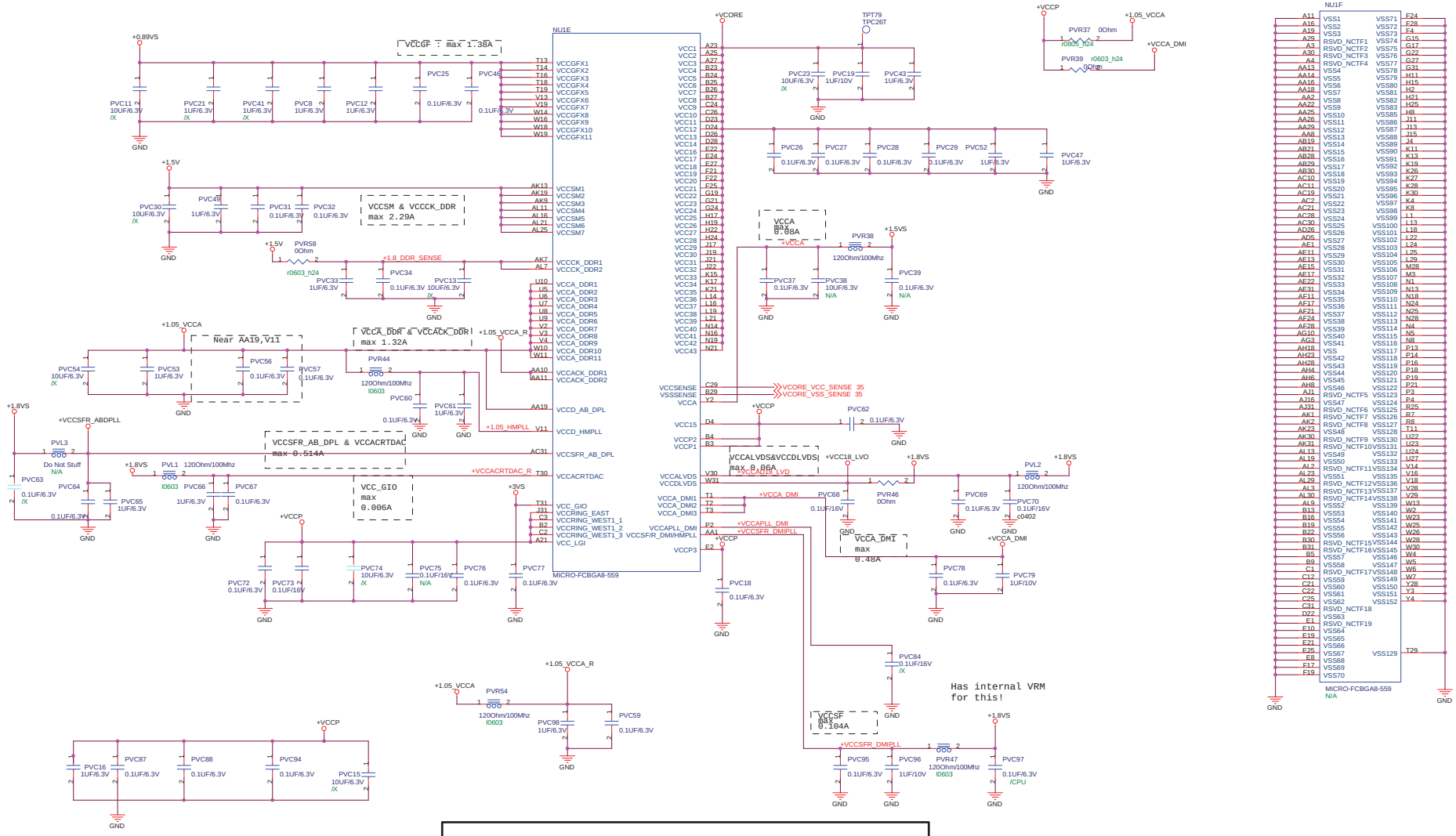
DDR2 CPU Sample SKU	ASUS P/N
ES1	01G013070000
ES2	01G013200000
QS	01G013200001
PRQ	01G013200002

DDR3 N455 CPU Sample SKU	ASUS P/N
PRE-ES1	01G013070003
ES1	01G013260100

DDR3 N475 CPU Sample SKU	ASUS P/N
ES	01G013260000




NU1C
MICRO-FCBGA8-559
N/A
NU1D
MICRO-FCBGA8-559
N/A
DDC CLK&DATA need 2.2K Pull up to +3VS(Or may we can use 4.7K);connector side has pull-up resistor.
Intel confirm only RSVD9 need stuff 1K resistor.
166MHZ
Near MCH Pin AL28
Default Group-1005P SR HIGH END
Title : PineView_2
ASUSTek Computer INC.
Engineer: Nicky_Cheng
Size A3
Project Name 1015P
Rev 1.2G
Date: Wednesday, February 24, 2010
Sheet 5 of 42

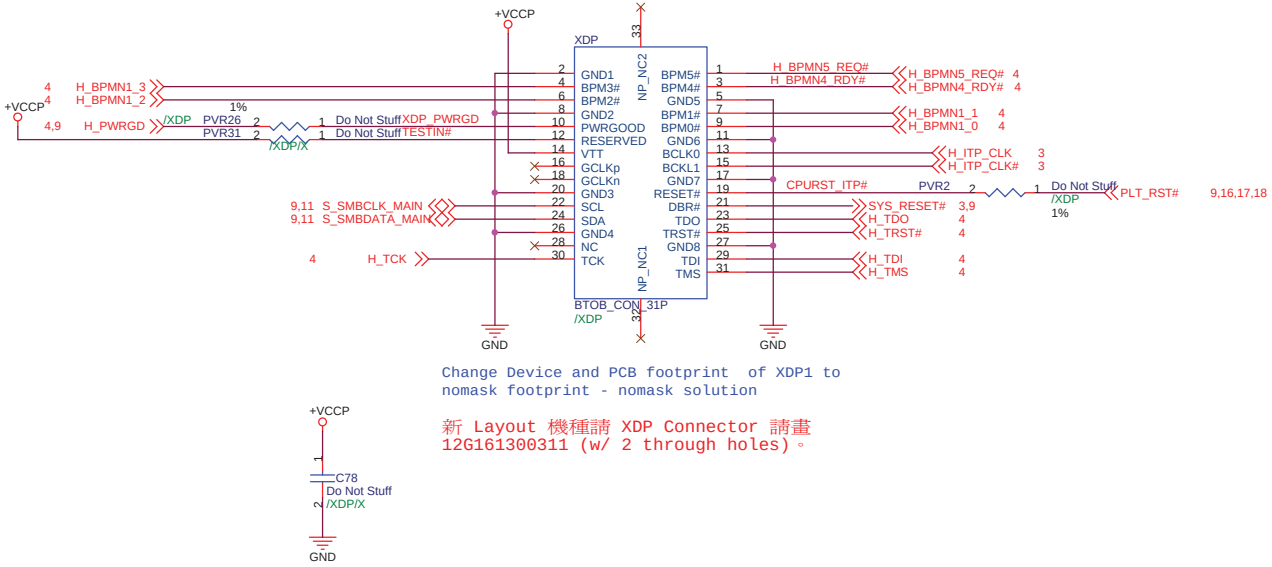


VCC = 3.5A
VCCA =0.08A
VCCGFX =1.38A
VCCALVDS , VCCDLVDS=0.06A
VCCA_DMI =0.48A
VCCSFR_DMIHMPLL =0.104A
VCCA_DDR and VCCACK_DDR =1.32A
VCCSM and VCCCK_DDR =2.27A
VCCRING_EAST , VCCRING_EAST_WEST , VCC_LGI , VCCD_AB_DPL , VCCD_HMPLL =0.33A
VCC_GIO =0.006A
VCCSFR_AB_DPL , VCCACRTDAC =0.154A

Current for PineView

Default Group-1005P SR HIGH END

ASUSTek Computer INC.	Title : PineView_3	
	Engineer: Nicky_Cheng	
Size: A2	Project Name: 1015P	Rev: 1.2G
Date: Wednesday, February 24, 2010	Sheet 6 of 42	



Change Device and PCB footprint of XDP1 to nomask footprint - nomask solution

新 Layout 機種請 XDP Connector 請畫 12G161300311 (w/ 2 through holes)。

Default Group-1005P SR HIGH END

ASUSTek Computer INC.	Title : XDP	
	Engineer: Nicky_Cheng	
Size: A3	Project Name: 1015P	Rev: 1.2G
Date: Wednesday, February 24, 2010	Sheet 7 of 42	

FOR 合料

USB0	USB CONN
USB1	USB CONN
USB2	USB CONN
USB3	USIM
USB4	Card Reader
USB5	Camera
USB6	Blue tooth
USB7	3G

Near Tigerpoint.

Remain PCICLK .

For strapping as Top-block Swap override.

STRAP1#/GPIO48 STRAP2#/GPIO17 Routing
0 1: Flash Cycles Routed to SPI
1 0: Flash Cycles Routed to PCI
1 1: Flash Cycles Routed to LPC

Default Group-1005P SR HIGH END

ASUSTek Computer INC.

Title : DMI&USB

Engineer: Nicky_Cheng

Size	Project Name	Rev
A3	1015P	1.2G

Date: Wednesday, February 24, 2010 Sheet 8 of 42

CLK 14MHZ has a 22ohm resistor near clk Gen.

LDRQ0/1 LPC DMA/master request,ICH7M has internal PU, but we need TPT datasheet

SATA RX,TX all need AC couple and place near Connector side for signal quality.And Traces to them should match length. ICH7M need pull down RX, if no use.

LAD[0:3] INT PU 20K

SU1C

MMAP-360

SU1D

MMAP-360

Already 10K pull up to +3VS in clk gen section.

PCICLK Run,if no use must PU!

0 ohm for debugging later.

Reserved as intel demo sck.

SB Sample SKU	ASUS P/N
QS	02G0010026301
PRQ	02G0010026302

Change from 10K to 2.2K

Main system SMBUS.

PCB ID.

PCB ID.

RTC well input requires pull down to reduce leakage from coin cell battery in G3.
Cann't float in G3.

RTC power.

DMI strap.

1=DMI interface is strapped to operate in DC coupled mode.
0=DMI interface is straped to operate in AC coupled mode.

For Rechargeable solution: Mount TPR2

For NON-Rechargeable solution: Unmount TPR2

Default Group-1005P SR HIGH END

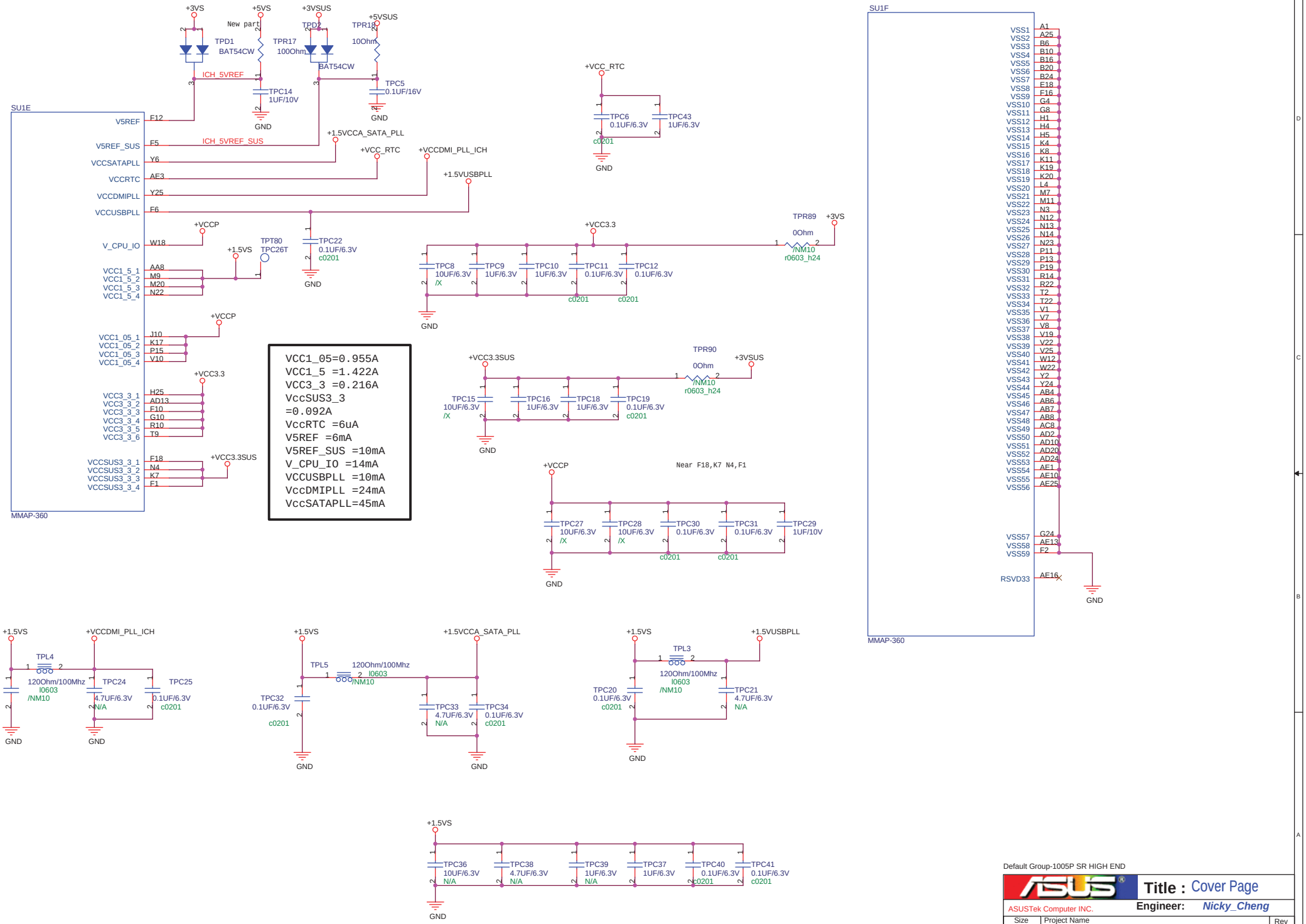
Title : SCH system

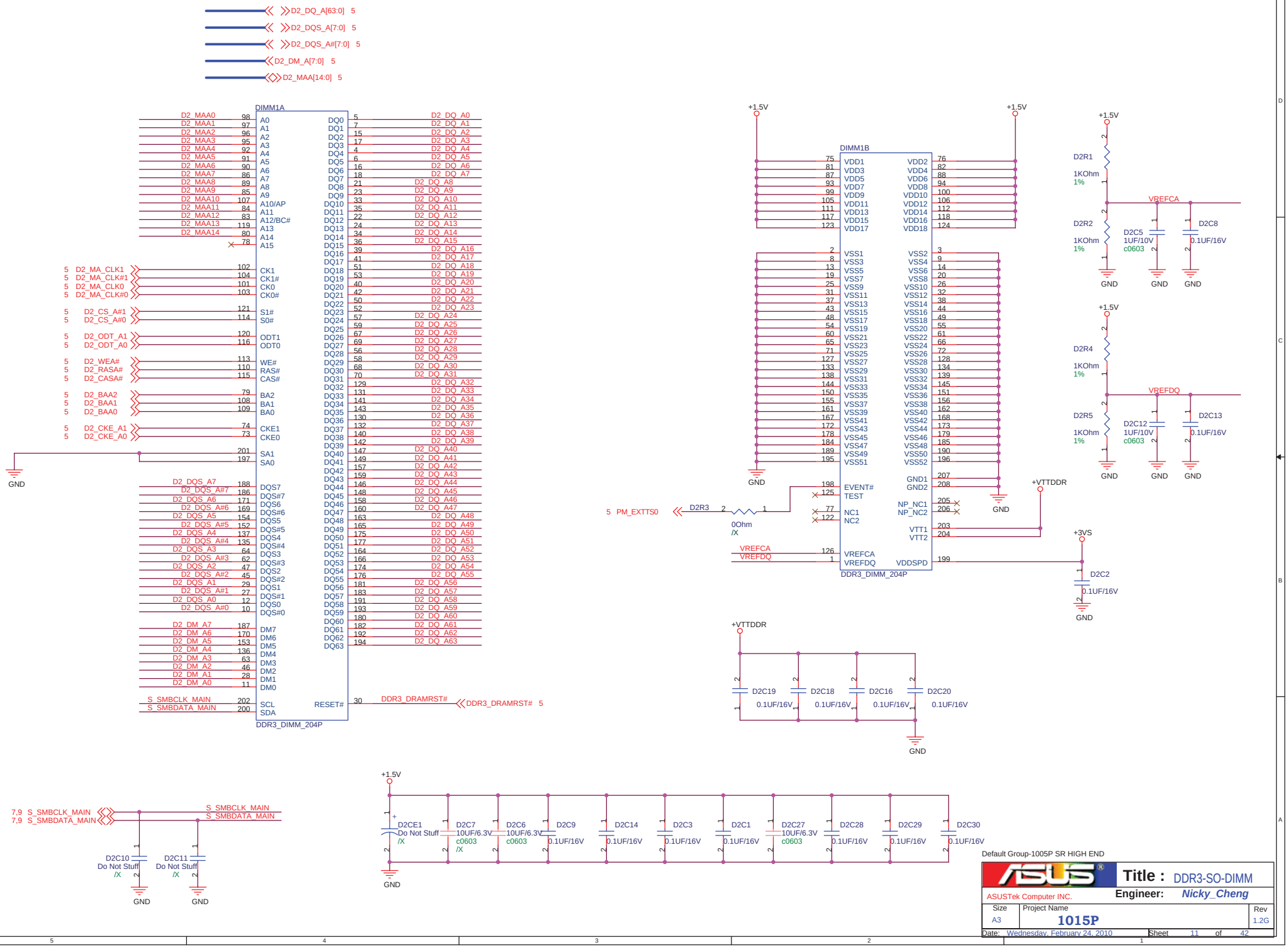
ASUSTek Computer INC.

Engineer: Nicky_Cheng

Size	Project Name	Rev
A2	1015P	1.2G

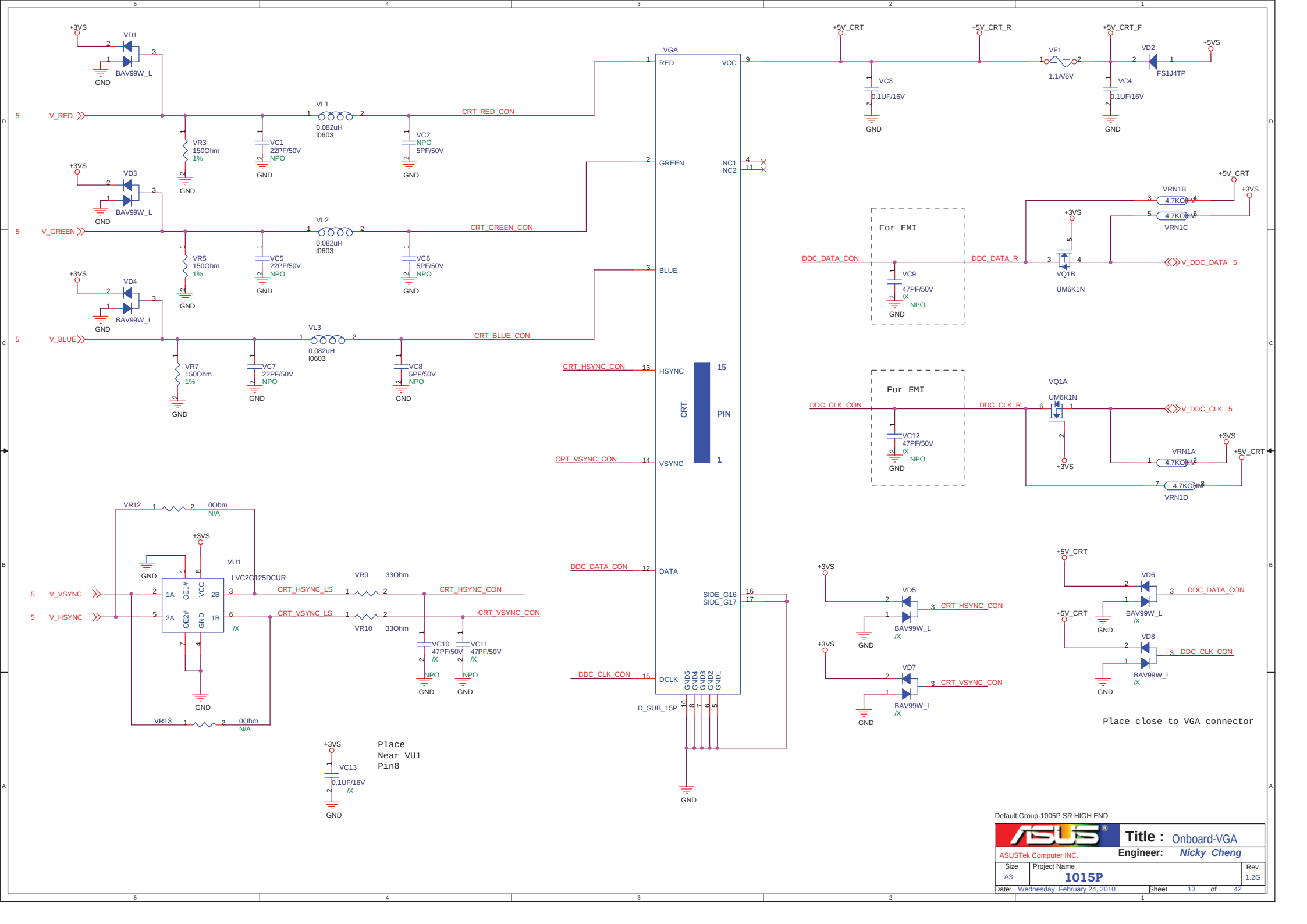
Date: Wednesday, February 24, 2010 Sheet 9 of 42

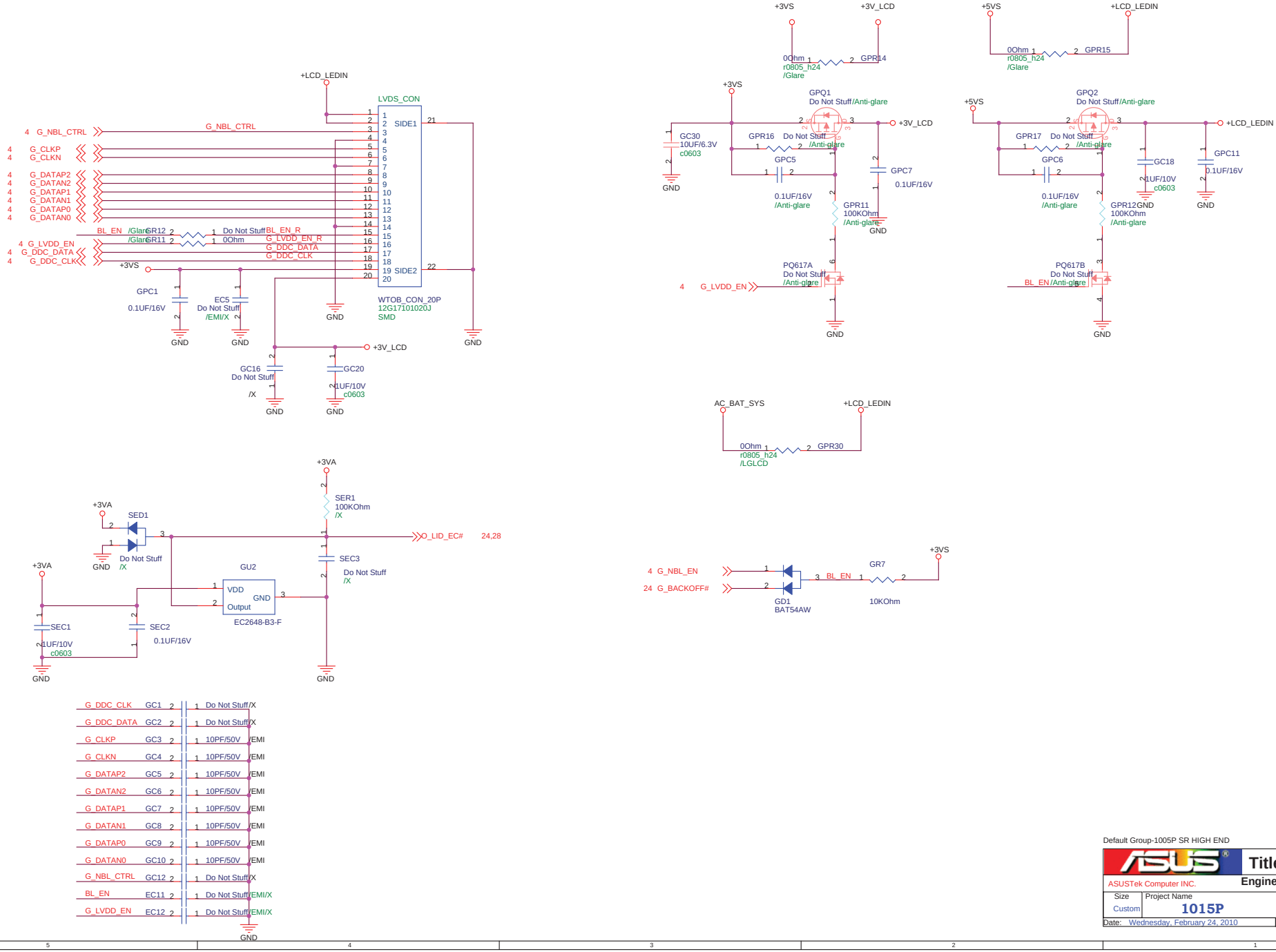

SU1E
V5REF
V5REF_SUS
VCCSATAPLL
VCCRTC
VCCDMIPLL
VCCUSBPLL
V_CPU_IO
VCC1_5_1
VCC1_5_2
VCC1_5_3
VCC1_5_4
VCC1_05_1
VCC1_05_2
VCC1_05_3
VCC1_05_4
VCC3_3_1
VCC3_3_2
VCC3_3_3
VCC3_3_4
VCC3_3_5
VCC3_3_6
VCCSUS3_3_1
VCCSUS3_3_2
VCCSUS3_3_3
VCCSUS3_3_4
MMAP-360
+3VS
+5VS
+3VSUS
+5VSUS
New part
TPD1
BAT54CW
TPR17
100Ohm
TPD2
TPR18
10Ohm
BAT54CW
ICH_5VREF
ICH_5VREF_SUS
TPC14
1UF/10V
TPC5
0.1UF/16V
GND
+1.5VCCA_SATA_PLL
+VCC_RTC
+VCCDMI_PLL_ICH
+1.5VUSBPLL
+VCCP
+1.5VS
TPT80
TPC26T
TPC22
0.1UF/6.3V
c0201
+VCC3.3
TPR89
0Ohm
/NM10
r0603_h24
TPC8
10UF/6.3V
/X
TPC9
1UF/6.3V
TPC10
1UF/6.3V
TPC11
0.1UF/6.3V
TPC12
0.1UF/6.3V
+VCC3.3SUS
TPR90
TPC15
10UF/6.3V
TPC16
1UF/6.3V
TPC18
1UF/6.3V
TPC19
0.1UF/6.3V
Near F18,K7 N4,F1
TPC27
10UF/6.3V
TPC28
10UF/6.3V
TPC30
0.1UF/6.3V
TPC31
0.1UF/6.3V
TPC29
1UF/10V
VCC1_05=0.955A
VCC1_5 =1.422A
VCC3_3 =0.216A
VccSUS3_3
=0.092A
VccRTC =6uA
V5REF =6mA
V5REF_SUS =10mA
V_CPU_IO =14mA
VCCUSBPLL =10mA
VccDMIPLL =24mA
VccSATAPLL=45mA
TPL4
120Ohm/100Mhz
l0603
/NM10
TPC23
TPC24
4.7UF/6.3V
N/A
TPC25
TPL5
TPC32
TPC33
TPC34
TPL3
TPC20
TPC21
TPC36
TPC38
TPC39
TPC37
TPC40
TPC41
SU1F
MMAP-360
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
VSS14
VSS15
VSS16
VSS17
VSS18
VSS19
VSS20
VSS21
VSS22
VSS23
VSS24
VSS25
VSS26
VSS27
VSS28
VSS29
VSS30
VSS31
VSS32
VSS33
VSS34
VSS35
VSS36
VSS37
VSS38
VSS39
VSS40
VSS41
VSS42
VSS43
VSS44
VSS45
VSS46
VSS47
VSS48
VSS49
VSS50
VSS51
VSS52
VSS53
VSS54
VSS55
VSS56
VSS57
VSS58
VSS59
RSVD33
Default Group-1005P SR HIGH END
Title : Cover Page
ASUSTek Computer INC.
Engineer: Nicky_Cheng
Size
A3
Project Name
1015P
Rev
1.2G
Date: Wednesday, February 24, 2010
Sheet 10 of 42


D2_DQ_A[63:0] 5
D2_DQS_A[7:0] 5
D2_DQS_A#[7:0] 5
D2_DM_A[7:0] 5
D2_MAA[14:0] 5
DIMM1A
DDR3_DIMM_204P
DIMM1B
DDR3_DIMM_204P
+1.5V
GND
+VTTDDR
+3VS
VREFCA
VREFDQ
D2R1
D2R2
D2R3
D2R4
D2R5
1KOhm
1%
0Ohm
/X
D2C5
D2C8
D2C12
D2C13
1UF/10V
0.1UF/16V
c0603
D2C2
D2C19
D2C18
D2C16
D2C20
D2C10
D2C11
Do Not Stuff
D2CE1
D2C7
D2C6
D2C9
D2C14
D2C3
D2C1
D2C27
D2C28
D2C29
D2C30
10UF/6.3V
S_SMBCLK_MAIN
S_SMBDATA_MAIN
DDR3_DRAMRST#
PM_EXTTS0
Default Group-1005P SR HIGH END
Title : DDR3-SO-DIMM
ASUSTek Computer INC.
Engineer: Nicky_Cheng
Size A3
Project Name 1015P
Rev 1.2G
Date: Wednesday, February 24, 2010
Sheet 11 of 42

Default Group-1005P SR HIGH END

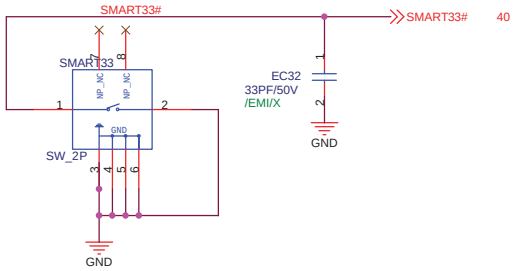
ASUSTek Computer INC.	Title : DDR3	
	Engineer: Nicky_Cheng	
Size: A3	Project Name: 1015P	Rev: 1.2G
Date: Wednesday, February 24, 2010	Sheet 12 of 42	

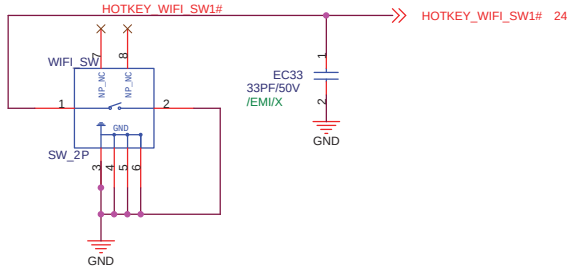

VGA
RED
GREEN
BLUE
HSYNC
VSYNC
DDC_DATA_CON
DDC_CLK_CON
DCLK
DATA
VCC
NC1
NC2
SIDE_G16
SIDE_G17
GND5
GND4
GND3
GND2
GND1
D_SUB_15P
CRT
15
PIN
1
V_RED
V_GREEN
V_BLUE
CRT_RED_CON
CRT_GREEN_CON
CRT_BLUE_CON
VD1
VD3
VD4
BAV99W_L
VL1
VL2
VL3
0.082uH
I0603
VR3
VR5
VR7
150Ohm
1%
VC1
VC5
VC7
22PF/50V
NPO
VC2
VC6
VC8
5PF/50V
+3VS
GND
+5V_CRT
+5V_CRT_R
+5V_CRT_F
+5VS
VF1
1.1A/6V
VD2
FS1J4TP
VC3
VC4
0.1UF/16V
For EMI
VC9
47PF/50V
/X
VQ1B
UM6K1N
VRN1B
VRN1C
VRN1A
VRN1D
4.7KOHM
V_DDC_DATA
V_DDC_CLK
VQ1A
VC12
VU1
LVC2G125DCUR
VR12
VR13
0Ohm
N/A
V_VSYNC
V_HSYNC
CRT_HSYNC_LS
CRT_VSYNC_LS
VR9
VR10
33Ohm
VC10
VC11
47PF/50V
VD5
VD6
VD7
VD8
Place
Near VU1
Pin8
VC13
0.1UF/16V
Place close to VGA connector
Default Group-1005P SR HIGH END
ASUSTek Computer INC.
Title : Onboard-VGA
Engineer: Nicky_Cheng
Size A3
Project Name 1015P
Rev 1.2G
Date: Wednesday, February 24, 2010
Sheet 13 of 42



Default Group-1005P SR HIGH END

ASUSTek Computer INC.	Title : LVDS Conn_LID		
	Engineer: Nicky_Cheng		
Size: Custom	Project Name: 1015P		Rev: 1.2G
Date: Wednesday, February 24, 2010	Sheet 14 of 42		





Default Group-1005P SR HIGH END

ASUSTek Computer INC.

Title : WIFI_SAMRT33

Engineer: *Nicky_Cheng*

Size	Project Name	Rev
A3	**1015P**	1.2G

Date: Wednesday, February 24, 2010 Sheet 15 of 42

LAN AR8132M

Symbol 02G911002600

BOM 02G911002601

	LR2
Normal	N/A
Overclocking	/X

LL1 close to Pin 1

LC2 close to Pin 15

LC8 close to Pin 2

LC20 close to Pin 8

close to pin6

Input 25M,unmount LR4.
Input 48M,mount LR4.

	LU1	LR59	LR58	LC51	LU2	LC49	LC50
AR8132	02G911002600	4.7K	N/A	N/A	N/A	/X	/X
AR8132M	02G911002601	0 ohm	/X	/X	/X	/X	N/A

	LR9	LR10
Normal	N/A	/X
Overclocking	/X	N/A

Close to LU1

Default Group-1005P SR HIGH END

ASUSTek Computer INC.

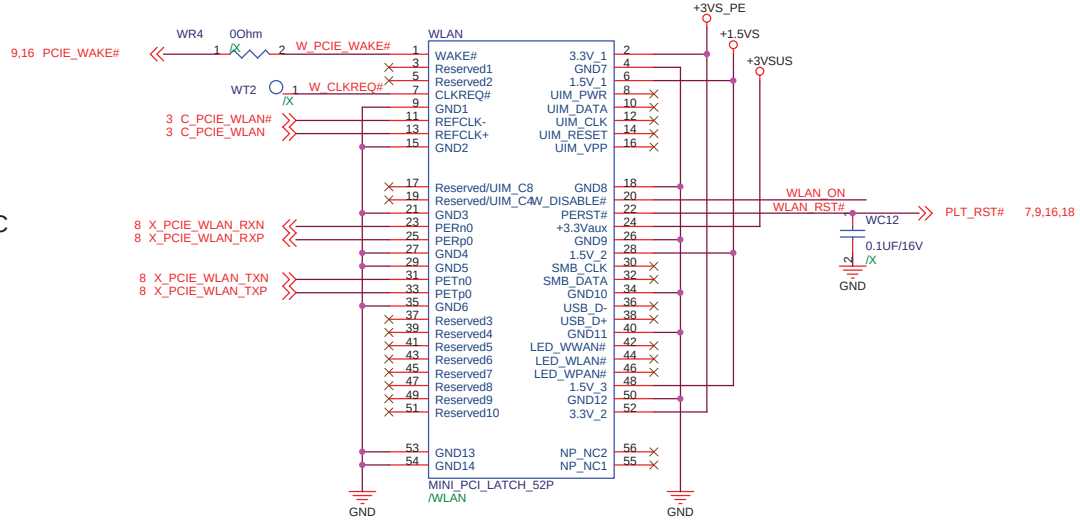
Title : LAN_AR8132

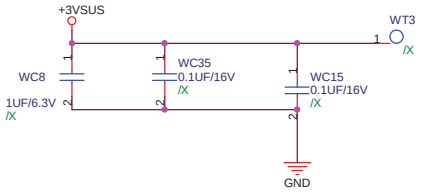
Engineer: Nicky_Cheng

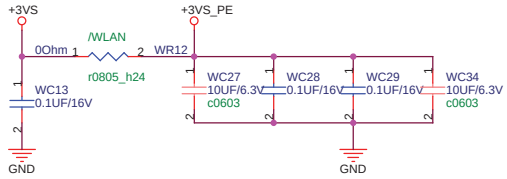
Size	Project Name	Rev
A3	1015P	1.2G

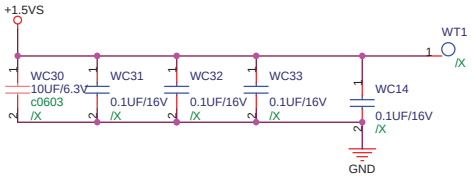
Date: Wednesday, February 24, 2010 Sheet 16 of 41

WIFI use PCIE 1.1 Spec
+3VS = 1.0A peak / 0.75A Normal
+1.5VS = 0.5A peak / 0.375A Normal
+3VSUS = 0.375A peak / 0.25A Normal

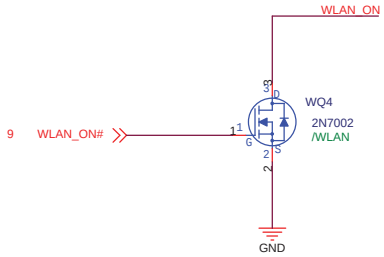






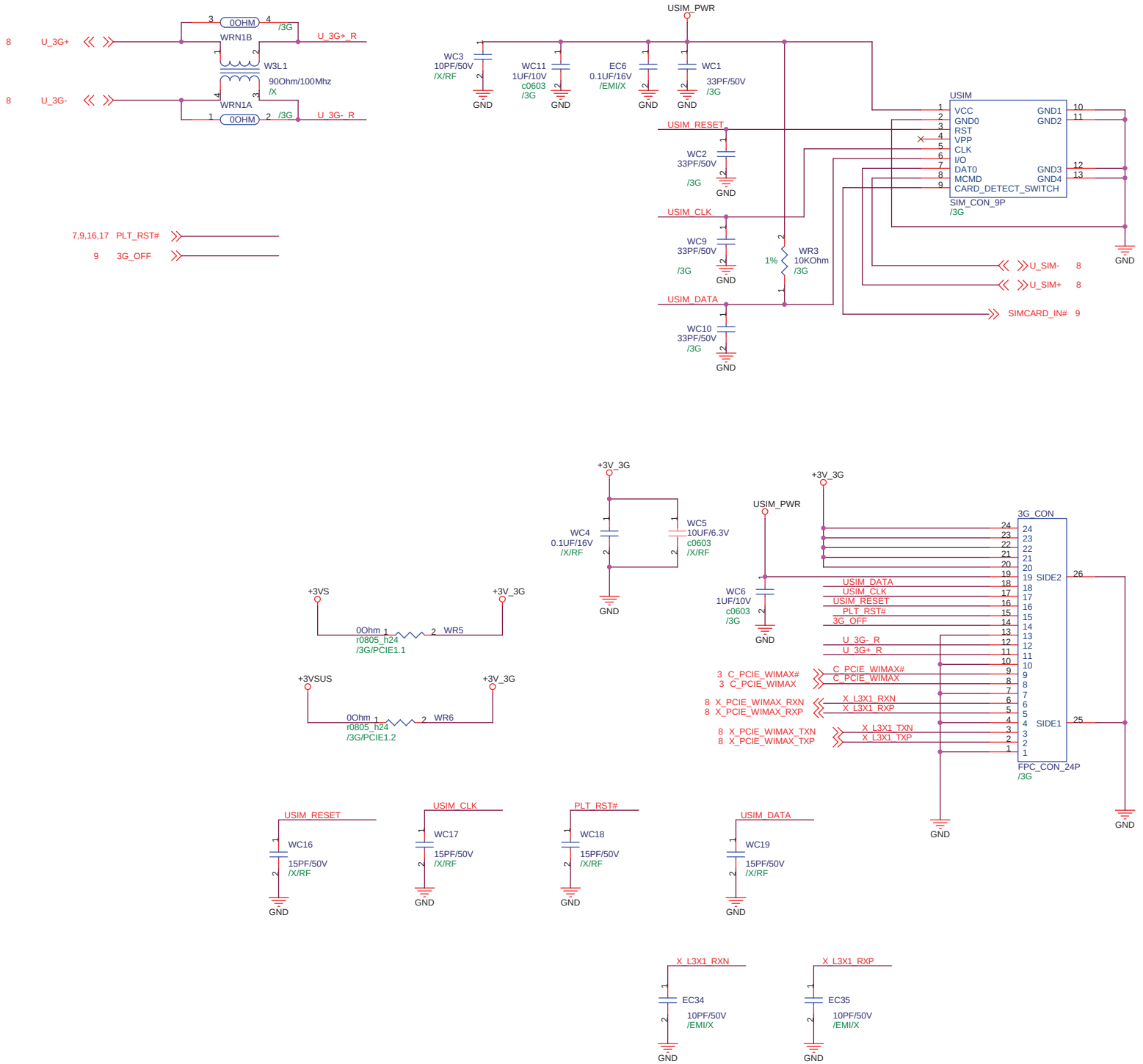






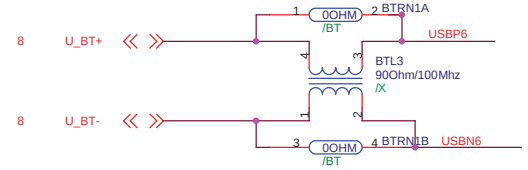
Default Group-1005P SR HIGH END

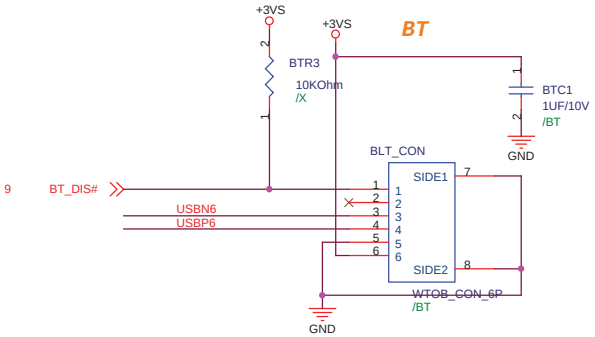
ASUSTek Computer INC.	Title : WLAN	
	Engineer: Nicky_Cheng	
Size: A3	Project Name: 1015P	Rev: 1.2G
Date: Wednesday, February 24, 2010	Sheet 17 of 42	



Default Group-1005P SR HIGH END

ASUSTek Computer INC.	Title : 3G CON	
	Engineer: Nicky_Cheng	
Size: A3	Project Name: 1015P	Rev: 1.2G
Date: Wednesday, February 24, 2010	Sheet 18 of 42	



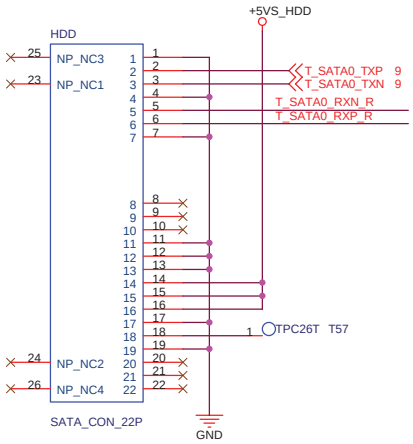


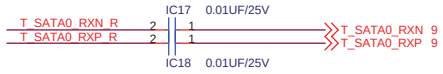
Default Group-1005P SR HIGH END

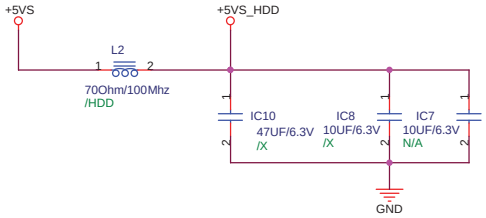
ASUSTek Computer INC.	Title : Bluetooth	
	Engineer: Nicky_Cheng	
Size: A3	Project Name: 1015P	Rev: 1.2G
Date: Wednesday, February 24, 2010	Sheet 19 of 42	

0.1A Beta

SATA HDD Connector







Default Group-1005P SR HIGH END

ASUSTek Computer INC.	Title : HD_CON	
	Engineer: Nicky_Cheng	
Size: A3	Project Name: 1015P	Rev: 1.2G
Date: Wednesday, February 24, 2010	Sheet 20 of 42	

Default Group-1005P SR HIGH END

Title : USB3.0

ASUSTek Computer INC.

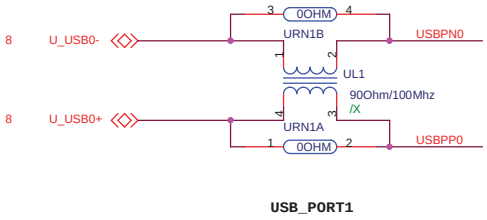
Engineer:

Size	Project Name	Rev
C	1015P	1.2G

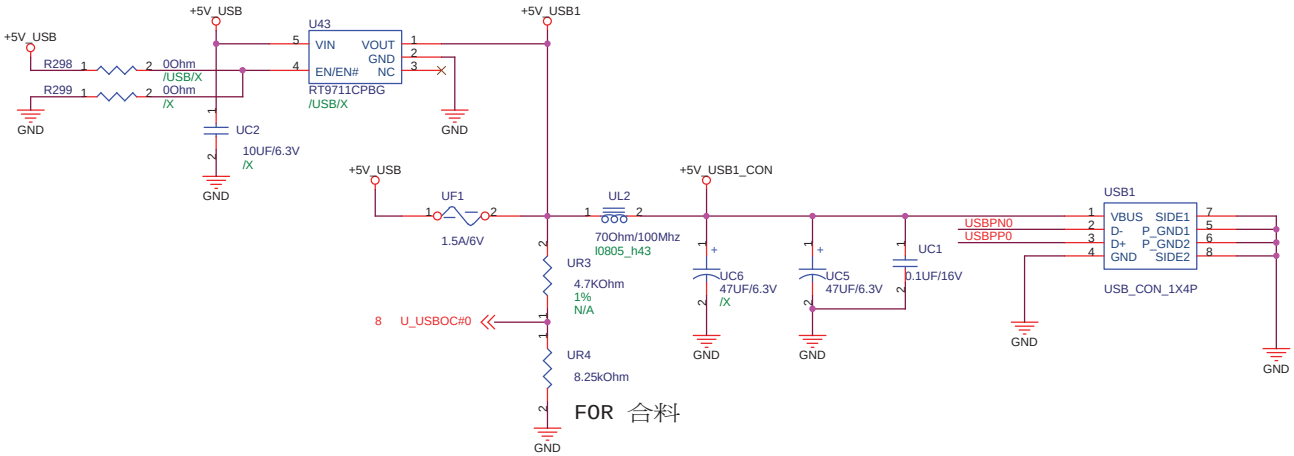
Date: Wednesday, February 24, 2010 Sheet 21 of 42

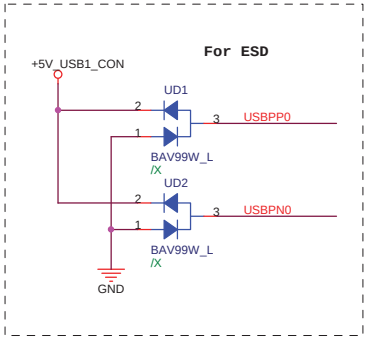
Default Group-1005P SR HIGH END

ASUSTek Computer INC.	Title : USB 3.0	
	Engineer: Nicky_Cheng	
Size: A3	Project Name: 1015P	Rev: 1.2G
Date: Wednesday, February 24, 2010	Sheet 22 of 42	



USB_PORT1





Default Group-1005P SR HIGH END

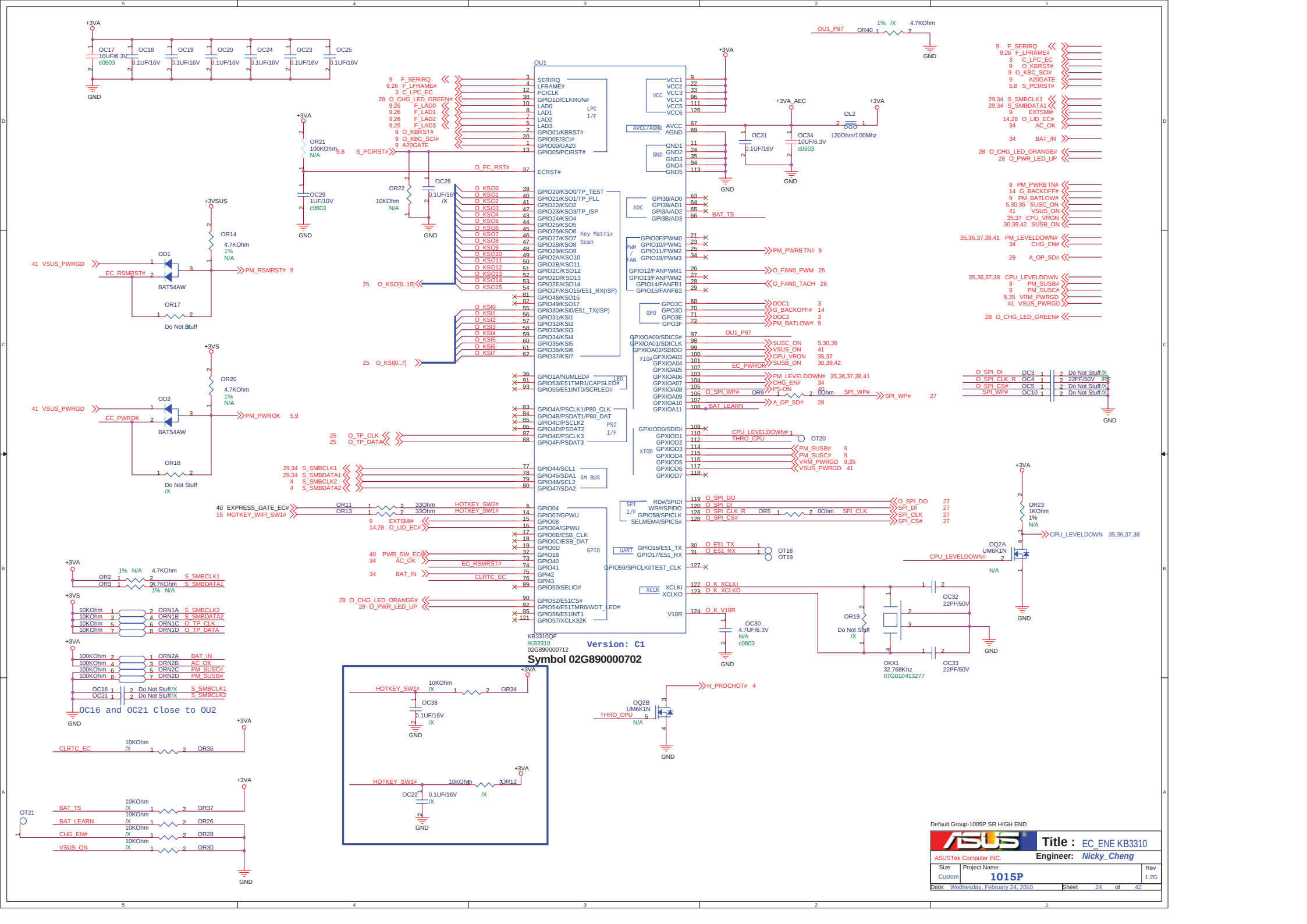
ASUSTek Computer INC.

Title : USB Port1

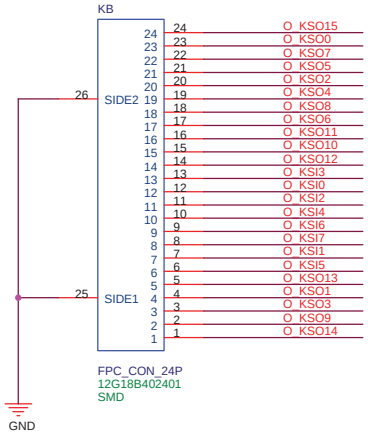
Engineer: Nicky_Cheng

Size	Project Name	Rev
A3	1015P	1.2G

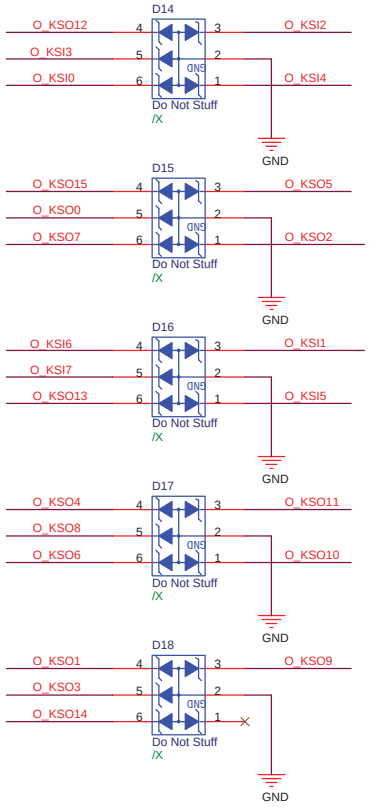
Date: Wednesday, February 24, 2010 Sheet 23 of 42


OU1
KB3310QF
/KB3310
02G890000712
Version: C1
Symbol 02G890000702
OC16 and OC21 Close to OU2
Default Group-1005P SR HIGH END
ASUSTek Computer INC.
Title : EC_ENE KB3310
Engineer: Nicky_Cheng
Size: Custom
Project Name: 1015P
Rev: 1.2G
Date: Wednesday, February 24, 2010
Sheet 24 of 42

For Keyboard Connector

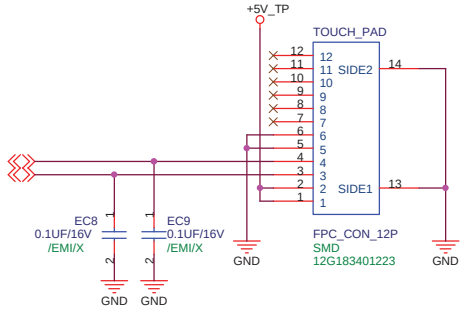


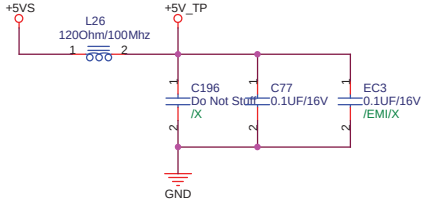
24 O_KSO[0..15]
24 O_KSI[0..7]



For Touch-Pad

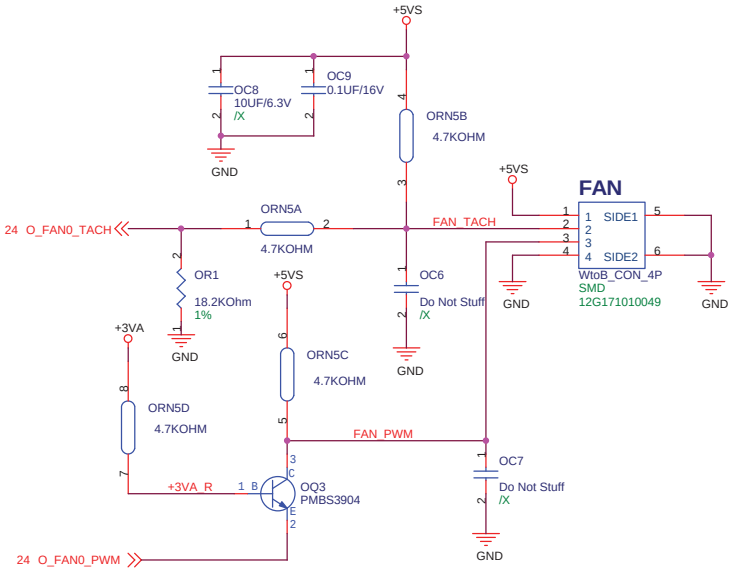
24 O_TP_CLK
24 O_TP_DATA

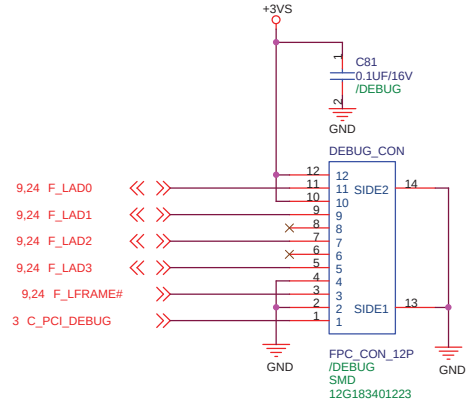




Default Group-1005P SR HIGH END

ASUSTek Computer INC.	Title : KB_TP	
	Engineer: Nicky_Cheng	
Size: A3	Project Name: 1015P	Rev: 1.2G
Date: Wednesday, February 24, 2010	Sheet 25 of 42	





Default Group-1005P SR HIGH END

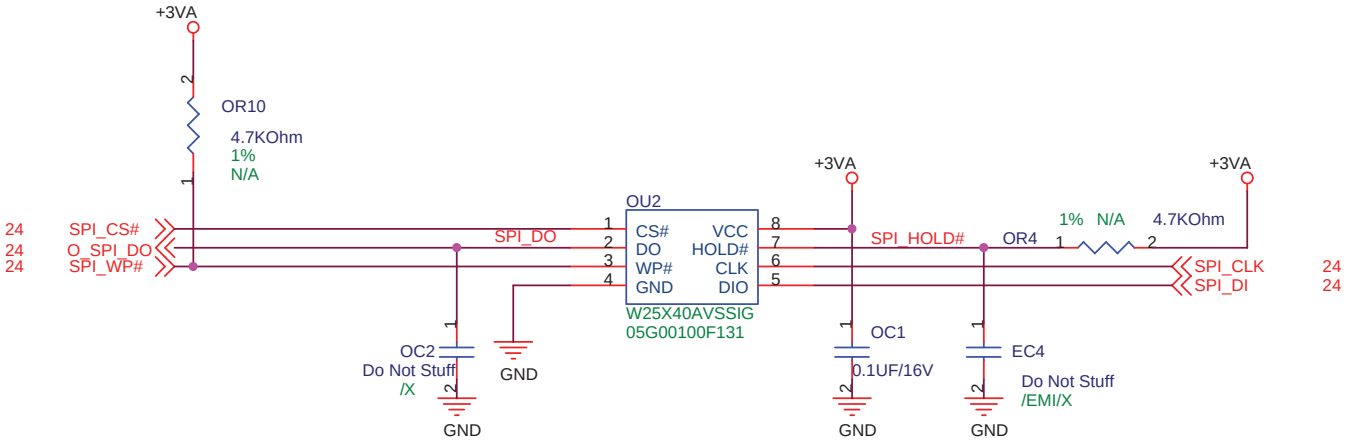
ASUSTek Computer INC.

Title : Fan_Debug

Engineer: *Nicky_Cheng*

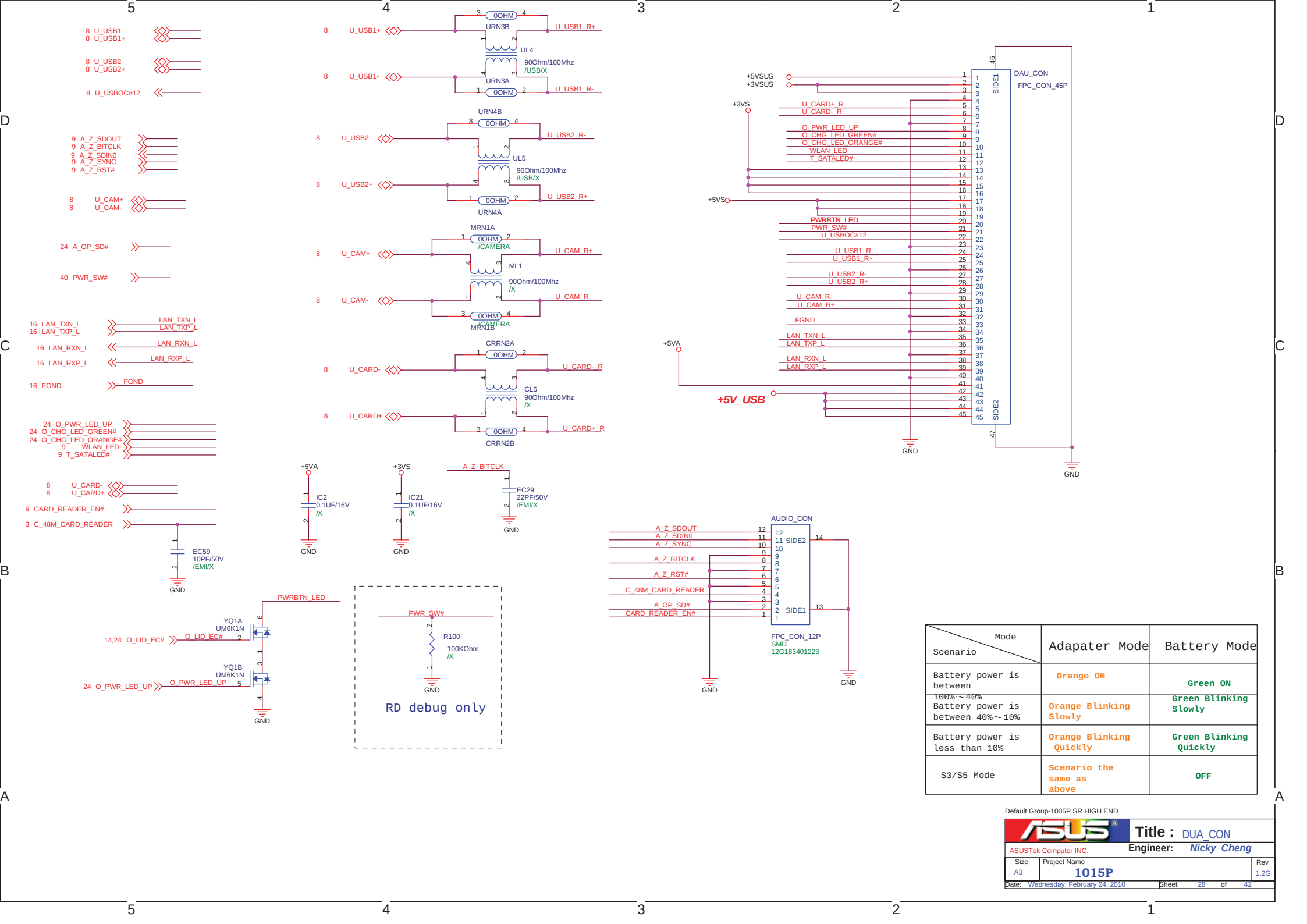
Size	Project Name	Rev
A3	**1015P**	1.2G

Date: Wednesday, February 24, 2010 Sheet 26 of 42



Default Group-1005P SR HIGH END

ASUSTek Computer INC.	Title : SPI_ROM	
	Engineer: Nicky_Cheng	
Size: A4	Project Name: 1015P	Rev: 1.2G
Date: Wednesday, February 24, 2010	Sheet 27 of 42	



Scenario \ Mode	Adapater Mode	Battery Mode
Battery power is between 100%～40%	Orange ON	Green ON
Battery power is between 40%～10%	Orange Blinking Slowly	Green Blinking Slowly
Battery power is less than 10%	Orange Blinking Quickly	Green Blinking Quickly
S3/S5 Mode	Scenario the same as above	OFF

Default Group-1005P SR HIGH END

ASUSTek Computer INC.

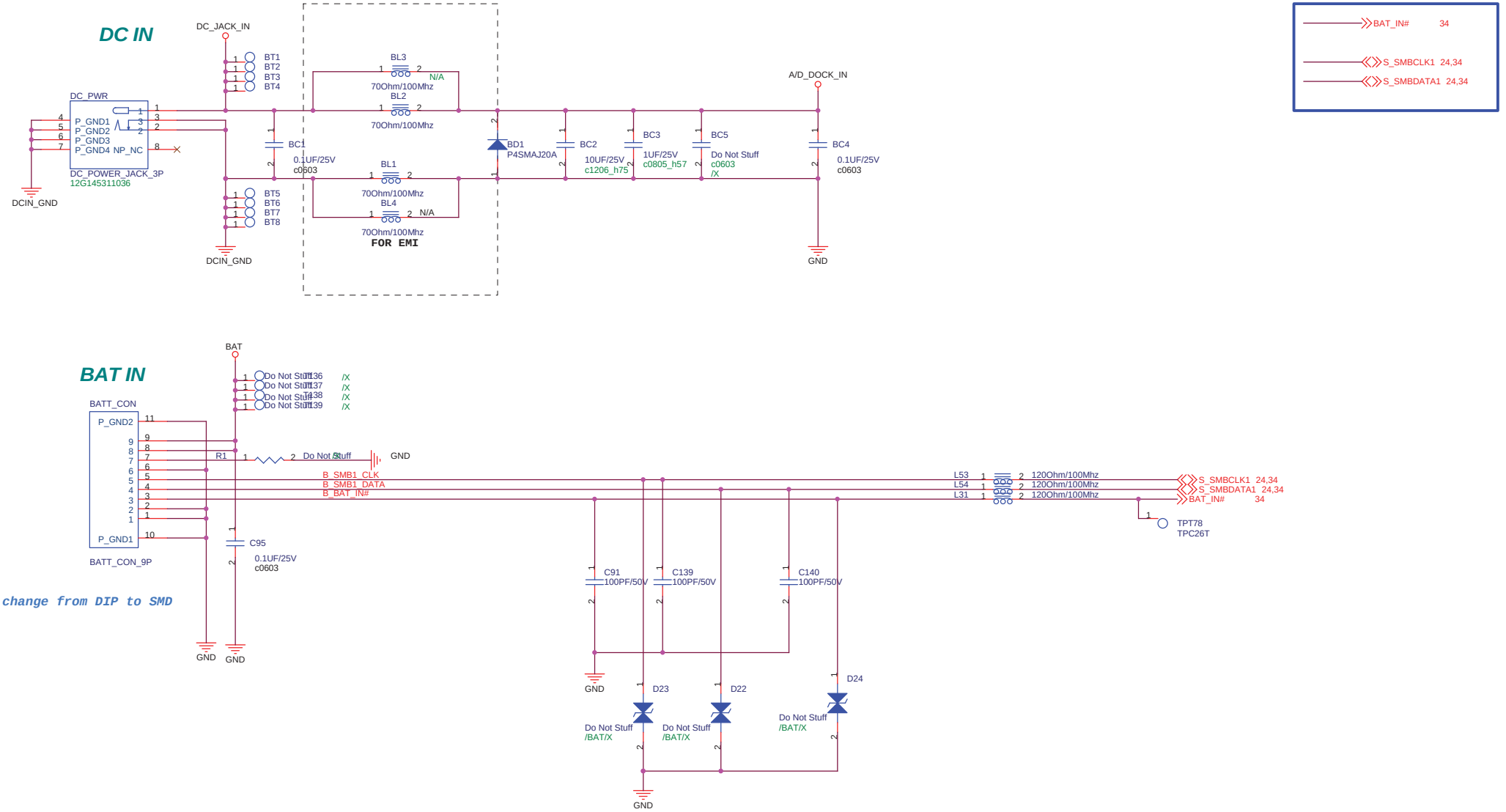
Title : DUA_CON

Engineer: Nicky_Cheng

Size	Project Name	Rev
A3	1015P	1.2G

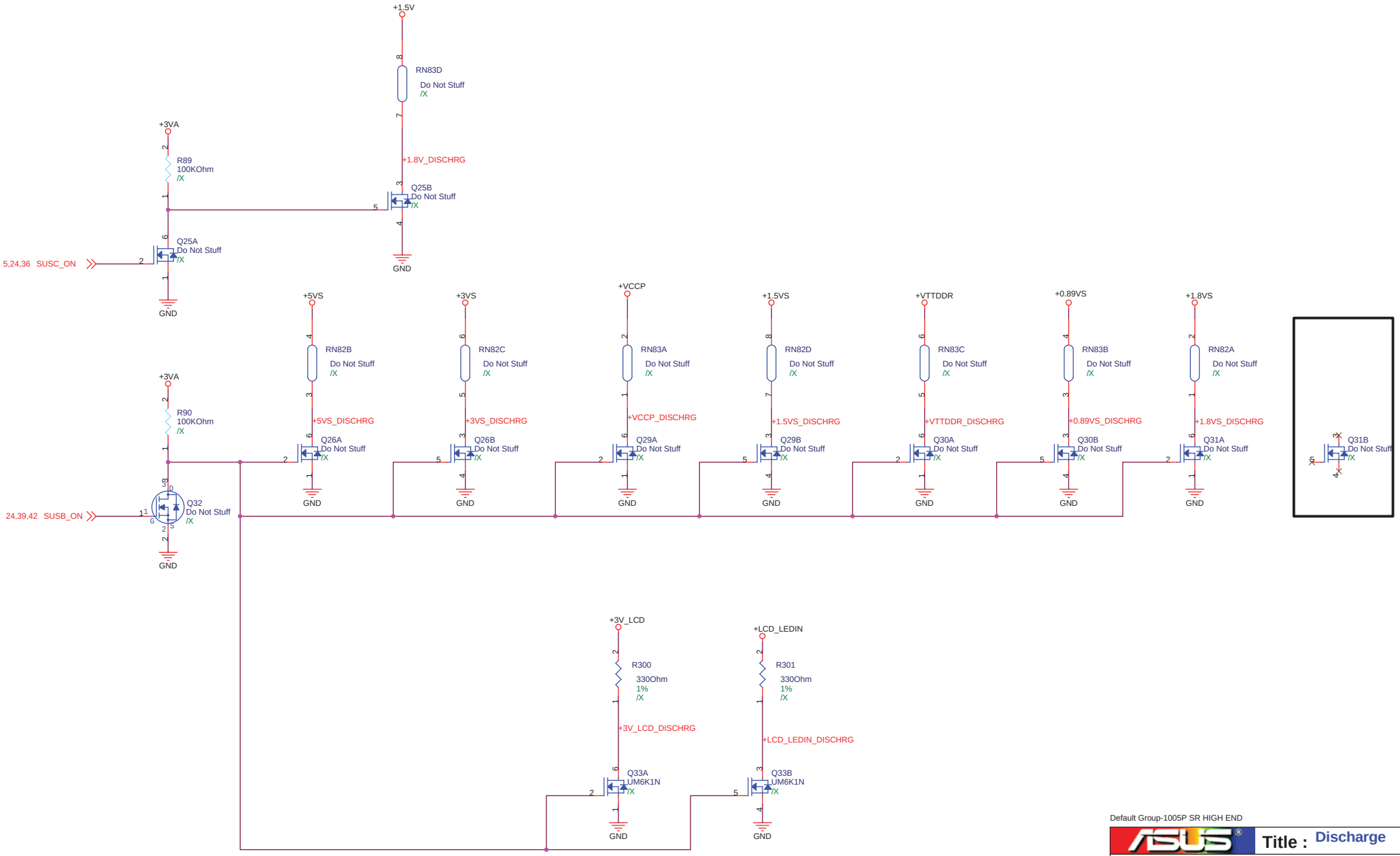
Date: Wednesday, February 24, 2010 Sheet 28 of 42

0.1B Beta



Default Group-1005P SR HIGH END

ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: Nicky_Cheng	
Size: A3	Project Name: 1015P	Rev: 1.2G
Date: Wednesday, February 24, 2010	Sheet 29 of 42	

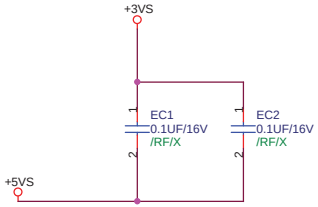


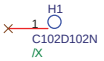
Default Group-1005P SR HIGH END

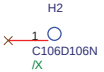
ASUSTek Computer INC.	Title : Discharge	
	Engineer: Nicky_Cheng	
Size: A3	Project Name: 1015P	Rev: 1.2G
Date: Wednesday, February 24, 2010	Sheet 30 of 42	

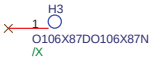
Default Group-1005P SR HIGH END

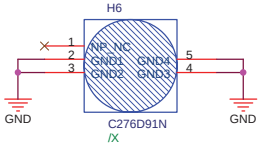
ASUSTek Computer INC.	Title : SD_CON	
	Engineer: *Nicky_Cheng*	
Size: A3	Project Name: **1015P**	Rev: 1.2G
Date: Wednesday, February 24, 2010	Sheet 31 of 42	

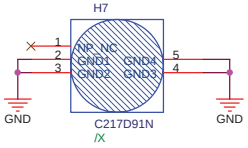


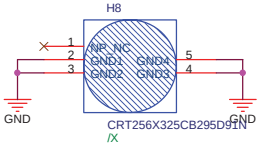


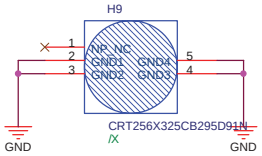


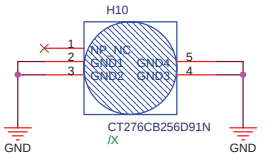


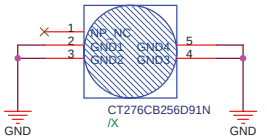


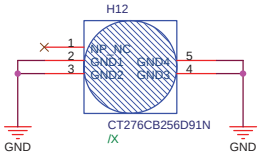


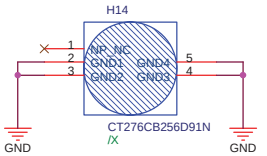


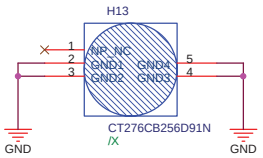


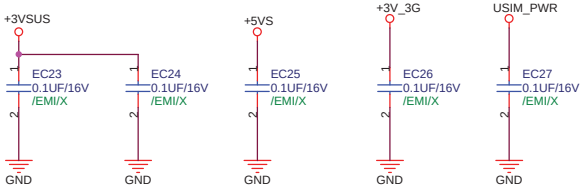


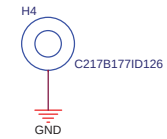




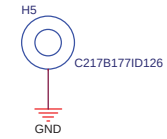


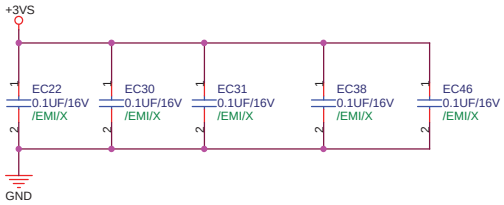


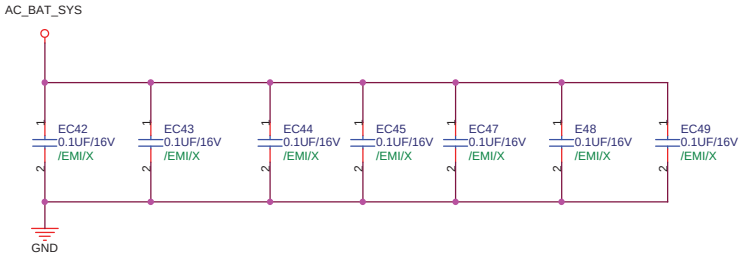




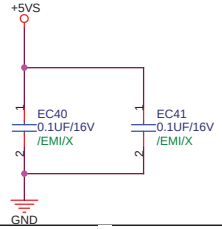
CPU Thermal HOLD











Default Group-1005P SR HIGH END

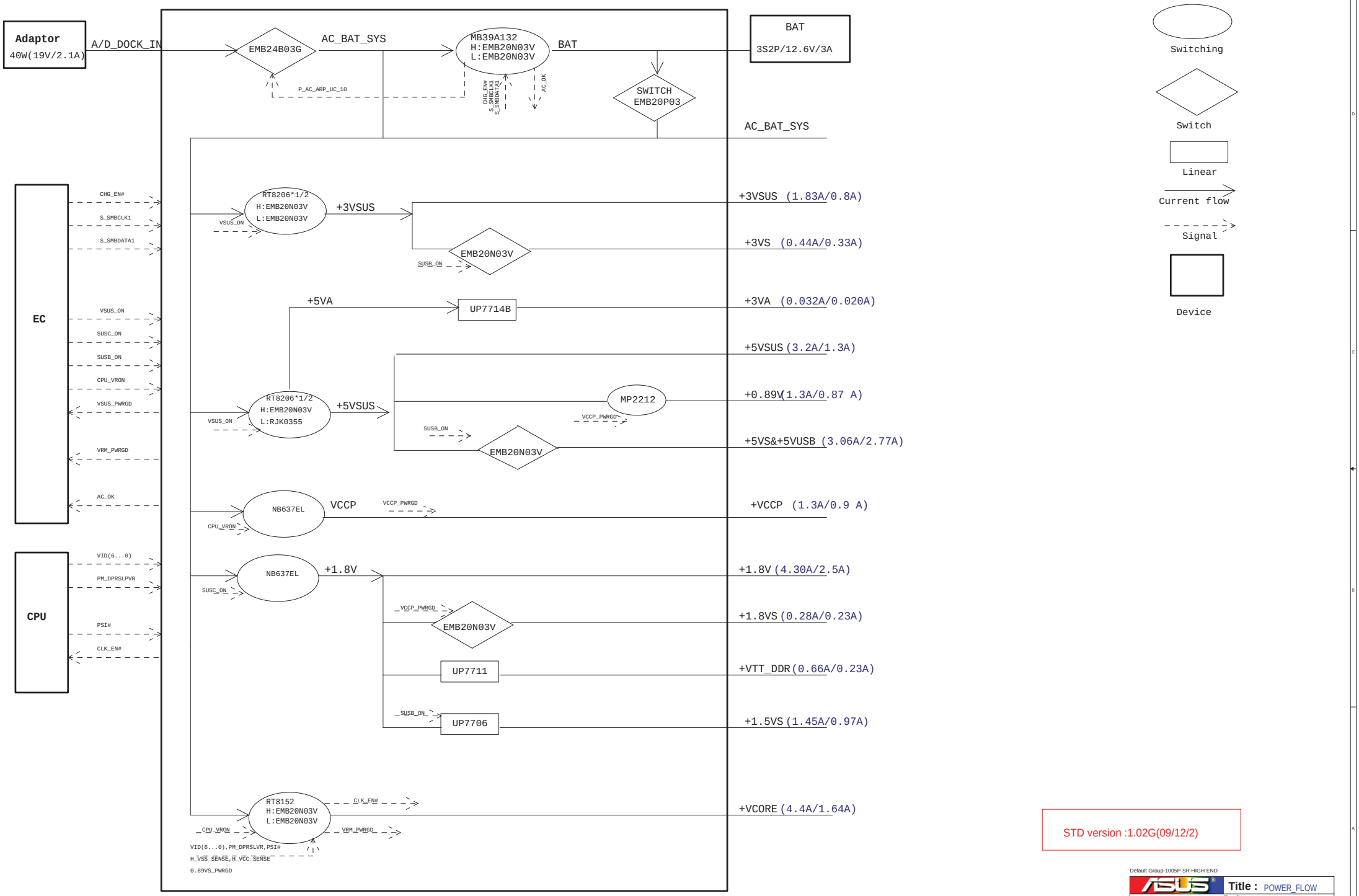
ASUSTek Computer INC.

Title : SREW HOLE&EMI

Engineer: Nicky_Cheng

Size	Project Name	Rev
A3	1015P	1.2G

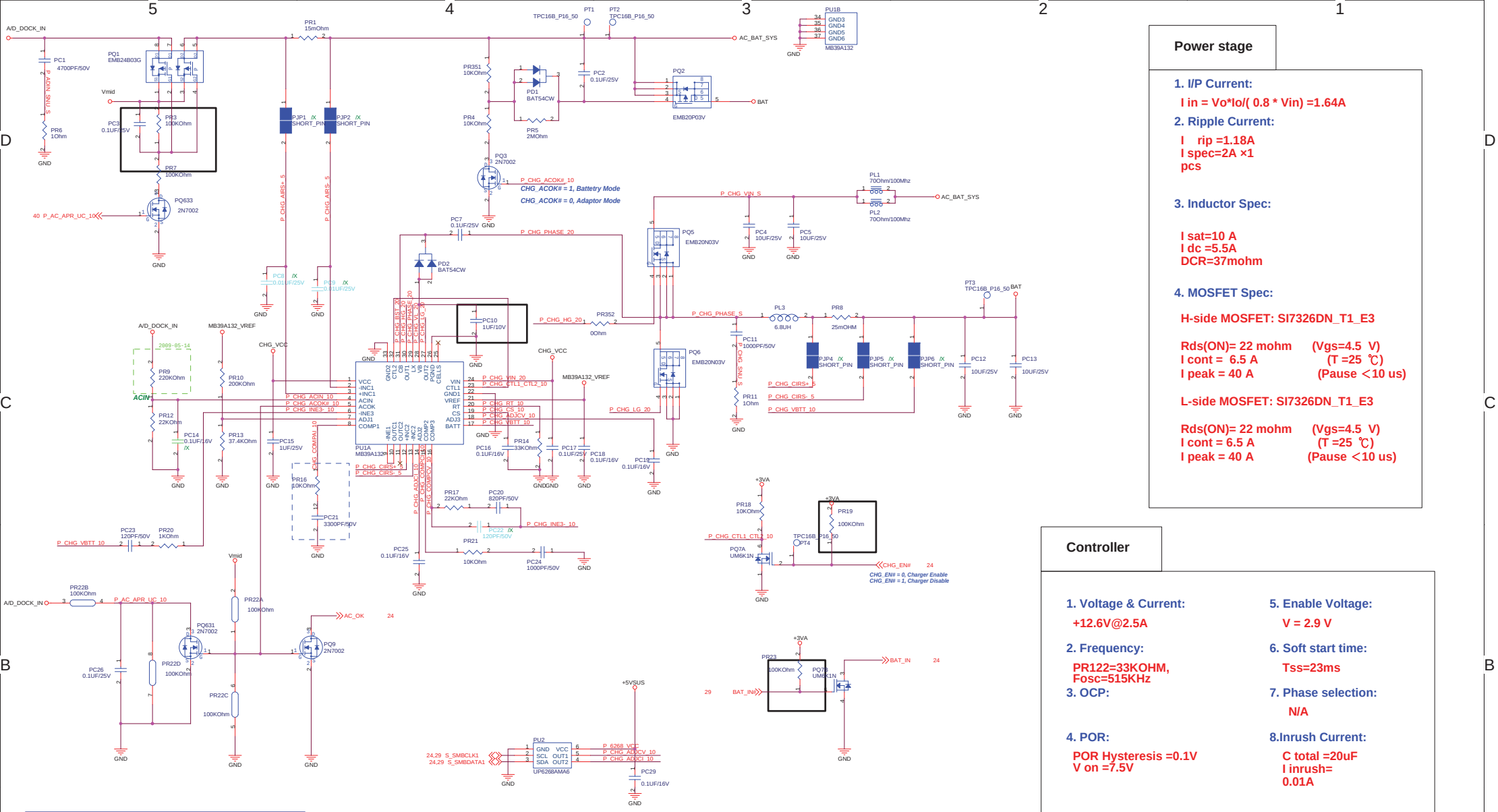
Date: Wednesday, February 24, 2010 Sheet 32 of 42



STD version :1.02G(09/12/2)

Default Group-1005P SR HIGH END

ASUSTek Computer INC	Title : POWER_FLOW	
	Engineer:	
Size: A2	Project Name: 1015P	Rev: 1.0
Date: Wednesday, February 24, 2010	Sheet 33 of 42	



Power stage

1. I/P Current:

I in = Vo*Io/(0.8 * Vin) =1.64A

2. Ripple Current:

I rip =1.18A
I spec=2A ×1 pcs

3. Inductor Spec:

I sat=10 A
I dc =5.5A
DCR=37mohm

4. MOSFET Spec:

H-side MOSFET: SI7326DN_T1_E3

Rds(ON)= 22 mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25 ℃)
I peak = 40 A (Pause ＜10 us)

L-side MOSFET: SI7326DN_T1_E3

Rds(ON)= 22 mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25 ℃)
I peak = 40 A (Pause ＜10 us)

Controller

1. Voltage & Current:

+12.6V@2.5A

2. Frequency:

PR122=33KOHM, Fosc=515KHz

3. OCP:

4. POR:

POR Hysteresis =0.1V
V on =7.5V

5. Enable Voltage:

V = 2.9 V

6. Soft start time:

Tss=23ms

7. Phase selection:

N/A

8.Inrush Current:

C total =20uF
I inrush= 0.01A

Battery Charging Current :

4.4V > Vadj2 >= 0V ==>
Ichg = (Vadj2-0.075)/(25*Rs)

BATSEL_2P# = 1, Ich=1.49A
BATSEL_2P# = 0, Ich=2.62A

Input Adaptor Max. Current Limit :

Ilimit_current = (Vadj1-0.075) / (25*Rs)=1.90A

Pre-Charging Mode :

Precharging current = 149.2mA

Vadj2 = 168mV

ACIN Threshold = 1.25V

Adaptor > 13.75V, System Powered by Adaptor

Adaptor <13.75V, System Powered by Battery

Battery Charging Voltage :

Vadj3 :VREF ==> Vbat = 4.2V /cell
3.9V>Vadj3>2.4V ==> Vbat = 4.35V/cell
Vadj3 :GND ==> Vbat = 4.0V /cell
2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell

Battery Cell Selection :

CELLS: VREF ==> 4 Cells;
CELLS: OPEN ==> 3 Cells;
CELLS: GND ==> 2 Cells;

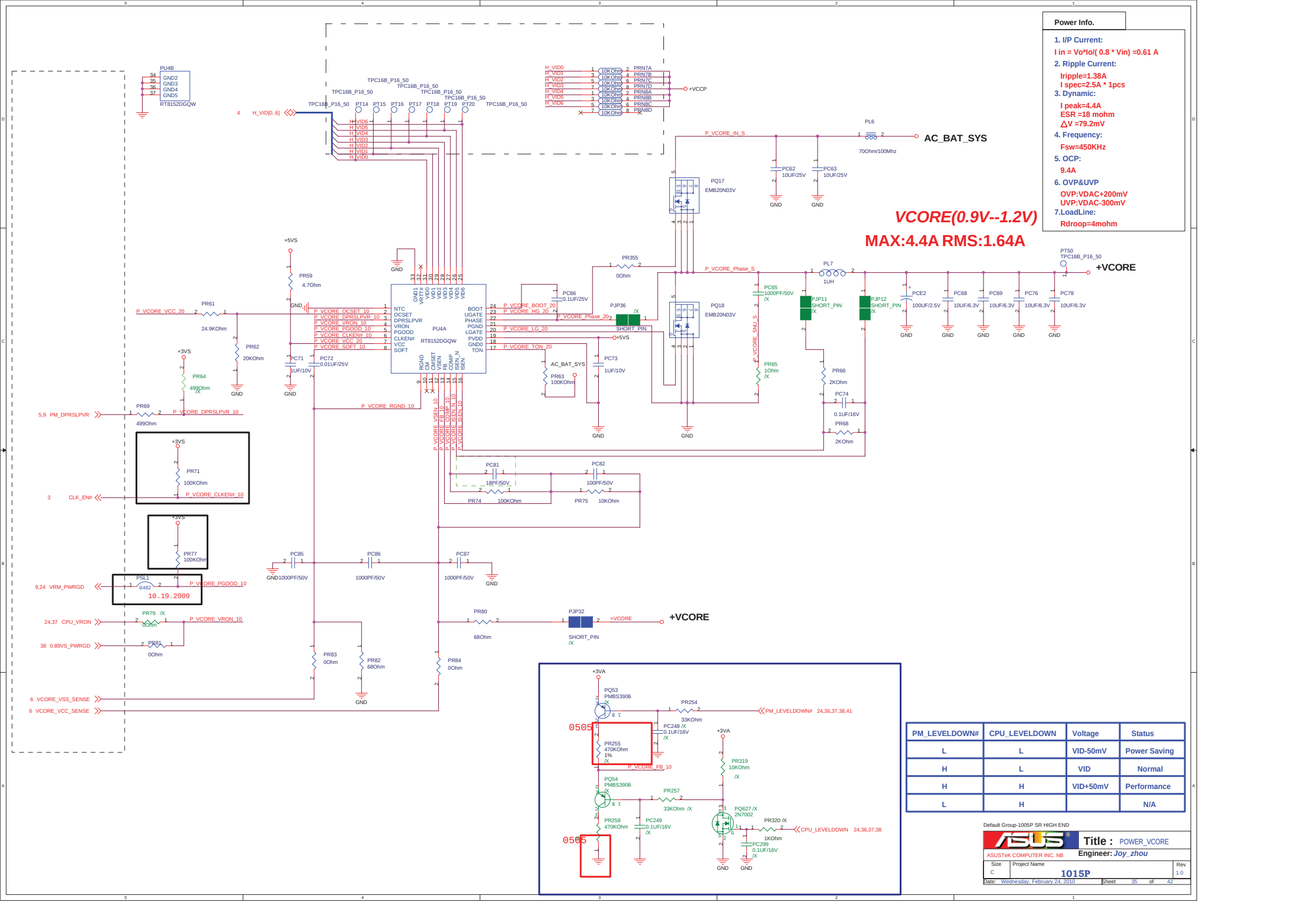
VREF = 5.0V

fosc(KHz) = 17000 / RT (KOhm)

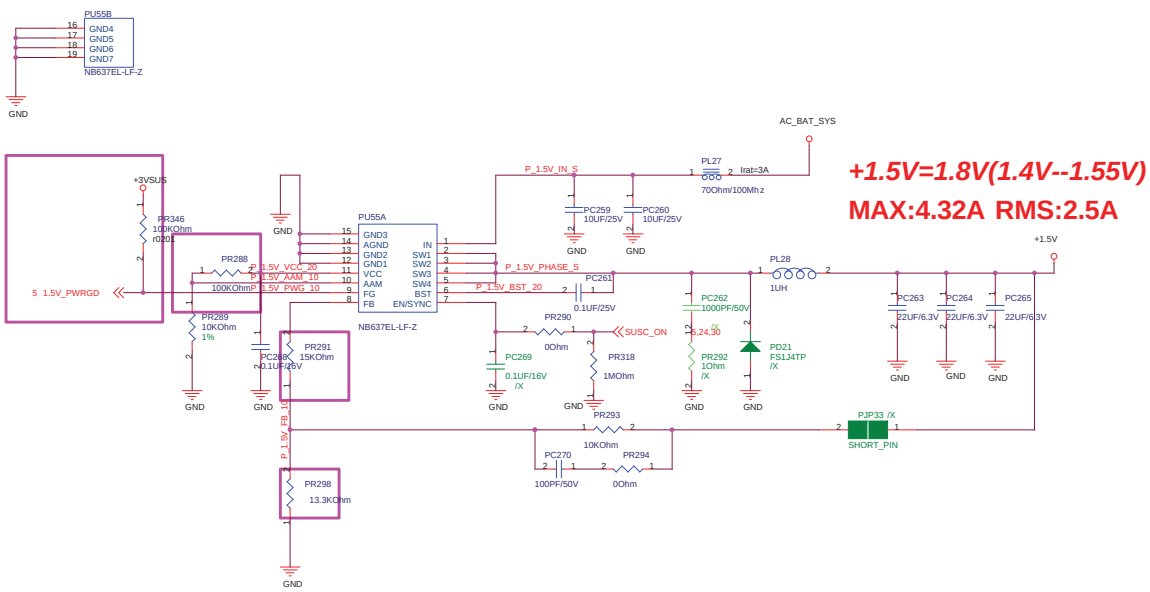
*Soft start: ts(s) = 0.13 * CS (uF)*

Default Group-1005P SR HIGH END

ASUSTek Computer INC	Title : Charger	
	Engineer: Joy_Zhou	
Size: A2	Project Name: 1008P	Rev: <RevCode>
Date: Wednesday, February 24, 2010	Sheet 34 of 42	



PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage	Status
L	L	VID-50mV	Power Saving
H	L	VID	Normal
H	H	VID+50mV	Performance
L	H		N/A



Power Info.

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.08A
2. Ripple Current:
   I rip =1A
3. Frequency:
   Fosc=600KHz
4. Current Limit:
   6A

0.9VS@1 A

1. Dropout Voltage:
   △V = 0.3V (Io = 2 A)
2. Current Limit:
   I limit = 4 A
3. Continue Current:
   I cont = 3 A
4. Power Dissipation:
   Rthjc = 52 ℃/W
   Pd = 1.9 W

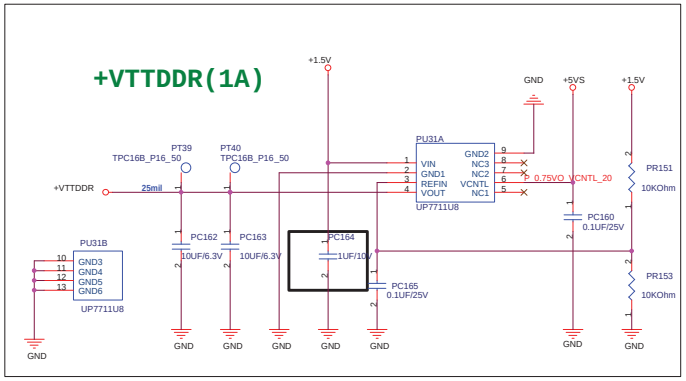
2009.11.27

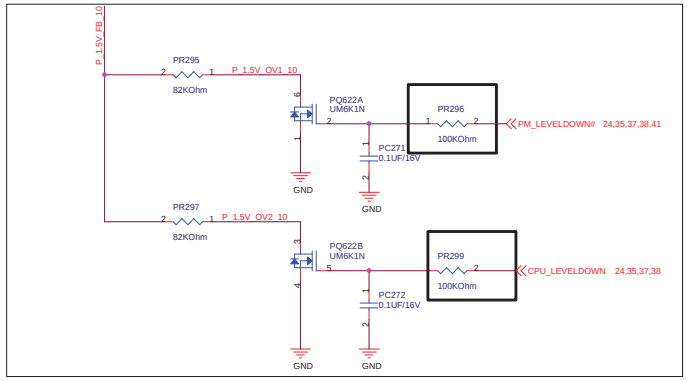
SUSC_ON 5,24,30

PM_LEVELDOWN# 24,35,37,38,41

CPU_LEVELDOWN 24,35,37,38

PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.670V	Power Saving
H	L	H	1.800V	Normal
H	H	L	1.912V	Performance
L	H	L		





Default Group-1005P SR HIGH END

ASUSTek Computer INC

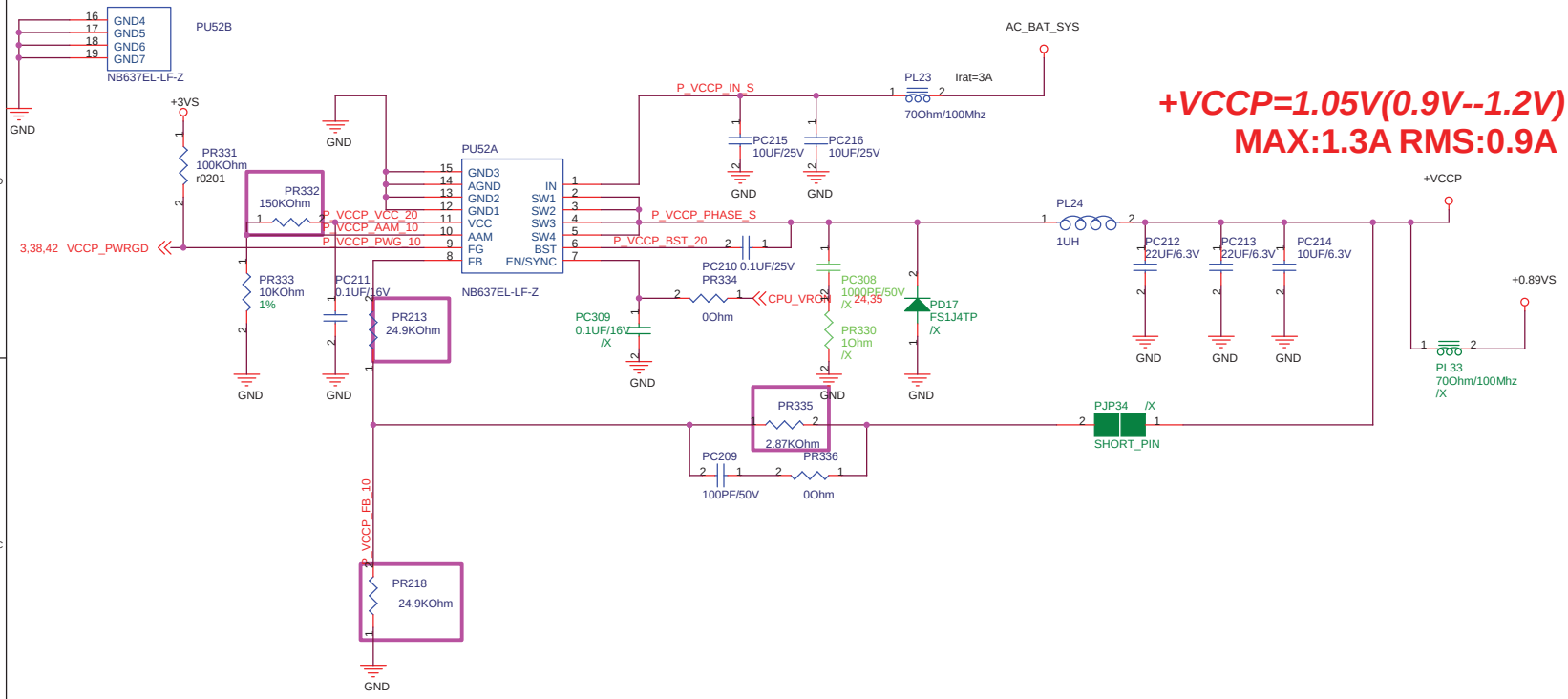
Title : +1.8V&VTTDDR

Engineer: Joy_Zhou

Size	Project Name	Rev
Custom	1015P	1.0

Date: Wednesday, February 24, 2010 Sheet 36 of 42

Power Info.



+VCCP=1.05V(0.9V--1.2V)
MAX:1.3A RMS:0.9A

1. I/P Current:

I in = Vo*Io/(0.8 * Vin) =0.7A

2. Ripple Current:

I rip =1.08A
I spec=2.5A ×1 pcs

3. Frequency:

Fosc=600KHz

4. Current Limit:

6A

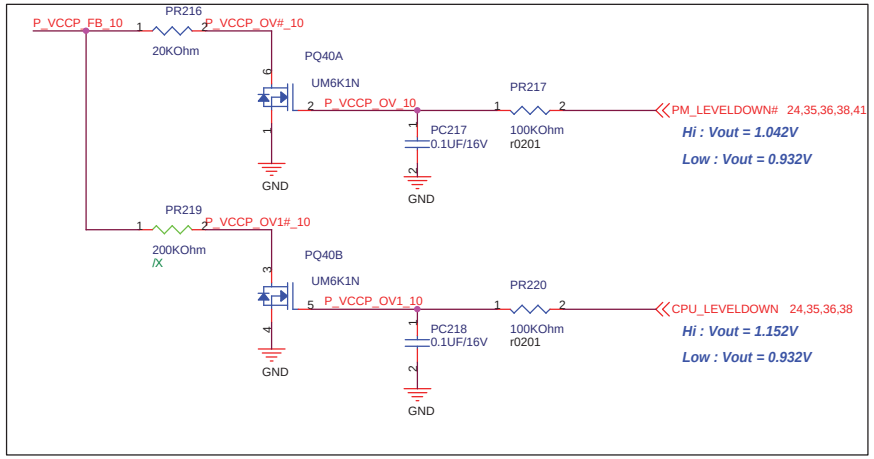
2009.11.27

CPU_VRON 24,35

PM_LEVELDOWN# 24,35,36,38,41

CPU_LEVELDOWN 24,35,36,38

PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.932V	Power Saving
H	L	H	1.042V	Normal
H	H	L	1.127V	Performance
L	H	L		N/A



Default Group-1005P SR HIGH END

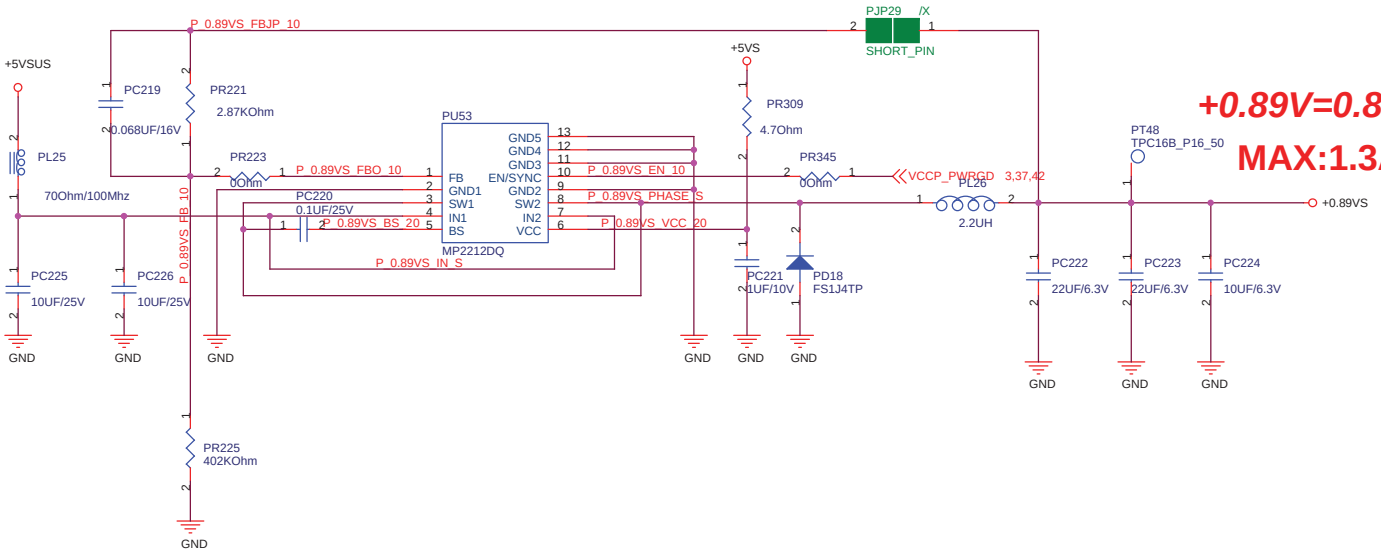
ASUSTek Computer INC

Title : +1.5VS & +2.5VS

Engineer: Joy_Zhou

Size	Project Name	Rev
A3	1015P	1.0

Date: Wednesday, February 24, 2010 Sheet 37 of 42



+0.89V=0.89V(0.844V--0.95V)

MAX:1.3A RMS:0.87A

Power Info.

1. I/P Current:

I in = Vo*Io/(0.8 * Vin) =0.36A

2. Ripple Current:

I rip =0.61A
I spec=2.5A * 1pcs

3. Dynamic:

I peak=1.6A
ESR=18 mohm
△V =28.8mV

4. Frequency:

Fosc=600KHz

5. Current Limit:

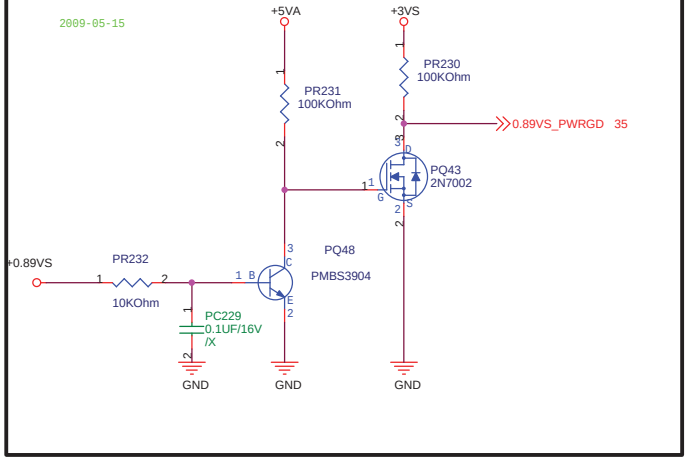
6A

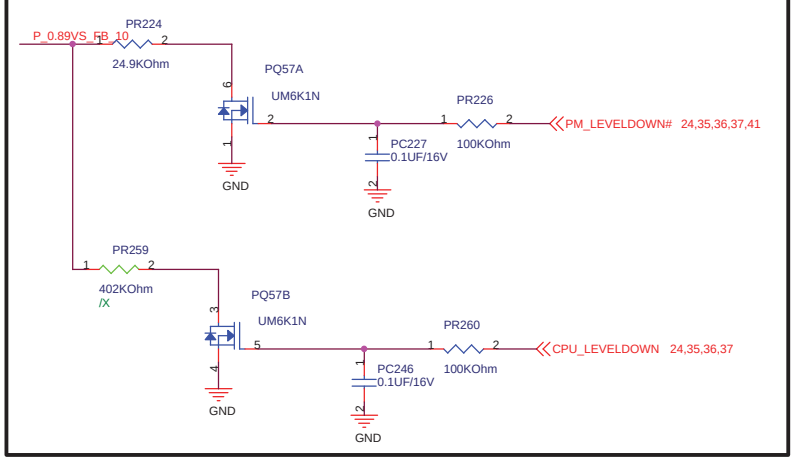
2009.11.27

VCCP_PWRGD 3,37,42

PM_LEVELDOWN# 24,35,36,37,41

CPU_LEVELDOWN 24,35,36,37





PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage	Status
L	L	0.844V	Power Saving
H	L	0.897V	Normal
H	H	0.950V	Performance
L	H		N/A

Default Group-1005P SR HIGH END

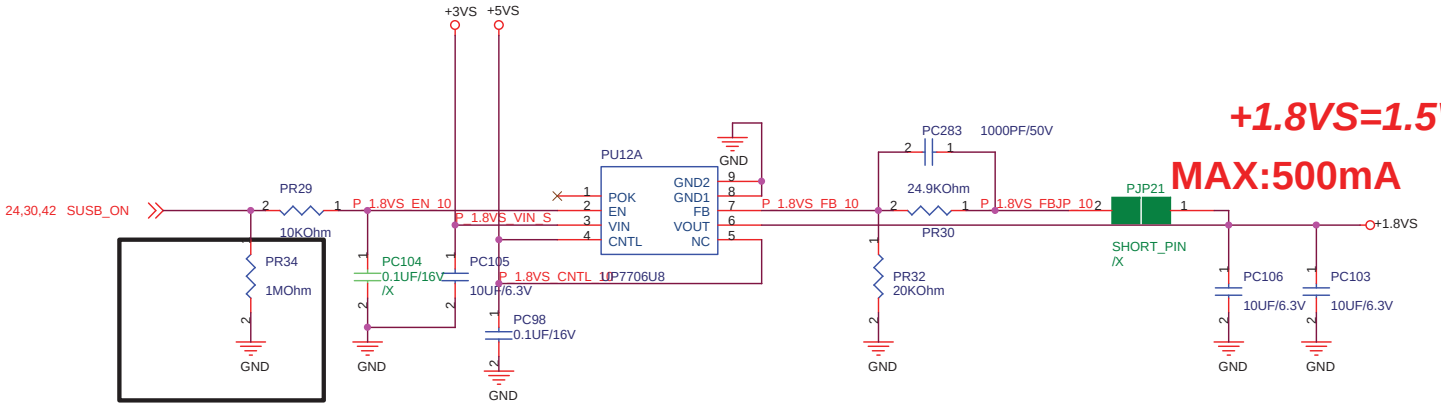
ASUSTek Computer INC

Title : +1.5VS & +2.5VS

Engineer: Joy_Zhou

Size	Project Name	Rev
A3	1015P	1.0

Date: Wednesday, February 24, 2010 Sheet 38 of 42



+1.8VS=1.5V(1.8V--1.78V)

MAX:500mA RMS:350mA

1. Dropout Voltage:

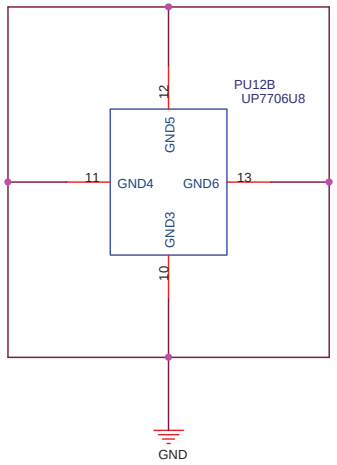
V= 300 mV (Io=2A)

2. Current Limit:

I limit= 2.8A

3. Pd:

R thjc =5 C/W
Pd =1.9W



Default Group-1005P SR HIGH END

ASUSTek Computer INC	Title : +1.5VS & +2.5VS	
	Engineer: Joy_Zhou	
Size: B	Project Name: 1015P	Rev: 1.0
Date: Wednesday, February 24, 2010	Sheet 39 of 42	

+3V_P L

Power Latch table :			
BAT	A/D_DOCK_IN		Mode
1	X	BAT /X	Latch
0	1	ADP, BAT	Out
0	0	ADP /X	Latch

RT8206

ADP_IN

BAT_IN

EC

Latch

For Power Latch

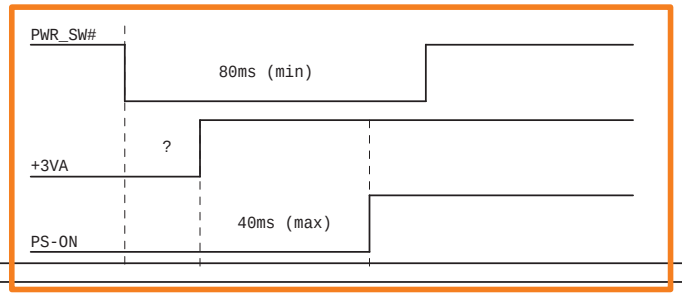
For ADP power latch

V1.3

V1.2

0-Ohm

0.22u



Default Group-1005P SR HIGH END

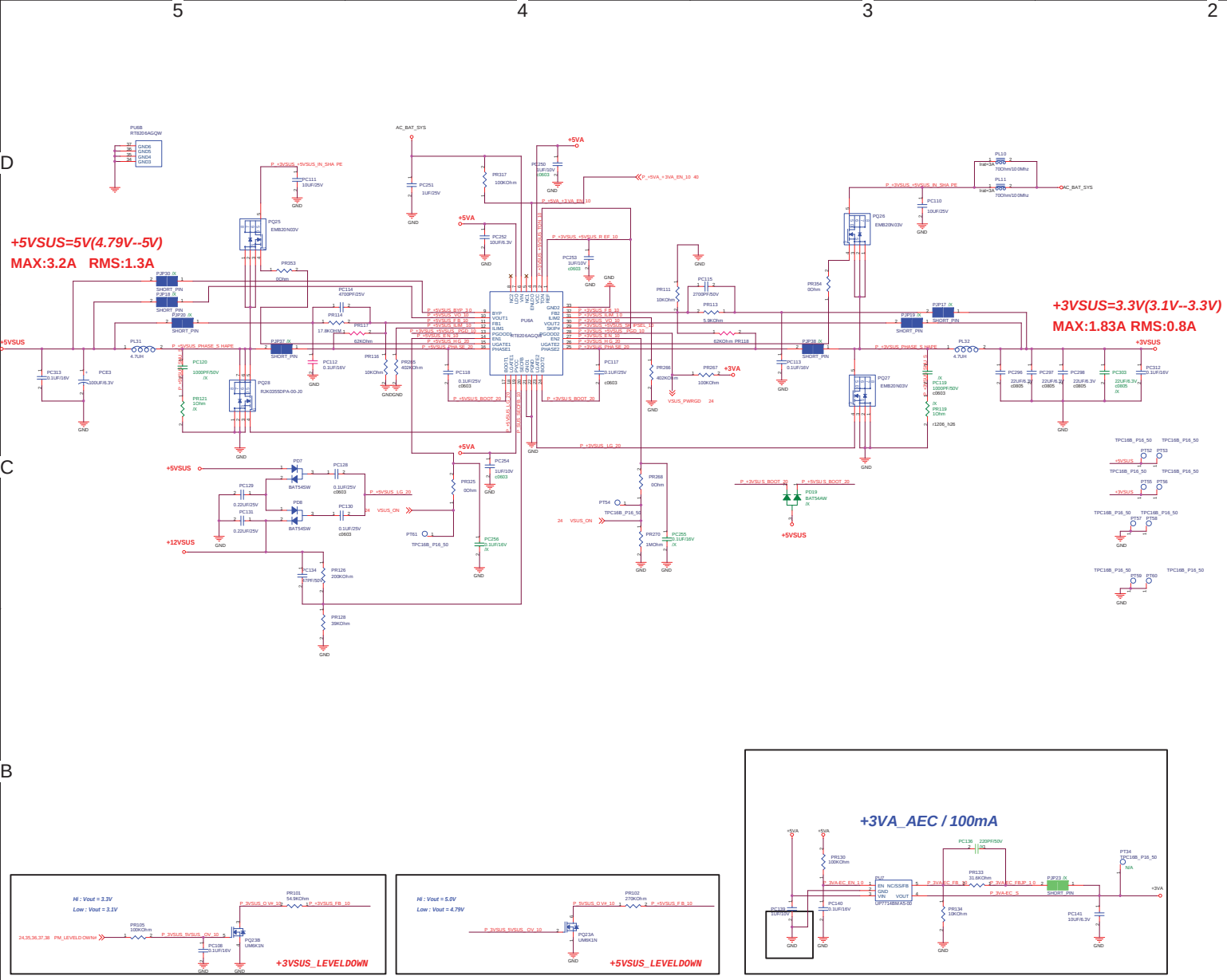
ASUSTek Computer INC.

Title : Power Latch

Engineer: River_Hsu

Size	Project Name	Rev
A4	1015P	1.0G

Date: Wednesday, February 24, 2010 Sheet 40 of 42



Power Info. +5VSUS

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =2.082A
2. Ripple Current:
   I rip =1.482A
   I spec=2.5A ×1 pcs
3. Frequency:
   fosc=300KHz
4. OCP:
   Iocp=17A

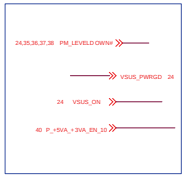
Power Info. +3VSUS

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.832A
2. Ripple Current:
   I rip =1.92A
   I spec=2.5A ×1 pcs
3. Frequency:
   fosc=375KHz
4. OCP:
   Iocp=8.74A

Power Info. +3VA

1. Dropout Voltage:
   ΔV= 210mV (Io=300m A)
2. Current Limit:
   I limit= 480mA
3. Pd:
   R thjc =5 C/W
   Pd =0.4W

2009.11.23



Default Group-1005P SR HIGH END

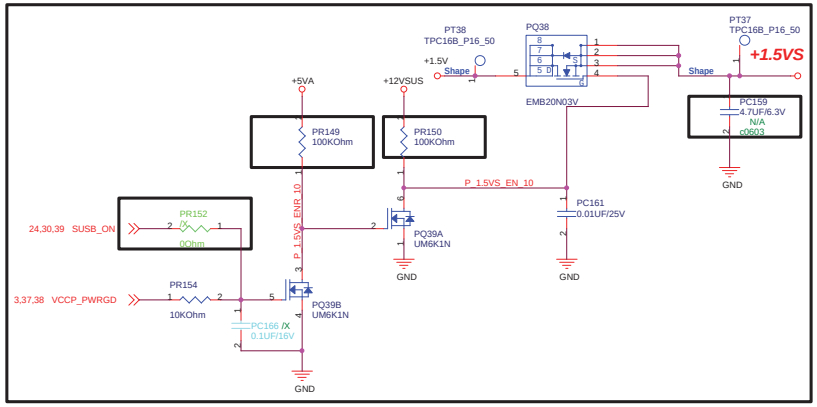
ASUSTek Computer INC.

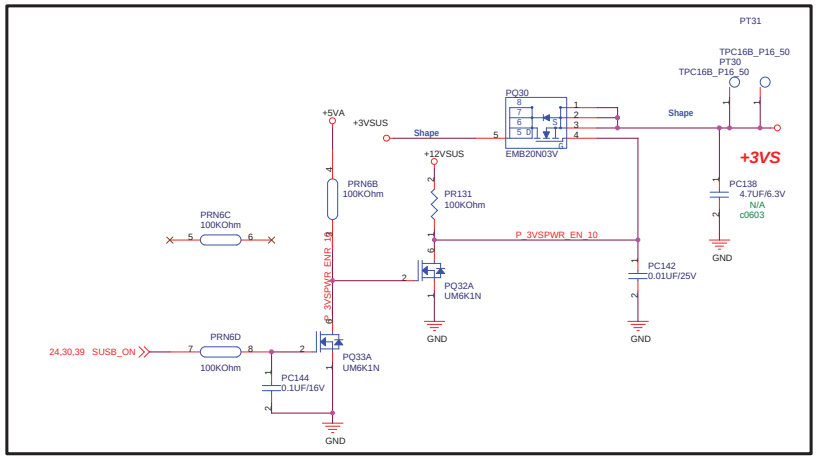
Title : +5VSUS&+12VSUS

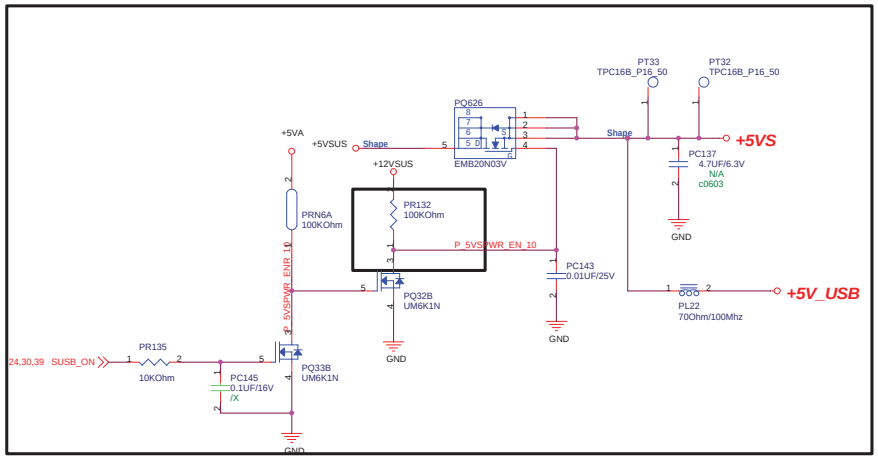
Engineer: Joy_Zhou

Size	Project Name	Rev
A1	1015P	1.0

Date: Wednesday, February 24, 2010 Sheet 41 of 42







2009.11.27

SUSB_ON 24,30,39

VCCP_PWRGD 3,37,38

Default Group-1005P SR HIGH END

ASUSTek Computer INC

Title : load switch

Engineer: Joy_Zhou

Size	Project Name	Rev
C	1015P	1.0

Date: Wednesday, February 24, 2010 Sheet 42 of 42

www.s-manuals.com