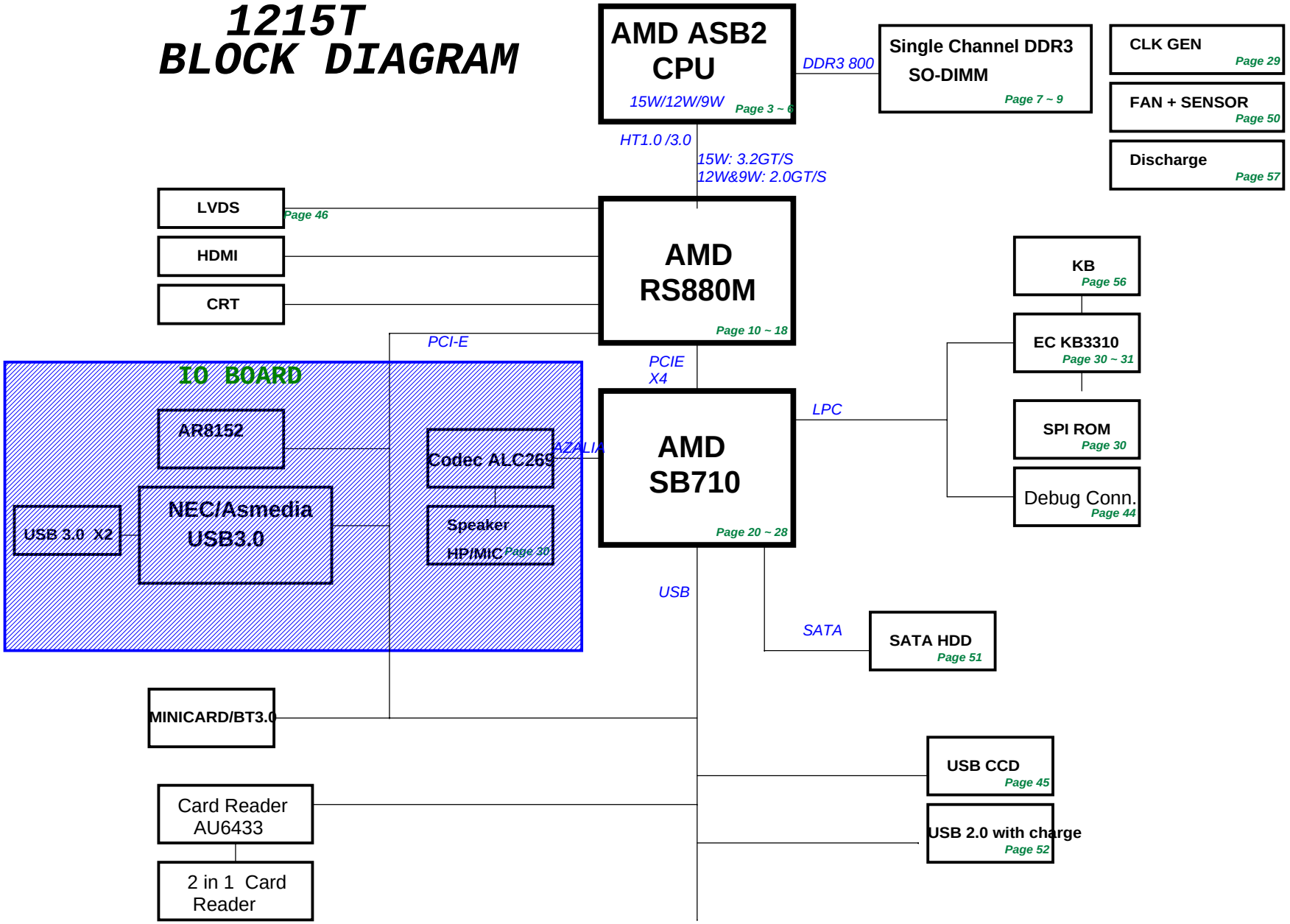
1215T BLOCK DIAGRAM



<Variant Name>

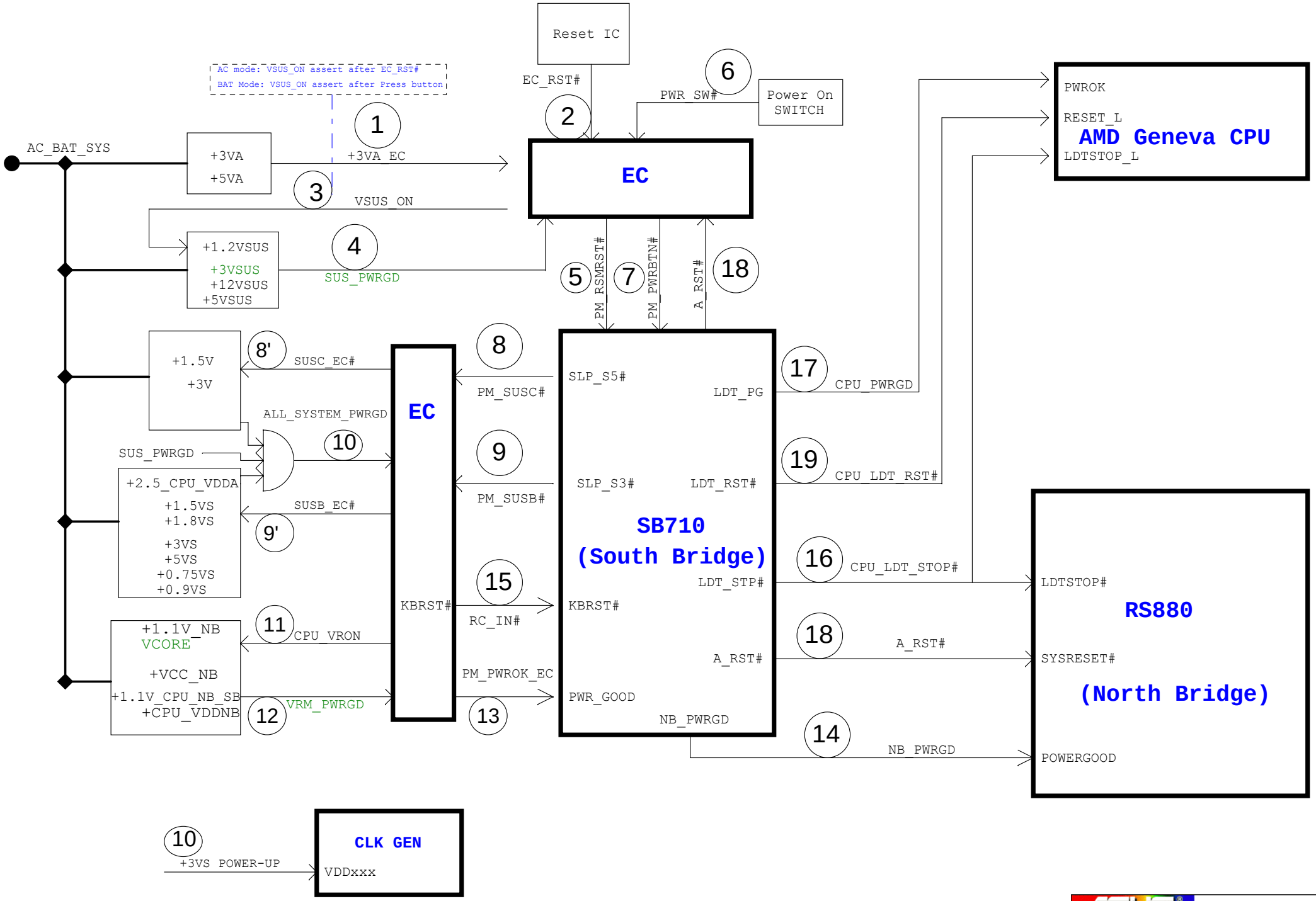
ASUSTeK Computer INC

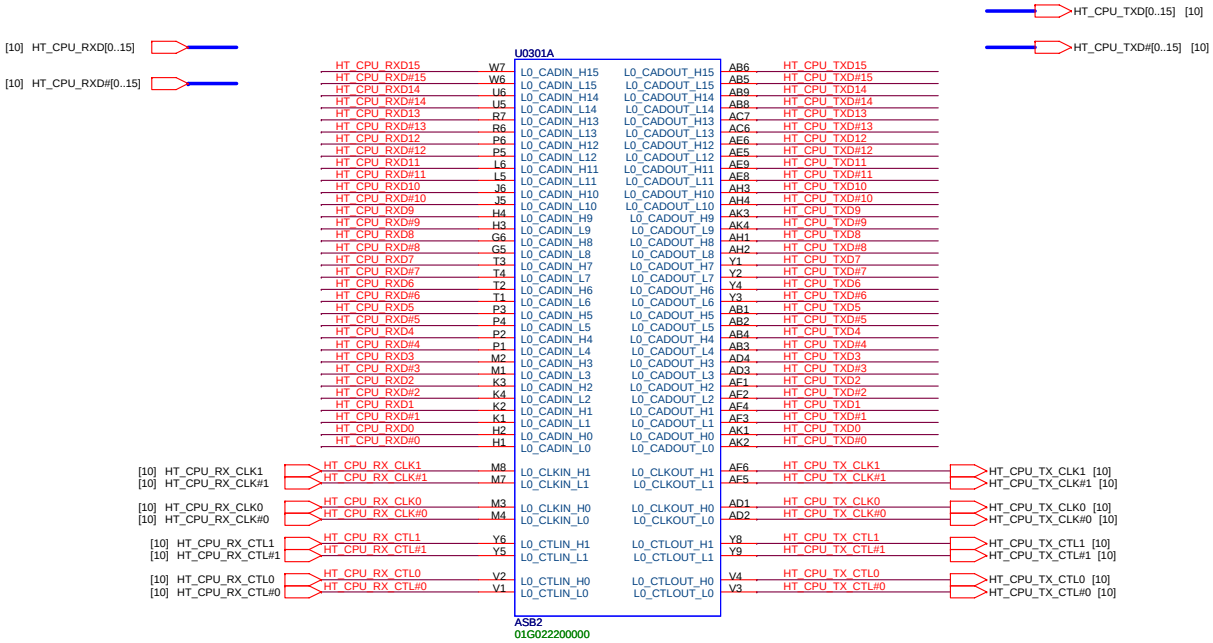
Title : Block Diagram

Engineer: N/A

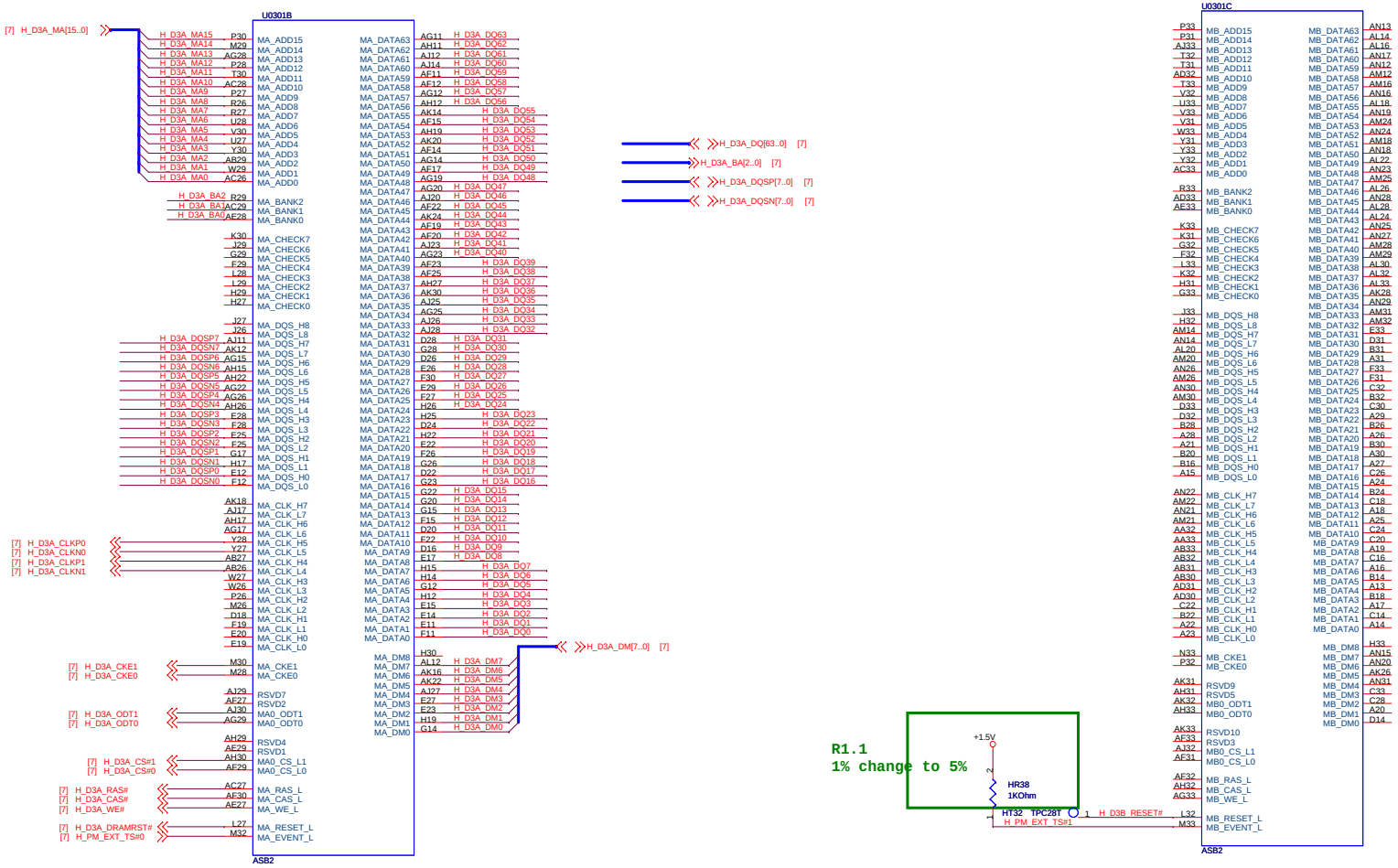
Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 1 of 80


Reset IC
AC mode: VSUS_ON assert after EC_RST#
BAT Mode: VSUS_ON assert after Press button
EC_RST#
PWR_SW#
Power On SWITCH
AC_BAT_SYS
+3VA
+5VA
+3VA_EC
VSUS_ON
EC
PWROK
RESET_L
AMD Geneva CPU
LDTSTOP_L
+1.2VSUS
+3VSUS
+12VSUS
+5VSUS
SUS_PWRGD
PM_RSMRST#
PM_PWRBTN#
A_RST#
+1.5V
+3V
SUSC_EC#
PM_SUSC#
SLP_S5#
LDT_PG
CPU_PWRGD
ALL_SYSTEM_PWRGD
SUS_PWRGD
+2.5_CPU_VDDA
+1.5VS
+1.8VS
+3VS
+5VS
+0.75VS
+0.9VS
SUSB_EC#
PM_SUSB#
SLP_S3#
LDT_RST#
CPU_LDT_RST#
SB710
(South Bridge)
LDT_STP#
CPU_LDT_STOP#
LDTSTOP#
RS880
KBRST#
RC_IN#
KBRST#
+1.1V_NB
VCORE
+VCC_NB
+1.1V_CPU_NB_SB
+CPU_VDDNB
CPU_VRON
A_RST#
SYSRESET#
(North Bridge)
PM_PWROK_EC
VRM_PWRGD
PWR_GOOD
NB_PWRGD
NB_PWRGD
POWERGOOD
+3VS POWER-UP
CLK GEN
VDDxxx
Title : Power sequence
ASUSTeK.Computer.INC
Engineer: N/A
Size Custom
Project Name 1215T
Rev 1.0
Date: Tuesday, August 10, 2010
Sheet 2 of 80



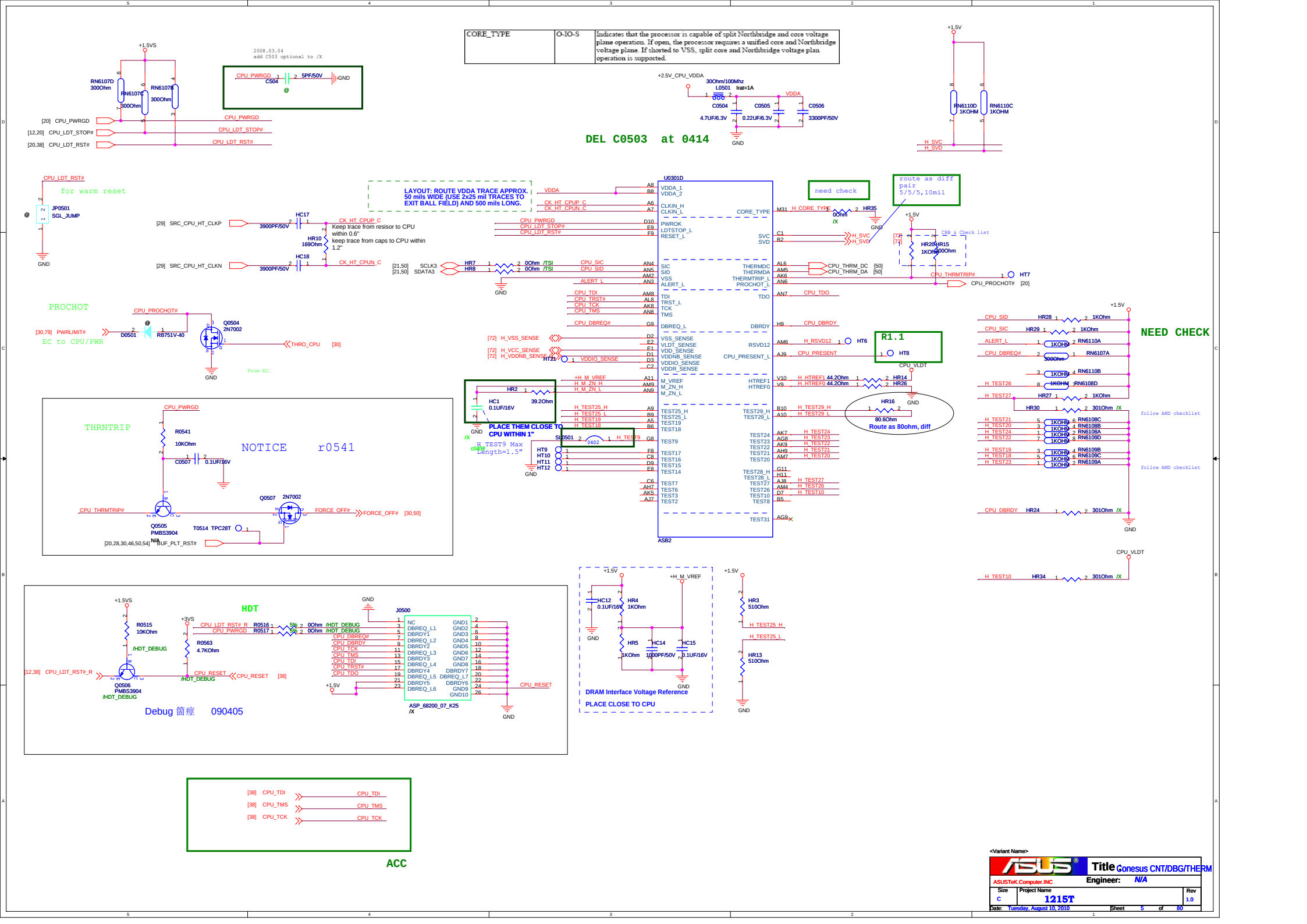
ASUSTeK.Computer.INC	Title : Conesus HT I/F	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 3 of 80	



Change list:

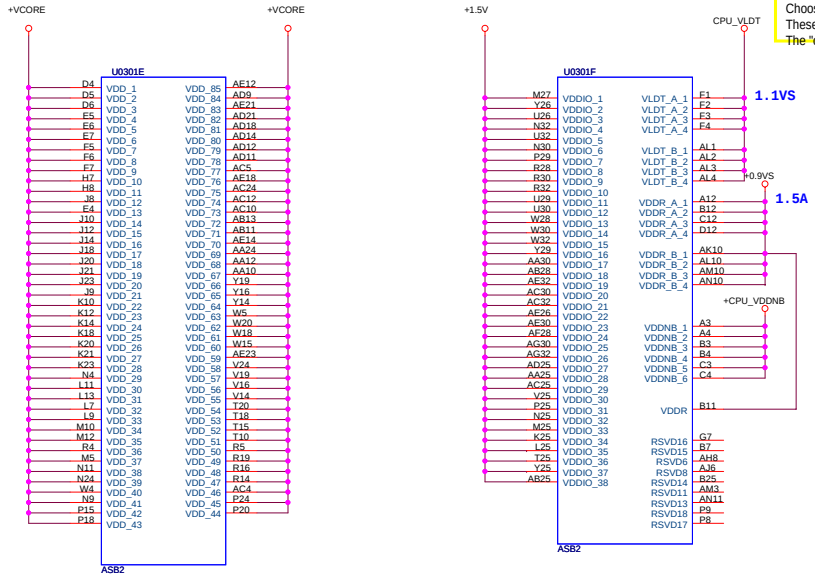
1、CLK 0 and 1 reserved follow AMD Schematic check list。

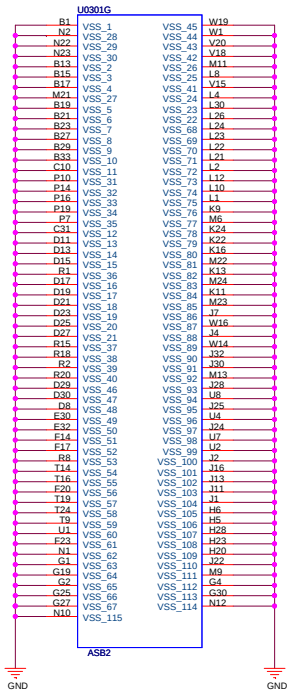
ASUSTeK.Computer.INC	Title : Conesus DDR2 MEM I/F		
	Engineer: N/A		
Size: C	Project Name: 1215T		Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 4 of 80		

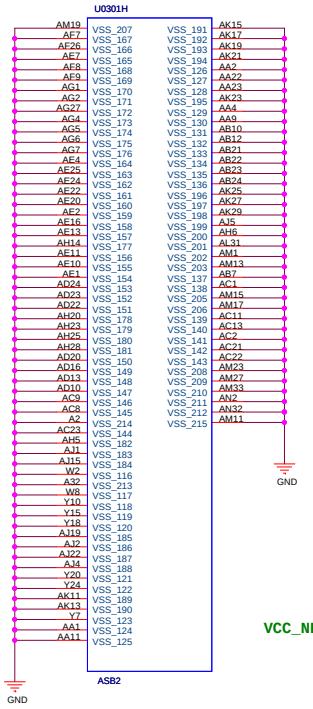


CORE_TYPE
O-IO-S
Indicates that the processor is capable of split Northbridge and core voltage plane operation. If open, the processor requires a unified core and Northbridge voltage plane. If shorted to VSS, split core and Northbridge voltage plan operation is supported.
DEL C0503 at 0414
2008.03.04
add C503 optional to /X
for warm reset
LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.
need check
route as diff pair 5/5/5,10mil
CRB & Check list
PROCHOT
EC to CPU/PWR
From EC.
R1.1
Route as 80ohm, diff
PLACE THEM CLOSE TO CPU WITHIN 1"
H_TEST9 Max Length=1.5"
NEED CHECK
follow AMD checklist
THRNTRIP
NOTICE r0541
HDT
Debug 箇痙 090405
DRAM Interface Voltage Reference
PLACE CLOSE TO CPU
ACC
<Variant Name>
Title Conesus CNT/DBG/THERM
ASUSTeK.Computer.INC
Engineer: N/A
Size C
Project Name 1215T
Rev 1.0
Date: Tuesday, August 10, 2010
Sheet 5 of 80

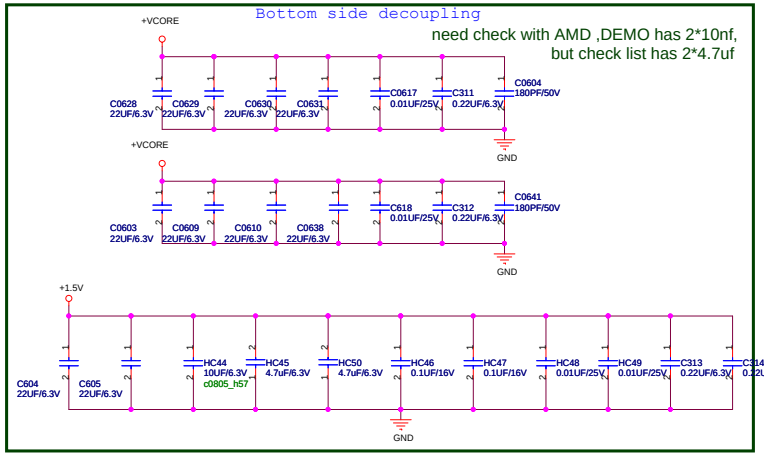
DESIGN NOTE:
VLDT must be routed as a pour or a trace at least 200 mils wide.
VLDT may be routed from the source to either ALx balls or Fx balls.
Choose whichever makes routing simpler.
These six capacitors must be placed very near the selected balls.
The "other" set of balls must be decoupled with a 4.7uF cap.

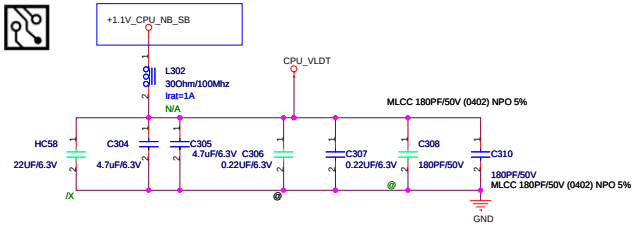






VCC_NB should not ramp before 1.1v





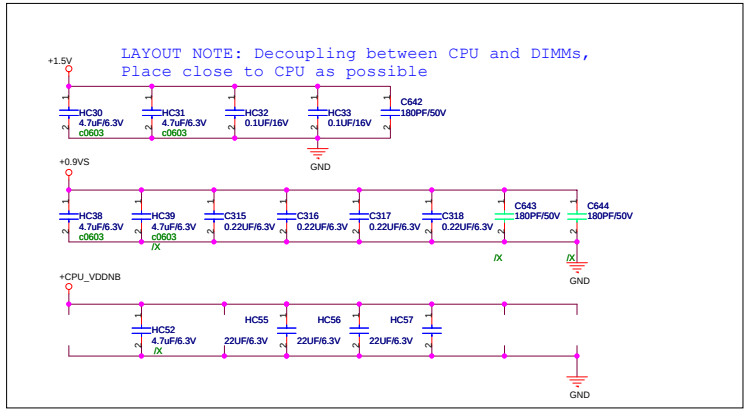
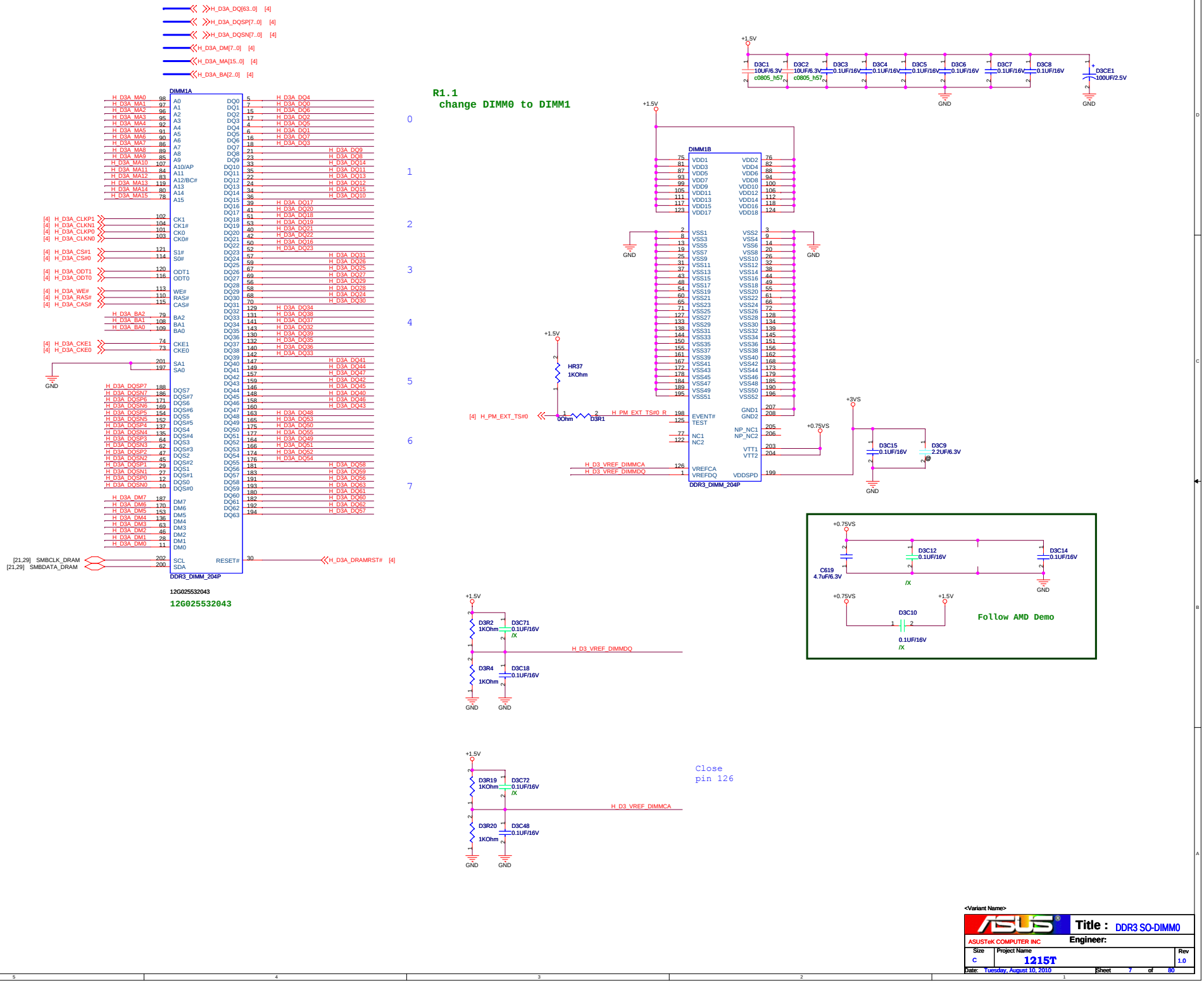


Table 6. Power Supply/Voltage Regulator Interface Pin Descriptions

Signal Name	Type	Description
PSI_L	O-IO-S	Power Status Indicator for the VDD Power Supply regulator. This signal may be used by the regulator to improve efficiency when the processor is in low power states.
VDD	S	Core power supply
VDD_SENSE	A	VDD voltage monitor pin
VDDNB	S	Northbridge power supply
VDDNB_SENSE	A	VDDNB voltage monitor pin
VDDIO	S	DDR SDRAM I/O ring power supply
VDDIO_SENSE	A	VDDIO voltage monitor pin
VDDA	S	Filtered PLL Supply Voltage
VDDR_A, VDDR_B	S	VDDR regulator voltage
VDDR_SENSE	A	VDDR voltage monitor pin
VLDT_A,VLDT_B	S	HyperTransport™ I/O ring power supplies
VLDT_SENSE	A	VLDT voltage monitor pin
VSS	S	Ground
VSS_SENSE	A	VSS voltage monitor pin
SVC	O-IO-S	Serial VID interface clock
SVD	B-IO-OD	Serial VID interface data

ASUSTeK.Computer.INC	Title : Conesus Power		
	Engineer: N/A		
Size: C	Project Name: 1215T		Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 6 of 80		


H_D3A_DQ[63..0] [4]
H_D3A_DQSP[7..0] [4]
H_D3A_DQSN[7..0] [4]
H_D3A_DM[7..0] [4]
H_D3A_MA[15..0] [4]
H_D3A_BA[2..0] [4]
DIMM1A
DDR3_DIMM_204P
R1.1
change DIMM0 to DIMM1
12G025532043
126025532043
DIMM1B
DDR3_DIMM_204P
HR37
1KOhm
0Ohm
D3R1
H_PM_EXT_TS#0
H_PM_EXT_TS#0_R
H_D3_VREF_DIMMCA
H_D3_VREF_DIMMDQ
D3C1
D3C2
D3C3
D3C4
D3C5
D3C6
D3C7
D3C8
D3CE1
D3C15
D3C9
D3C12
D3C14
C619
4.7uF/6.3V
D3C10
Follow AMD Demo
D3R2
D3C71
D3R4
D3C18
D3R19
D3C72
D3R20
D3C48
Close
pin 126
<Variant Name>
Title : DDR3 SO-DIMM0
ASUSTeK COMPUTER INC
Engineer:
Size C
Project Name 1215T
Rev 1.0
Date: Tuesday, August 10, 2010
Sheet 7 of 80

<Variant Name>

Title : DDR2 SO-DIMM1

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 8 of 80

Title : DDR2_TERMINATIONS

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 9 of 80



Signal	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R

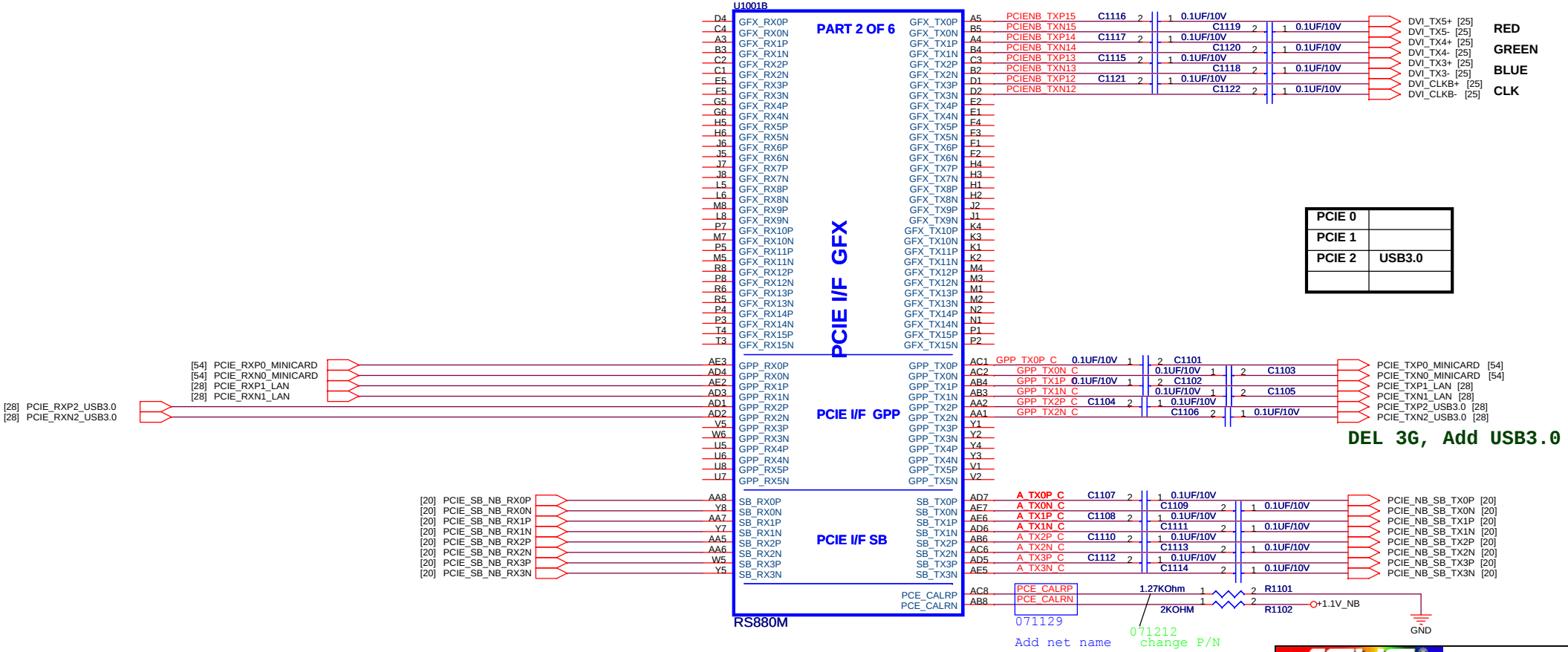
ASUSTeK.Computer.INC

Title : RS780M-HT LINK I/F

Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 10 of 80



PCIE 0	
PCIE 1	
PCIE 2	USB3.0

ASUSTeK.Computer.INC

Title : RS780M-PCIE LINK I/F

Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 11 of 80

notice L1201 L1204 change SL?
090411

09.7.14

090407

080201 R1.1
Change to +1.1V_NB
form NB_VDD_MUX

R1.1 ADD C1210

R2.0080401
Change NB_ALLOW_LDTSTOP to ALLOW_LDTSTOP

R1.11
080310

STRP_DATA	0	1
VCC_NB	1.0V	1.1V

for HDMI

for HDMI

R1.2 for AMD review

R2.0 change R1210 to1K

071218
for measurement near U1001

DEL serial R

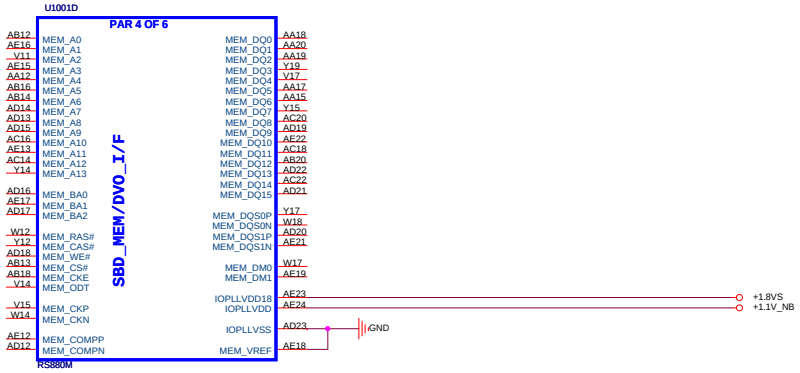
for external graphic?
NEED CHECK

100M FOR ALINK
NEED CHECK

071115

071116

Title :	RS780M-SYS I/F
ASUSTeK.Computer.INC	Engineer: N/A
Size: C	Project Name: 1215T
Rev: 1.0	
Date: Tuesday, August 10, 2010	Sheet 12 of 80



DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS780:SUS_STAT
```

STRAP_DEBUG_BUS_PCIE_ENABLE

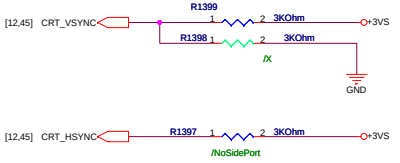
```
Enables the Test Debug Bus using PCIE bus:
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable


RS780: configurable thru register setting only
```

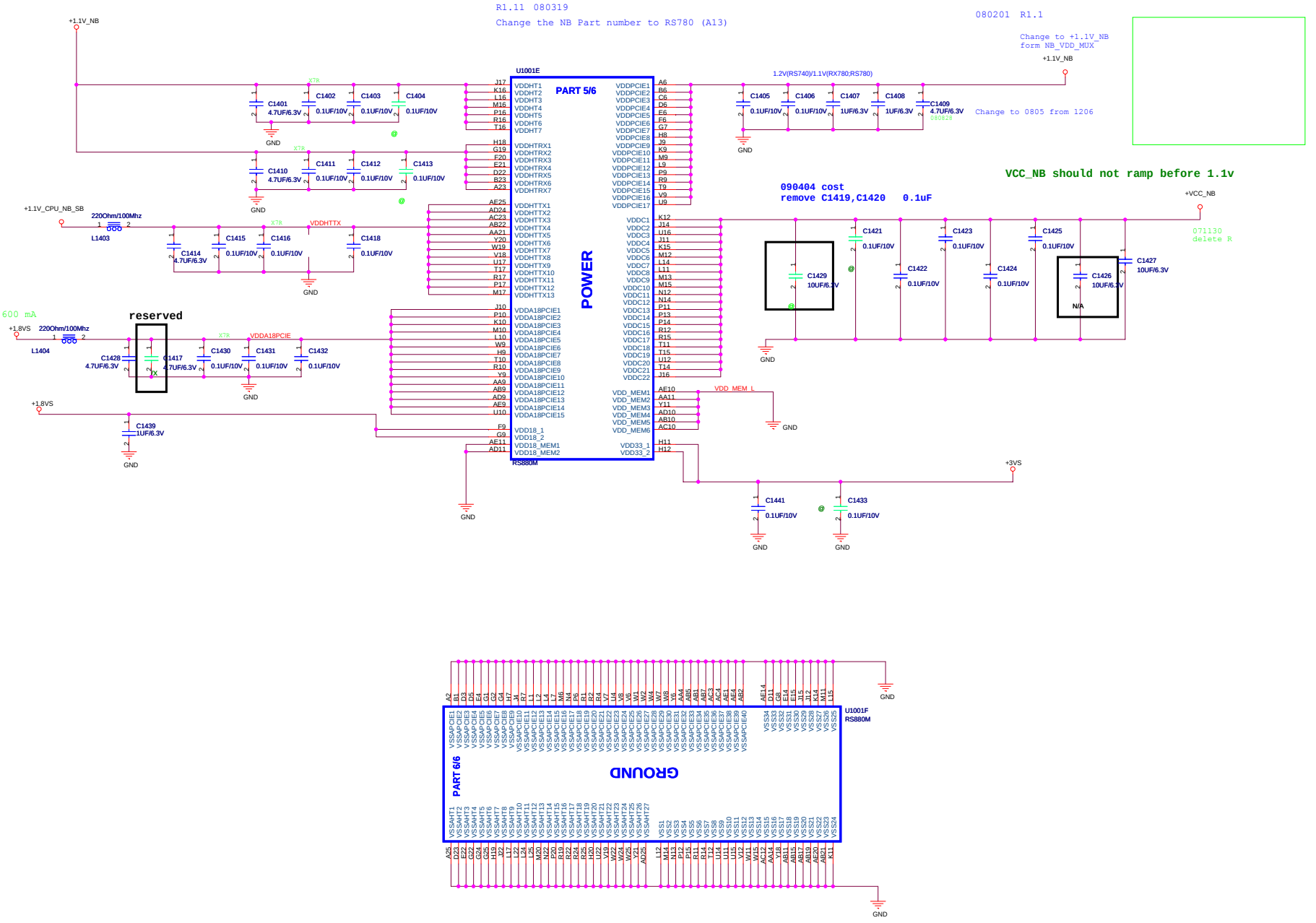
RS740/RS780: Enables Side port memory

```
RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
```

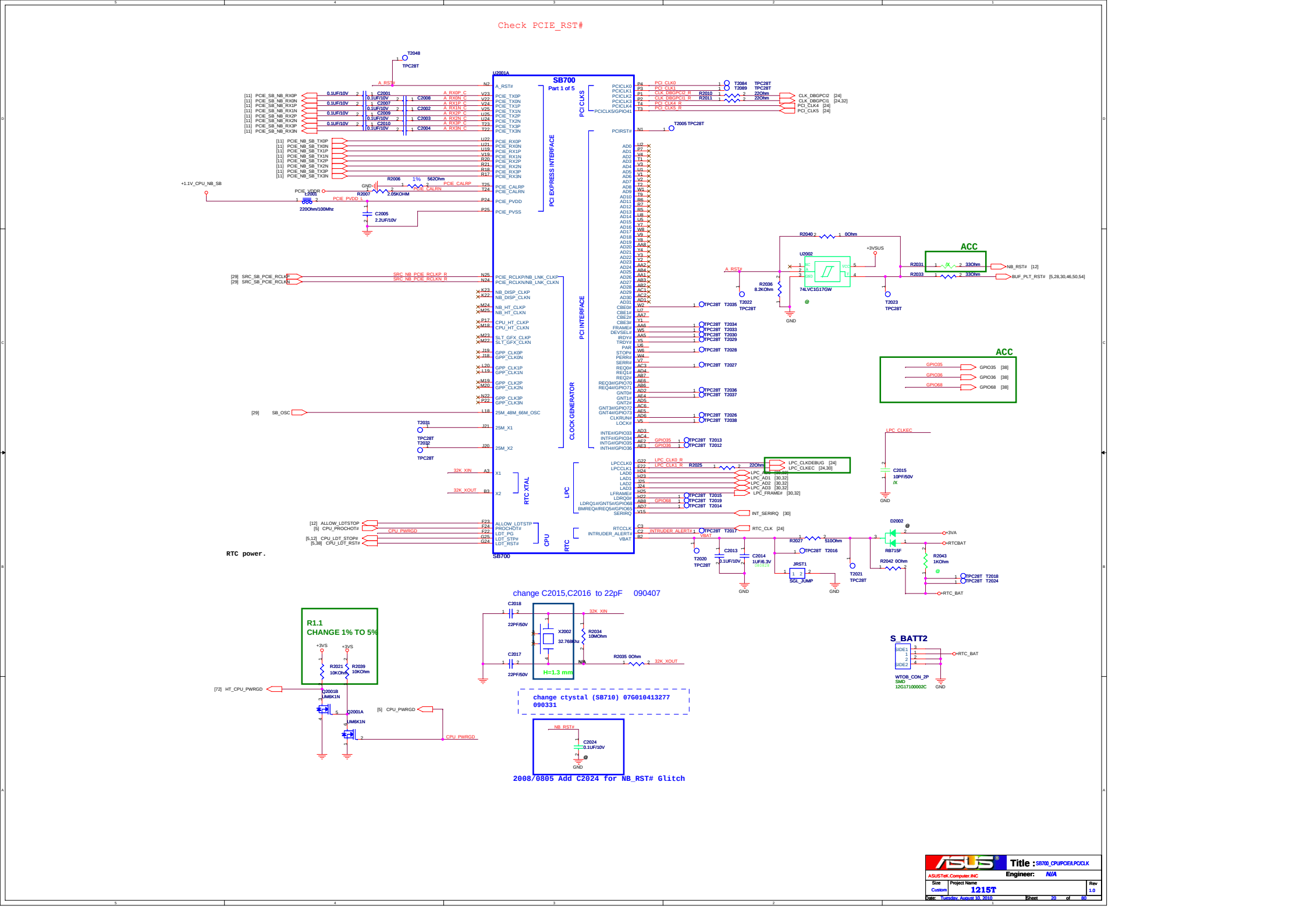


ASUSTeK.Computer.INC	Title : RS780M-SPMEM/STRAP	
	Engineer: N/A	
Size: C	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 13 of 80	



ASUSTeK.COMPUTER.INC	Title : RS780M-POWER		
	Engineer: N/A		
Size: C	Project Name: 1215T		Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 14 of 80		

Check PCIE_RST#



ASUSTeK.Computer.INC	Title : SB700_CPUPCIE/LPCCLK		
	Engineer: N/A		
Size: Custom	Project Name: 1215T		Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 20 of 80		

R1.11 080319
Change the SB Part number to SB700 (A12)

071129
Add net name

R1.1

USB 0	External USB
USB 1	External USB
USB 2	
USB 3	
USB 4	
USB 5	
USB 6	Card reader
USB 7	
USB 8	CAMERA
USB 9	
USB 10	
USB 11	WLAN(MiniCard)
USB 12	
USB 13	
USB 14	
USB 15	

071207
RS780 POWERGOOD is 1.8VS rail

09.7.13

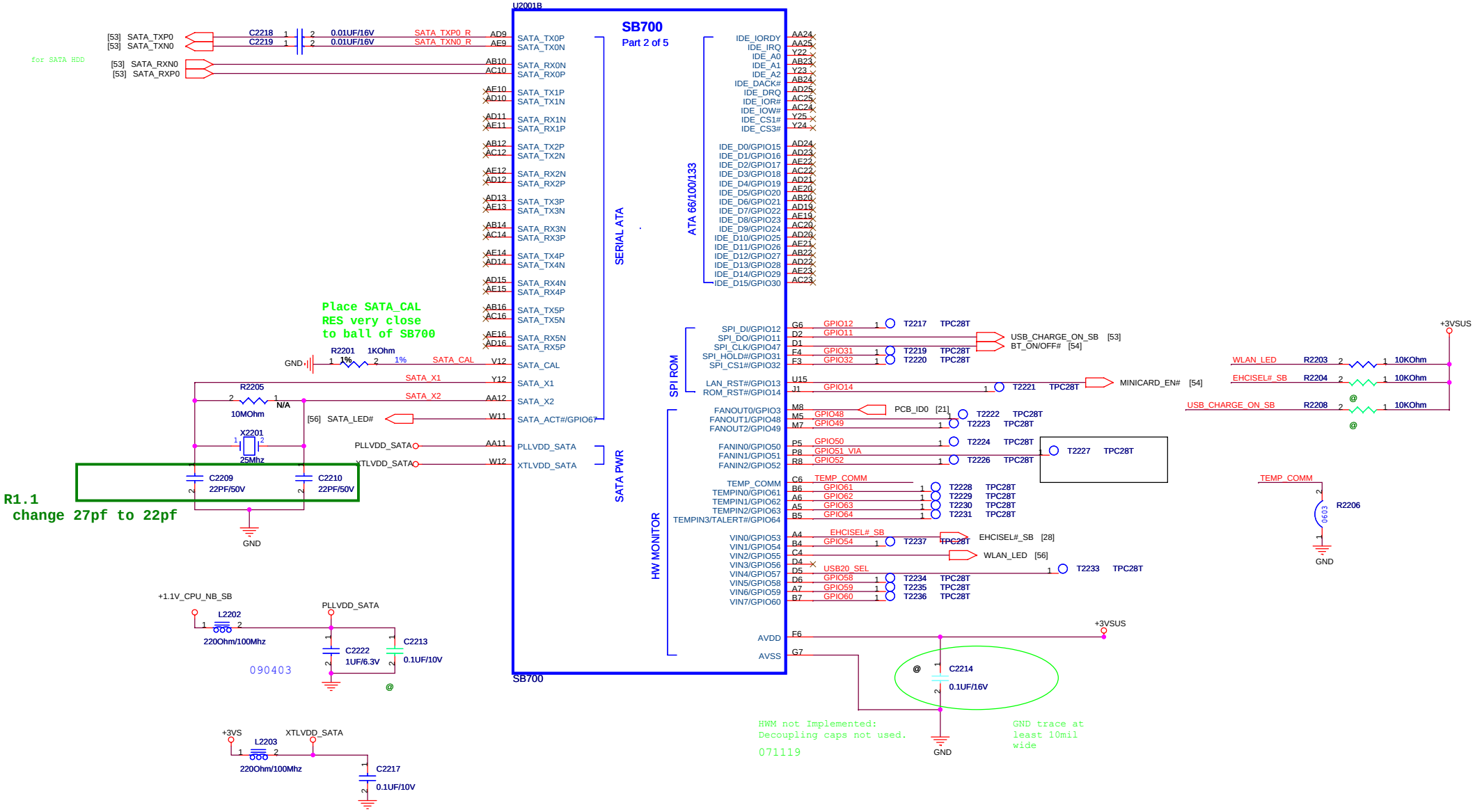
EMI 100411

R1.1 EMI
R2123 33 ohm change to 39 ohm
C2148 22pf change to 33pf,mount

SB700A11 EC enable Strap Workaround

Title :	SB700_GPIO/USB/HDI/ACPI	
ASUSTeK.Computer.INC	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 21 of 80	

Change the SB Part number to SB710 (A14)



<Variant Name>

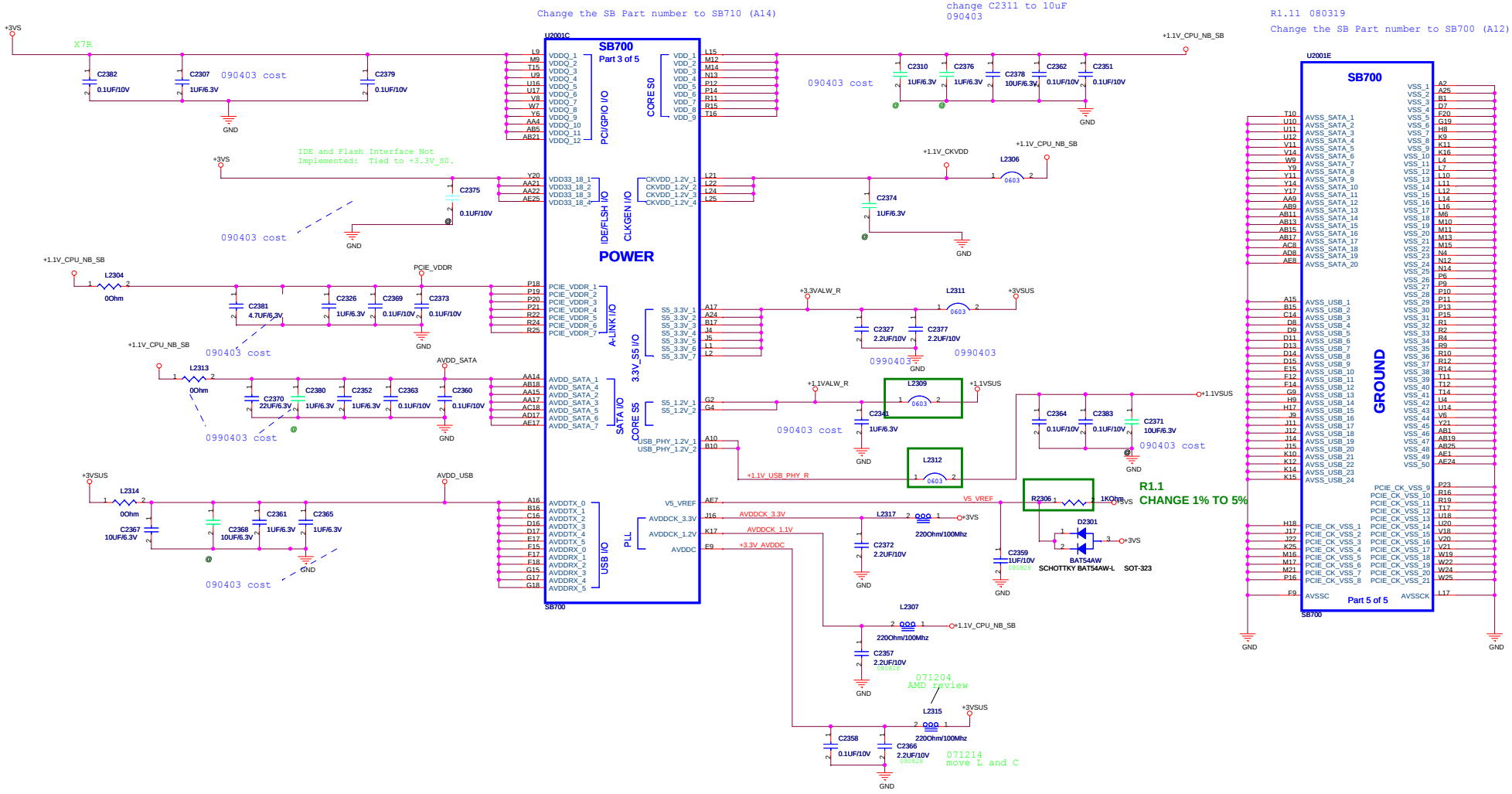
Title : SB700_PATA/SATA

ASUSTeK.Computer.INC

Engineer: N/A

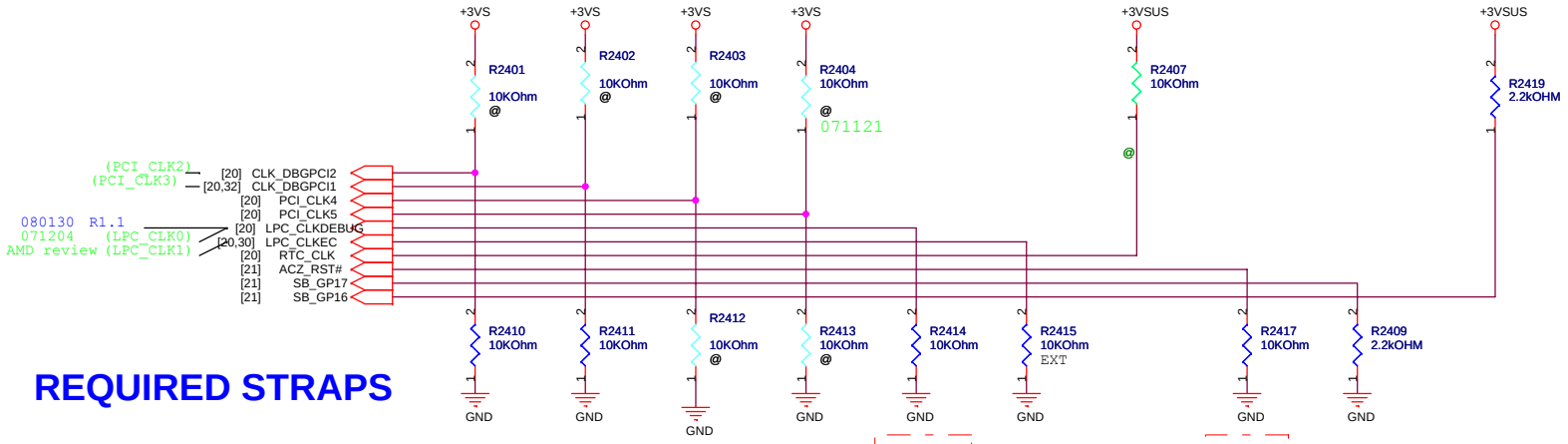
Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 22 of 80


Change the SB Part number to SB710 (A14)
change C2311 to 10uF
090403
R1.11 080319
Change the SB Part number to SB700 (A12)
SB700
Part 3 of 5
POWER
GROUND
Part 5 of 5
IDE and Flash Interface Not Implemented: Tied to +3.3V_S0.
090403 cost
0990403
R1.1
CHANGE 1% TO 5%
071204
AMD review
071214
move L and C
ASUSTeK.Computer.INC
Title : SB700_POWER
Engineer: N/A
Project Name 1215T
Rev 1.0
Tuesday, August 10, 2010
Sheet 23 of 80

Remove R2405, R2406,R2416
R2408, R2418, R2420, R2418 090405

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI MEM BOOT	H,H = Reserved H,L = SPI ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

For SB700 A12 and later version

080204 R1.1
Change the Text Comment

<Variant Name>

ASUSTeK.Computer.INC	Title : SB700_STRAP	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 24 of 80	

Close to HDMI CON(ESD Protection)

IP4284CZ10-TB

DVI_TX5- MB
DVI_TX5+ MB
DVI_TX4- MB
DVI_TX4+ MB

TMDS_CH2+ NC1
TMDS_CH2- NC2
GND1 GND2
TMDS_CH1+ NC3
TMDS_CH1- NC4

U4801

/X/ESD

IP4284CZ10-TB

DVI_TX3- MB
DVI_TX3+ MB
DVI_CLK- MB
DVI_CLK+ MB

U4802

/X/ESD

HDMI CON

RED
GREEN
BLUE
CLK

HDMI_CON1

P_GND1 P_GND3 P_GND4 P_GND2

HDMI_CON_19P

12G24110195X

+5VS_HDMI

D4801 SS0520
F4801 0.2A/9V
+5VS
+5VS_HDMI

C4801 4.7UF/6.3V

PJP4801
1MM_OPEN_5MIL
/X

[12] NB_TMDS_HPD

D4804 BAV99
R4811 100KOhm
R4810 20KOhm
/X/ESD

R4805 4.7KOhm DVI_DDCDAT_MB
R4803 4.7KOhm DVI_DDCCLK_MB

R4807 4.7KOhm
R4806 4.7KOhm
+3VS

Q4804A UM6K1N
Q4804B UM6K1N

[12] DVI_DDCDAT1
[12] DVI_DDCCLK1
DVI_DDCDAT1
DVI_DDCCLK1

R4831 0Ohm
R4832 0Ohm

C4802 10PF
C4803 10PF

D4803 BAV99
D4802 BAV99

/X
+5VS
GND

[11] DVI_TX5-
[11] DVI_TX5+
[11] DVI_TX3-
[11] DVI_TX3+
[11] DVI_TX4-
[11] DVI_TX4+
[11] DVI_CLKB-
[11] DVI_CLKB+

RNX4801A 0Ohm
RNX4801B 0Ohm
RNX4802A 0Ohm
RNX4802B 0Ohm
RNX4803A 0Ohm
RNX4803B 0Ohm
RNX4804A 0Ohm
RNX4804B 0Ohm

90Ohm/100Mhz

L4804 N/A
L4805 N/A
L4806 N/A
L4807 N/A

R1.1

DVI_TX5- MB
DVI_TX5+ MB
DVI_TX3- MB
DVI_TX3+ MB
DVI_TX4- MB
DVI_TX4+ MB
DVI_CLK- MB
DVI_CLK+ MB

RED
GREEN
BLUE
CLK

R1908 R1909 R1910 R1911 R1912 R1913 R1914 R1915
680Ohm

Q4802 2N7002
+5VS
R1917 100KOhm r0402

2008.03.10
R1908, R1909, R1910, R1911, R1912, R1913, R1914, R1915 change to 680OHM

R1.1 EMI
mount choke,unmount o ohm resistor

<Variant Name>

ASUSTek COMPUTER INC

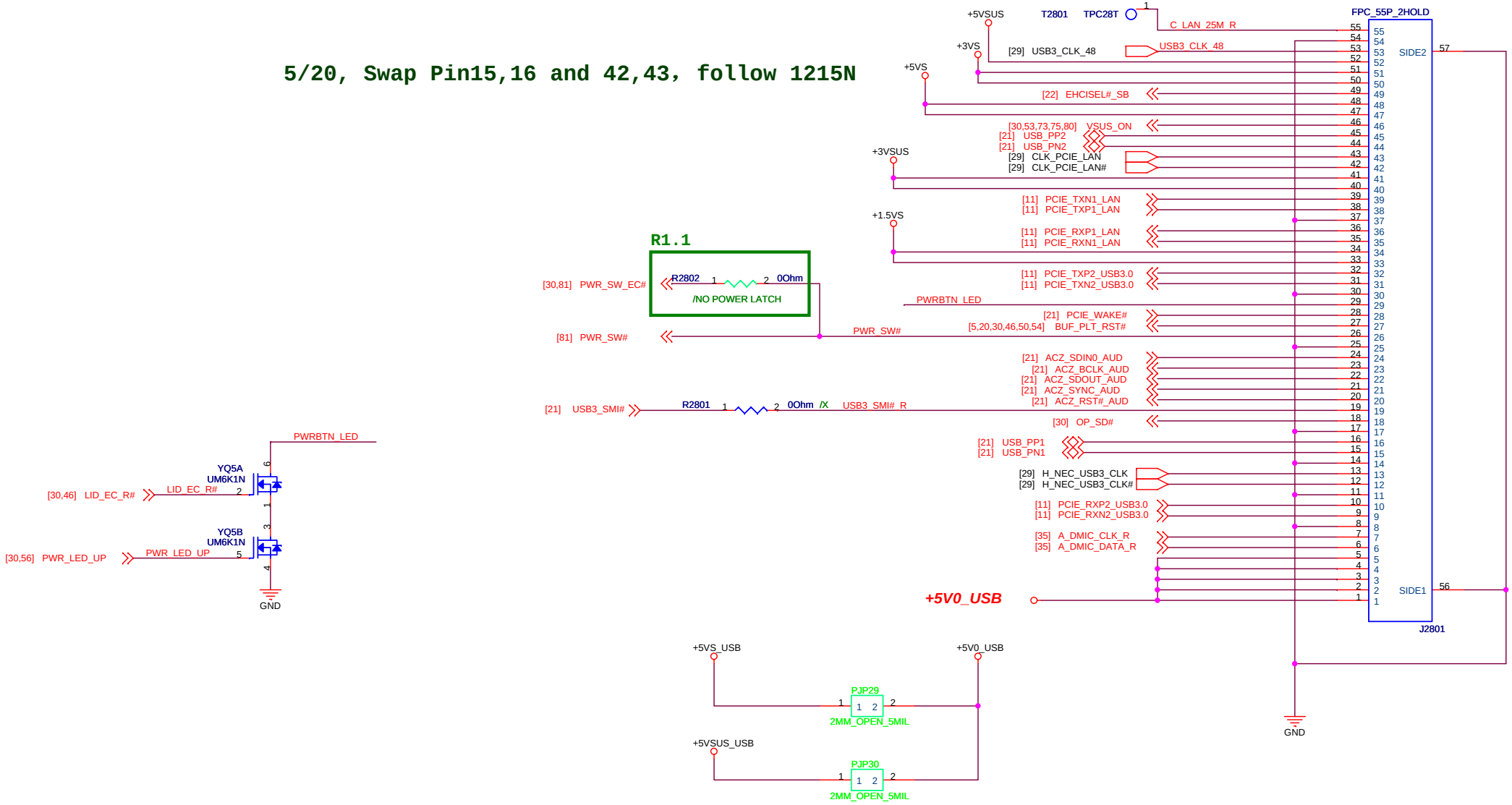
Title : HDMI
Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 25 of 80

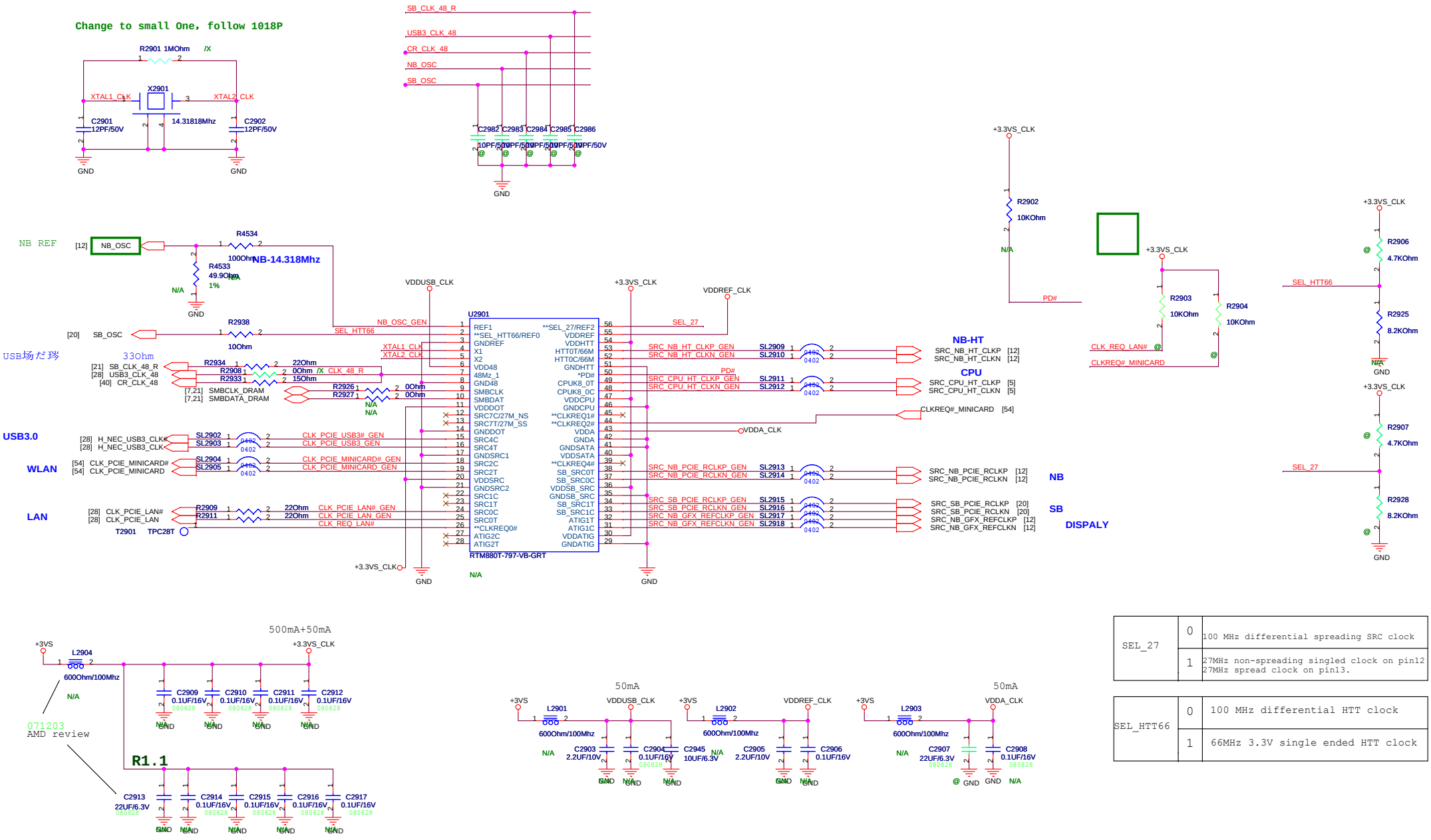
<Variant Name>

ASUSTek Computer INC.	Title : Bluetooth	
	Engineer: N/A	
Size: A	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 27 of 80	



<Variant Name>

ASUSTek Computer INC.	Title : Small brd Conn	
	Engineer: N/A	
Size: B	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 28 of 80	



SEL_27	0	100 MHz differential spreading SRC clock
	1	27MHz non-spreading singled clock on pin12 27MHz spread clock on pin13.

SEL_HTT66	0	100 MHz differential HTT clock
	1	66MHz 3.3V single ended HTT clock

<Variant Name>

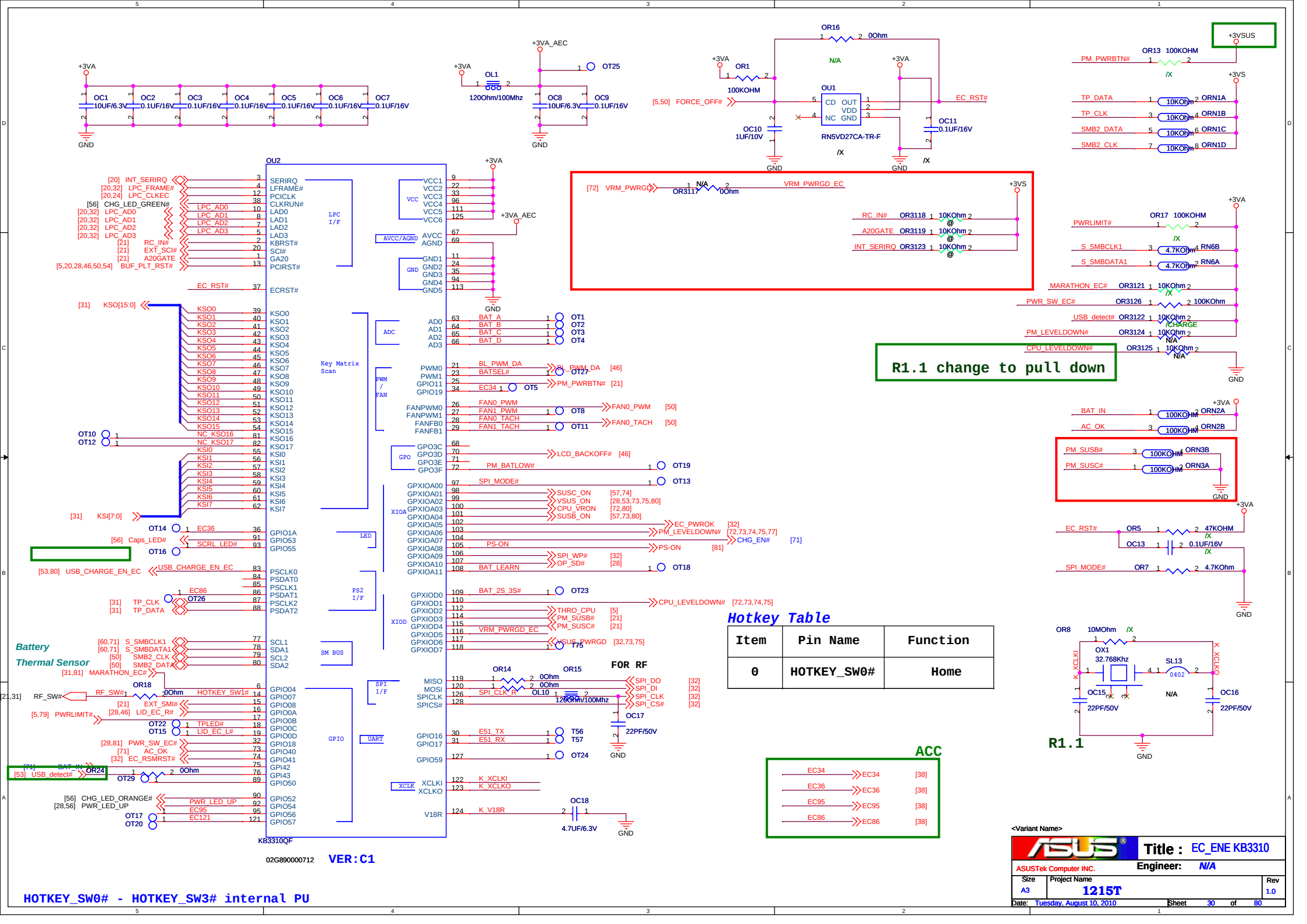
ASUSTeK COMPUTER INC

Title : RTM880T-797-VB-GRT

Engineer: N/A

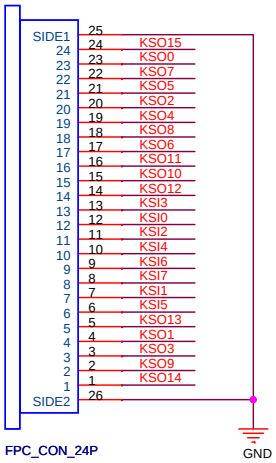
Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 29 of 80

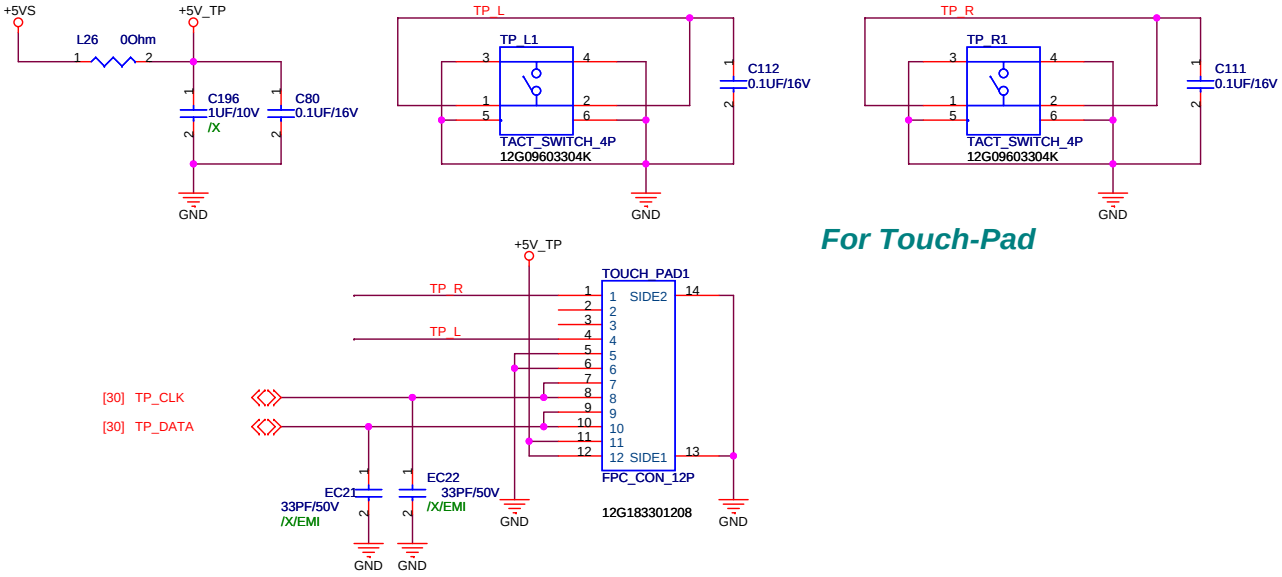

OU2
KB3310QF
02G890000712
VER:C1
R1.1 change to pull down
Hotkey Table
Item | Pin Name | Function
0 | HOTKEY_SW0# | Home
ACC
FOR RF
Battery
Thermal Sensor
HOTKEY_SW0# - HOTKEY_SW3# internal PU
R1.1
Title : EC_ENE KB3310
ASUSTek Computer INC.
Engineer: N/A
Size A3
Project Name 1215T
Rev 1.0
Date: Tuesday, August 10, 2010
Sheet 30 of 80

follow 1201T

KB_CON1 12G182102402

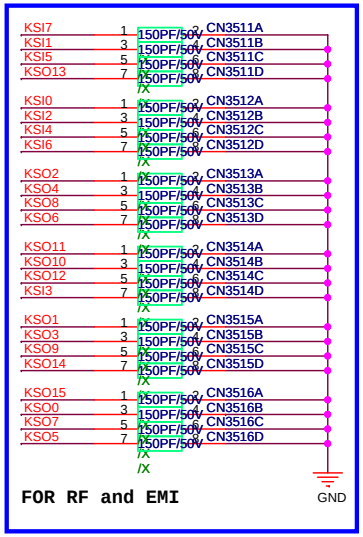


For Keyboard Connector

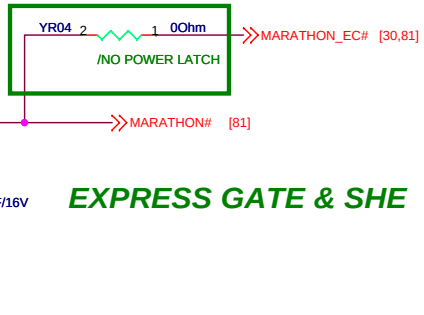


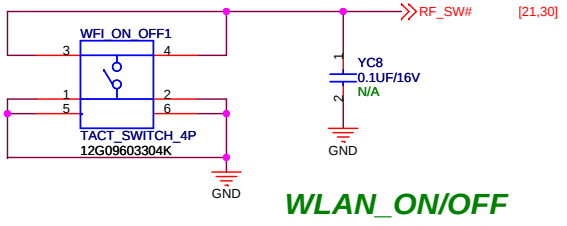
KSO[15:0] [30]

KSI[7:0] [30]



R1.1



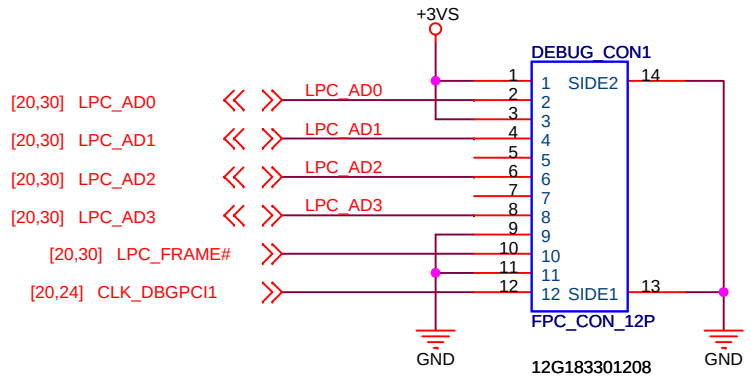


R1.1
DEL PWR1

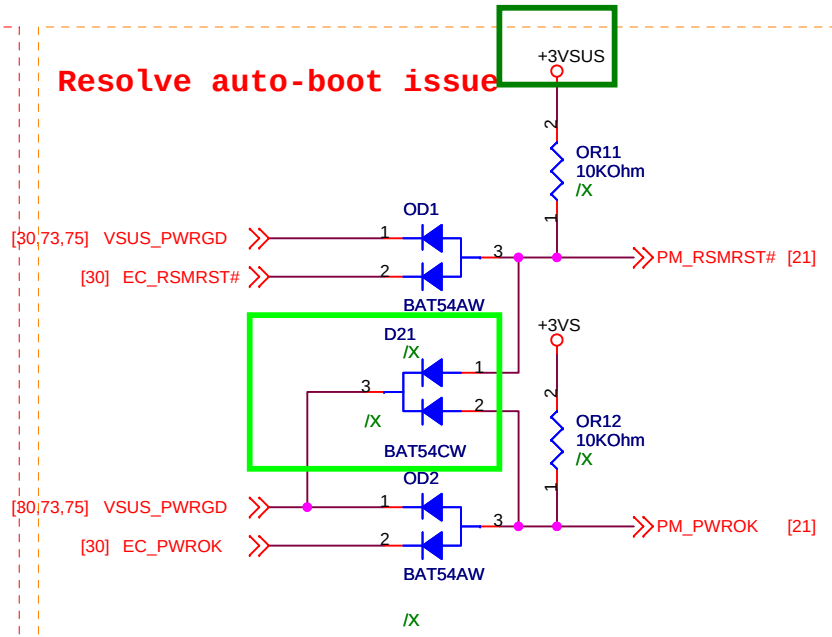
<Variant Name>

ASUSTek Computer INC.	Title : KB_Touch Pad	
	Engineer: N/A	
Size: B	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 31 of 80	

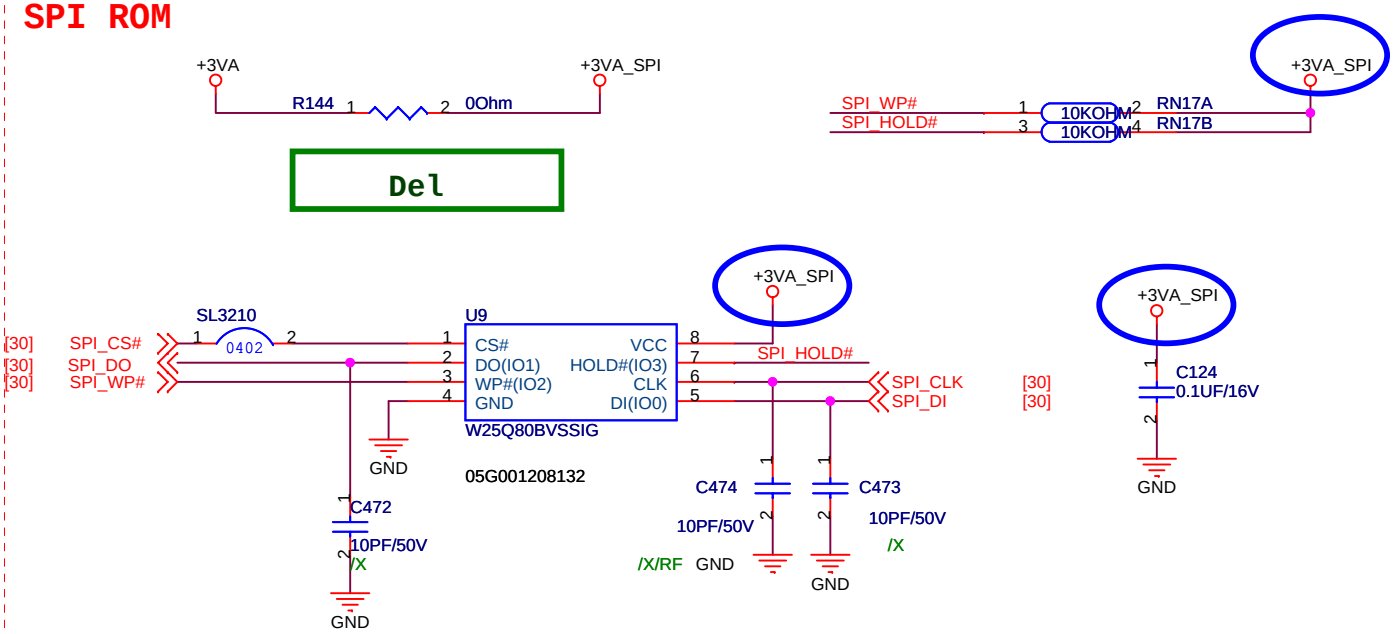
For Debug

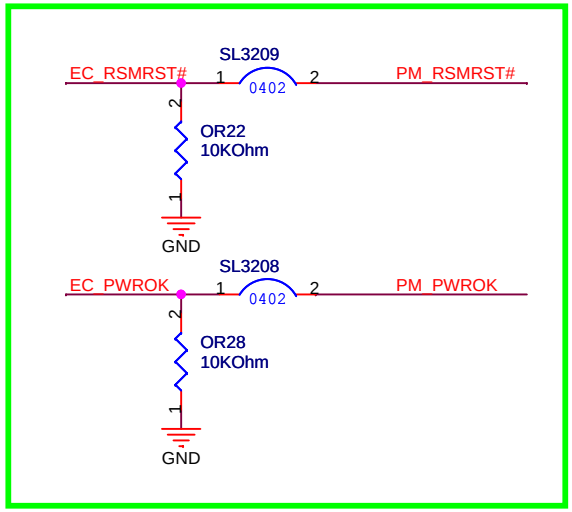


Resolve auto-boot issue



SPI ROM





<Variant Name>

ASUSTek Computer INC.	Title : SPI ROM/ Debug	
	Engineer: N/A	
Size: A4	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 32 of 80	

<Variant Name>

Title : AR8113/AR8132

ASUSTek Computer INC

Engineer: N/A

Size	Project Name	Rev
A3	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 33 of 80

<Variant Name>

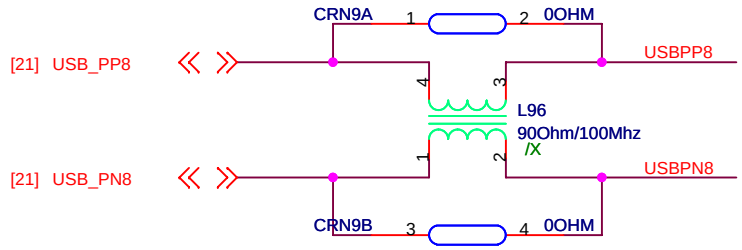
Title : RJ45

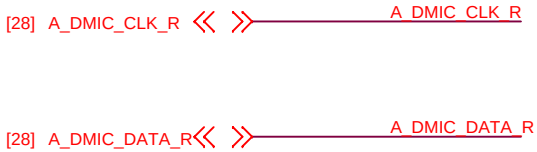
ASUSTek Computer INC.

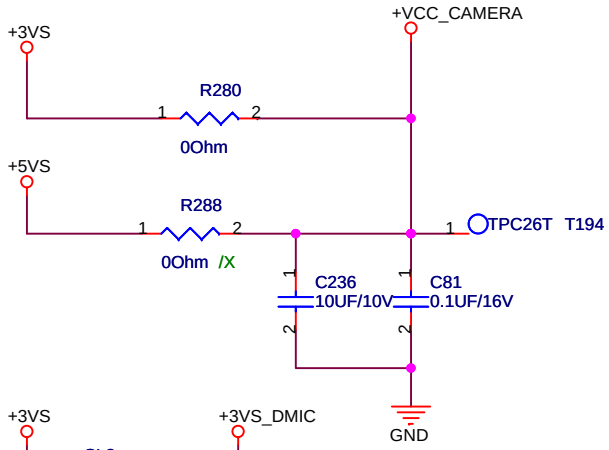
Engineer: N/A

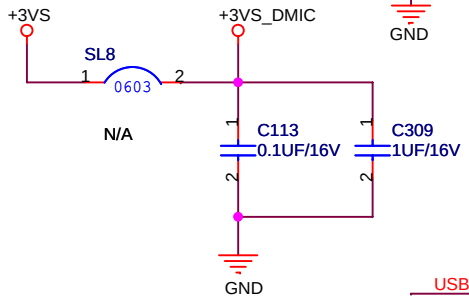
Size	Project Name	Rev
A3	1215T	1.0

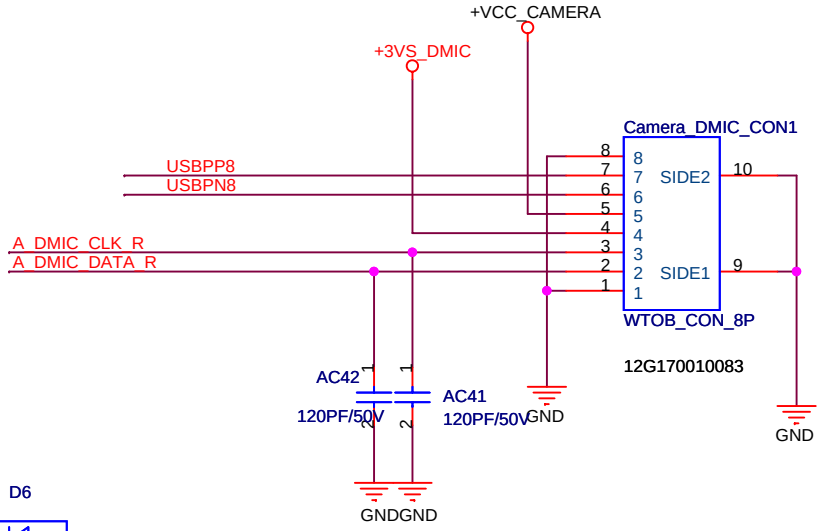
Date: Tuesday, August 10, 2010 Sheet 34 of 80

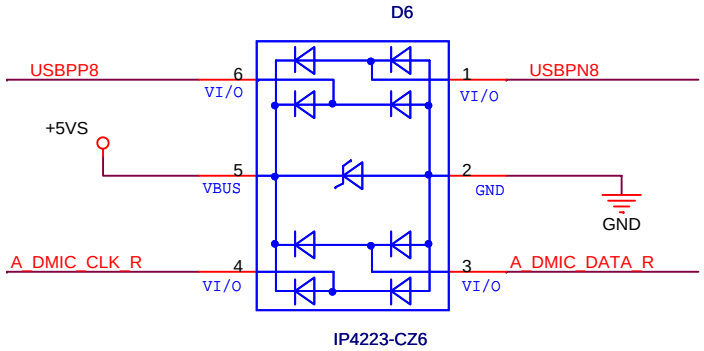












<variant_name>

ASUSTek Computer INC.	Title : CMOS	
	Engineer: N/A	
Size: A4	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 35 of 80	

NOTE

VA6:02G611005006

VB5:02G611005015

<Variant Name>

ASUSTek Computer INC.	Title : ALC269	
	Engineer: N/A	
Size: A	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 36 of 80	

<Variant Name>

Title : MIC_HP_SPK

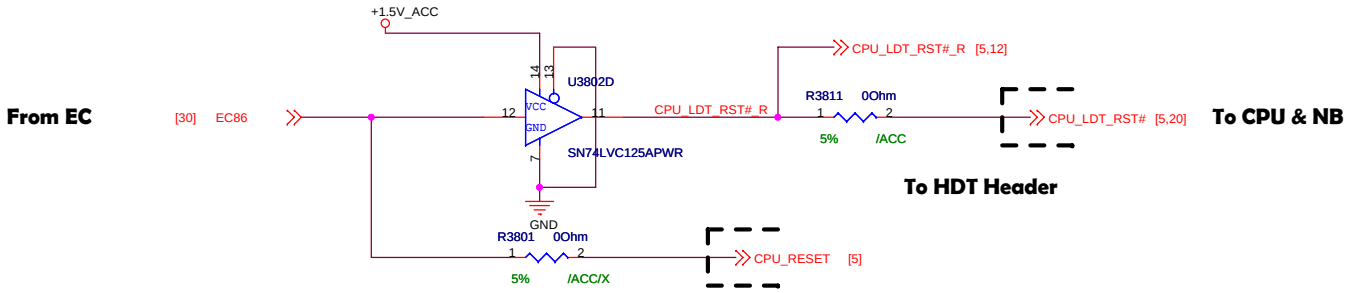
ASUSTek Computer INC.

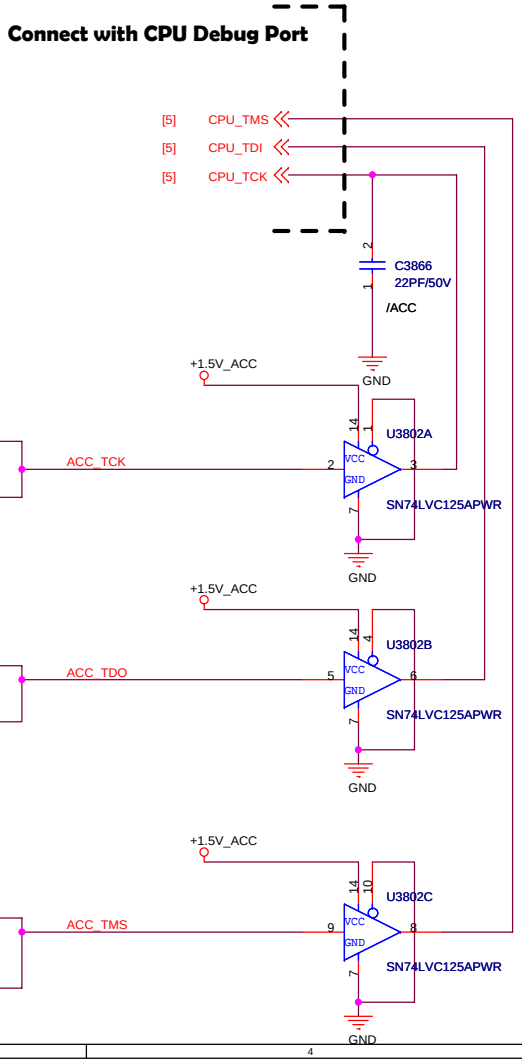
Engineer: N/A

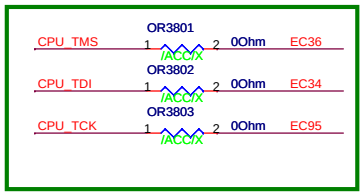
Size	Project Name	Rev
A	1215T	1.0

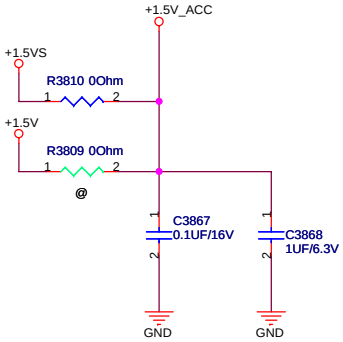
Date: Tuesday, August 10, 2010 Sheet 37 of 80

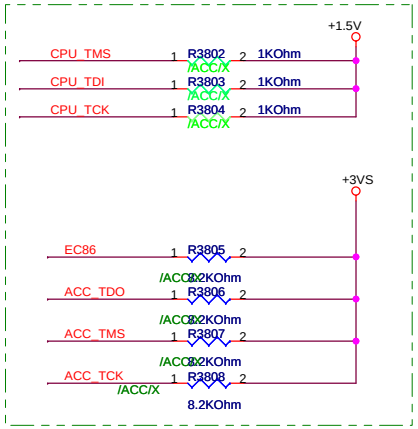
AOD ACC Function





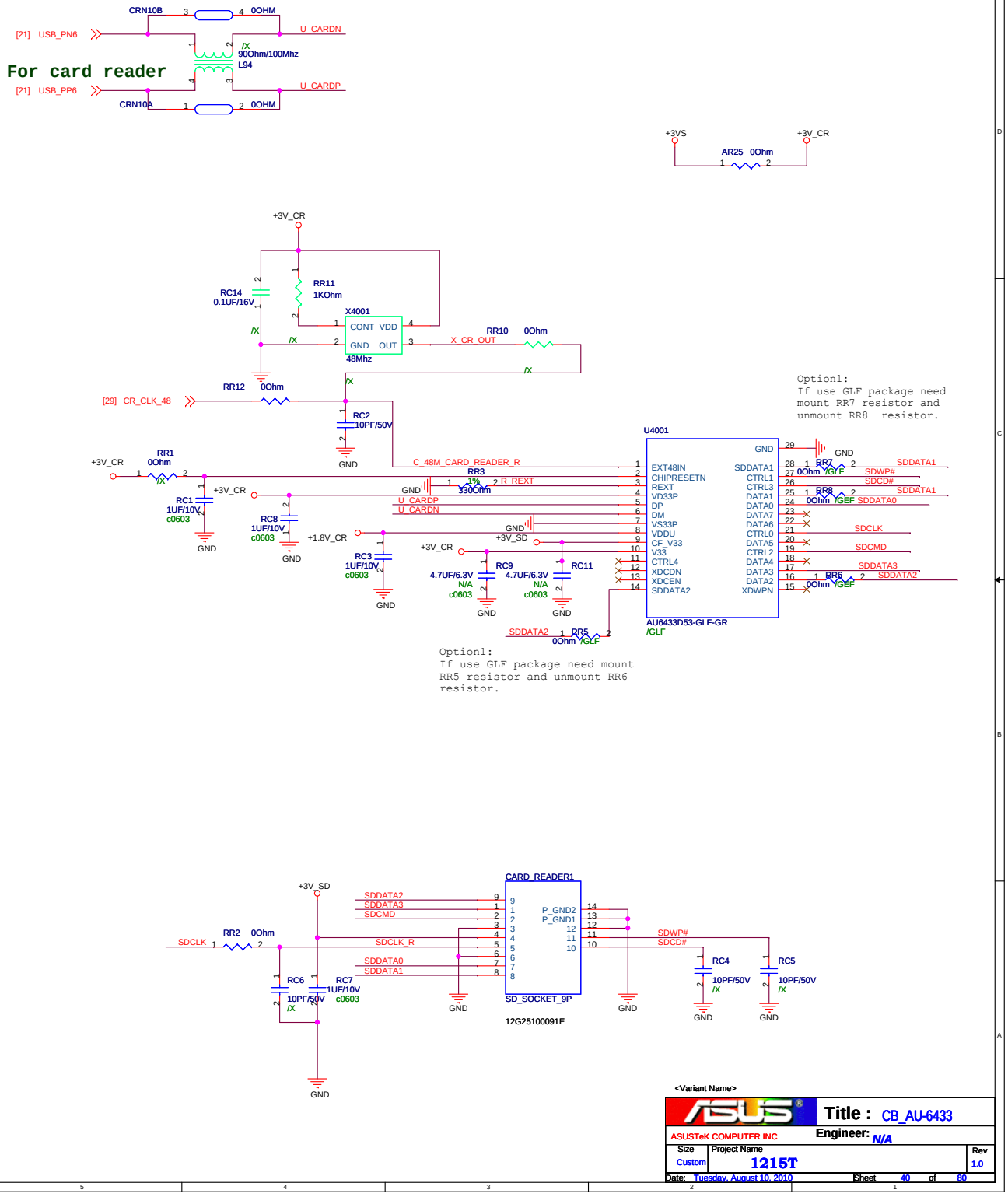






<variant_name>

ASUSTek Computer INC.	Title : ACC	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 38 of 70	


For card reader
CRN10B
0OHM
[21] USB_PN6
U_CARDN
/X
90Ohm/100Mhz
L94
[21] USB_PP6
U_CARDP
CRN10A
0OHM
+3VS
+3V_CR
AR25 0Ohm
+3V_CR
RR11
1KOhm
RC14
0.1UF/16V
X4001
CONT VDD
GND OUT
48Mhz
X_CR_OUT
RR10 0Ohm
RR12 0Ohm
[29] CR_CLK_48
RC2
10PF/50V
GND
Option1:
If use GLF package need
mount RR7 resistor and
unmount RR8 resistor.
U4001
C_48M_CARD_READER_R
RR1
0Ohm
RR3
1%
330Ohm
R_REXT
RC1
1UF/10V
c0603
RC8
1UF/10V
c0603
U_CARDP
U_CARDN
+1.8V_CR
RC3
1UF/10V
c0603
+3V_SD
RC9
4.7UF/6.3V
N/A
c0603
RC11
4.7UF/6.3V
N/A
c0603
EXT48IN
CHIPRESETN
REXT
VD33P
DP
DM
VS33P
VDDU
CF_V33
V33
CTRL4
XDCDN
XDCEN
SDDATA2
SDDATA1
CTRL1
CTRL3
DATA1
DATA0
DATA7
DATA6
CTRL0
DATA5
CTRL2
DATA4
DATA3
DATA2
XDWPN
AU6433D53-GLF-GR
/GLF
RR7
SDDATA1
SDWP#
SDCD#
RR8
SDDATA0
SDCLK
SDCMD
SDDATA3
RR6
SDDATA2
RR5
Option1:
If use GLF package need mount
RR5 resistor and unmount RR6
resistor.
CARD_READER1
SD_SOCKET_9P
12G25100091E
P_GND2
P_GND1
SDCLK
RR2 0Ohm
SDCLK_R
SDDATA0
SDDATA1
SDDATA2
SDDATA3
SDCMD
SDWP#
SDCD#
RC6
10PF/50V
/X
RC7
1UF/10V
c0603
RC4
10PF/50V
/X
RC5
10PF/50V
/X
GND
+3V_SD
<Variant Name>
Title : CB_AU-6433
ASUSTeK COMPUTER INC
Engineer: N/A
Size
Custom
Project Name
1215T
Rev
1.0
Date: Tuesday, August 10, 2010
Sheet 40 of 80

<variant_name><Variant Name></variant_name>

3.5G Module & External Antenna

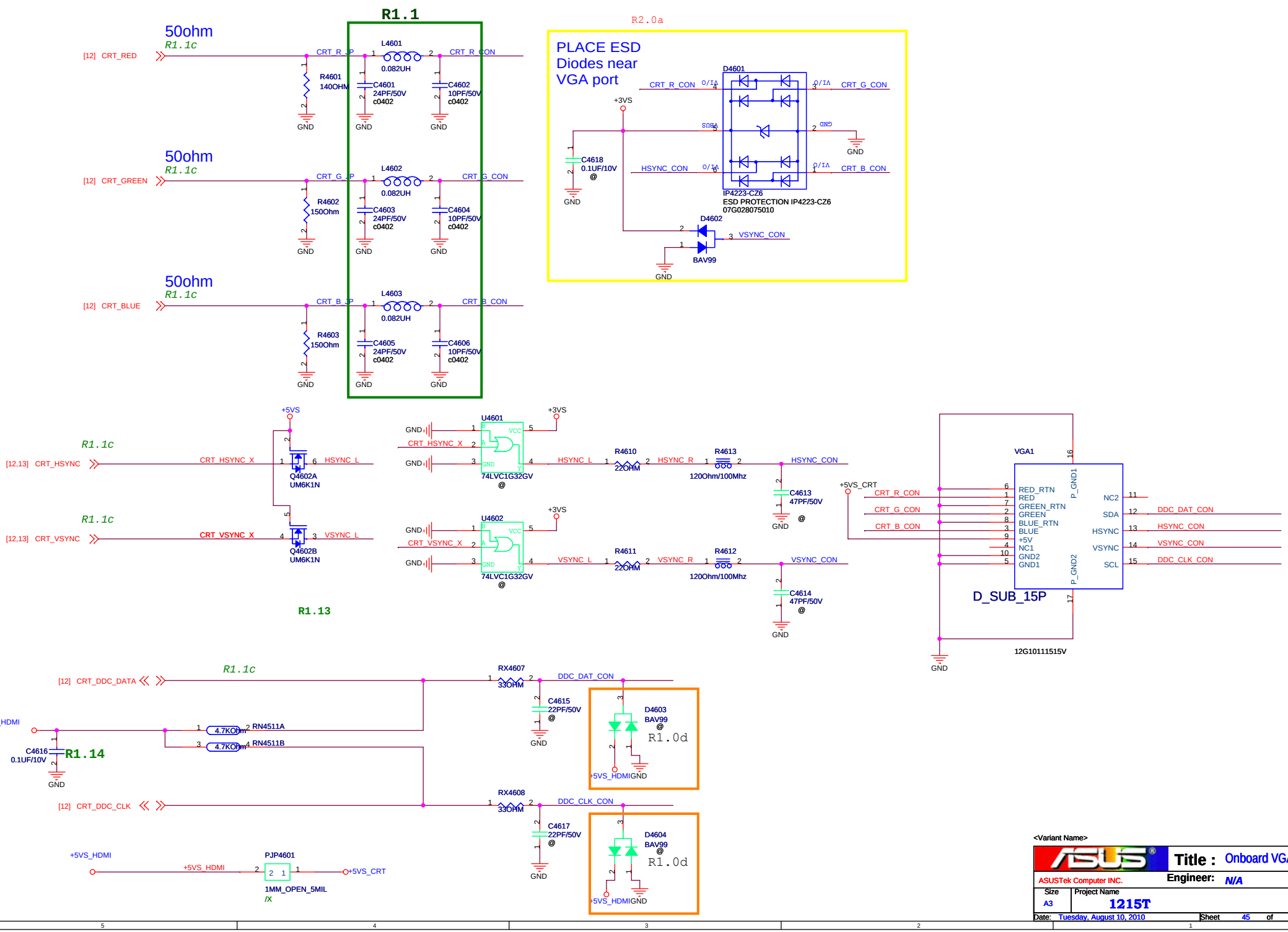
Title :

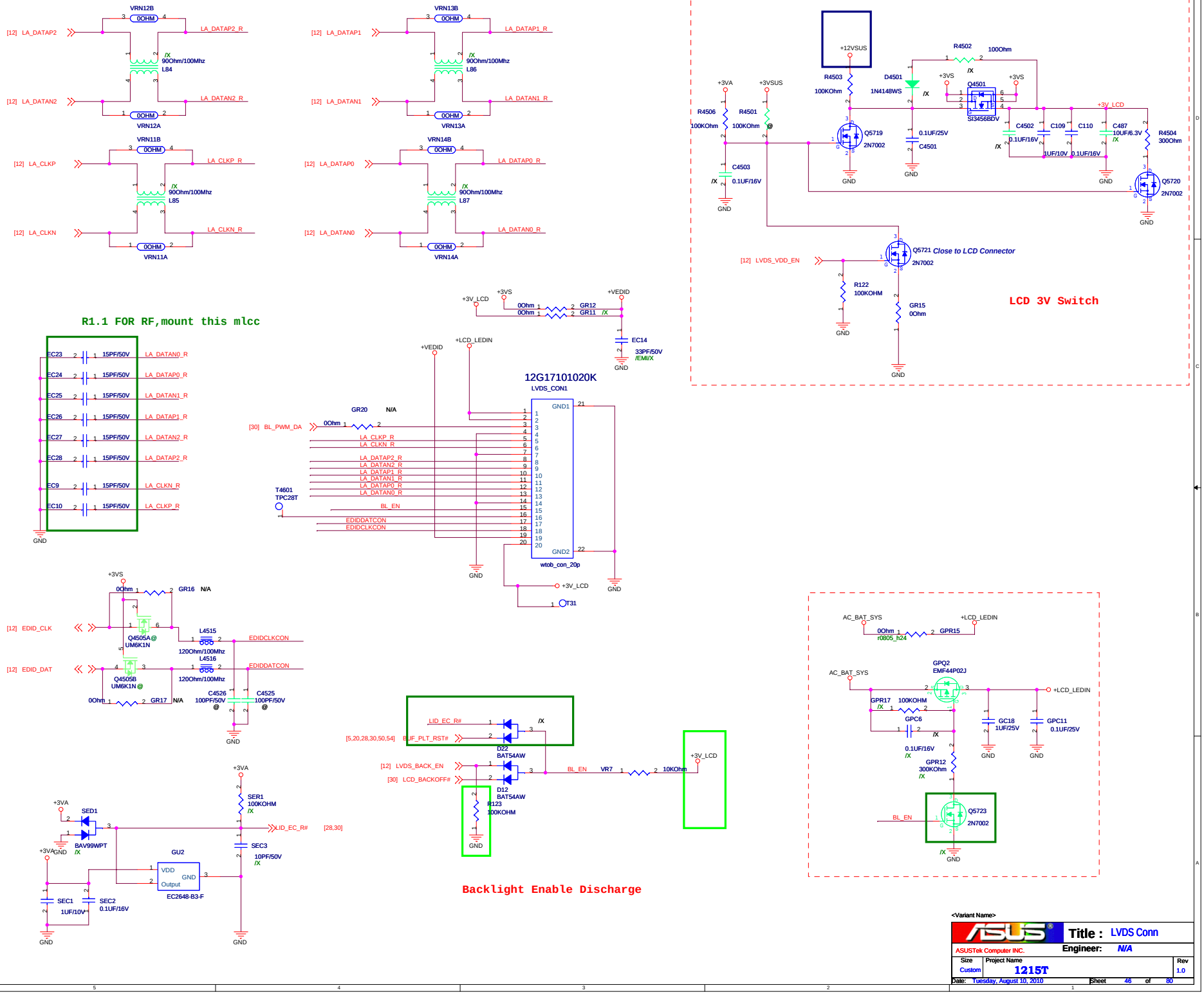
ASUSTek Computer INC.

Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 41 of 80

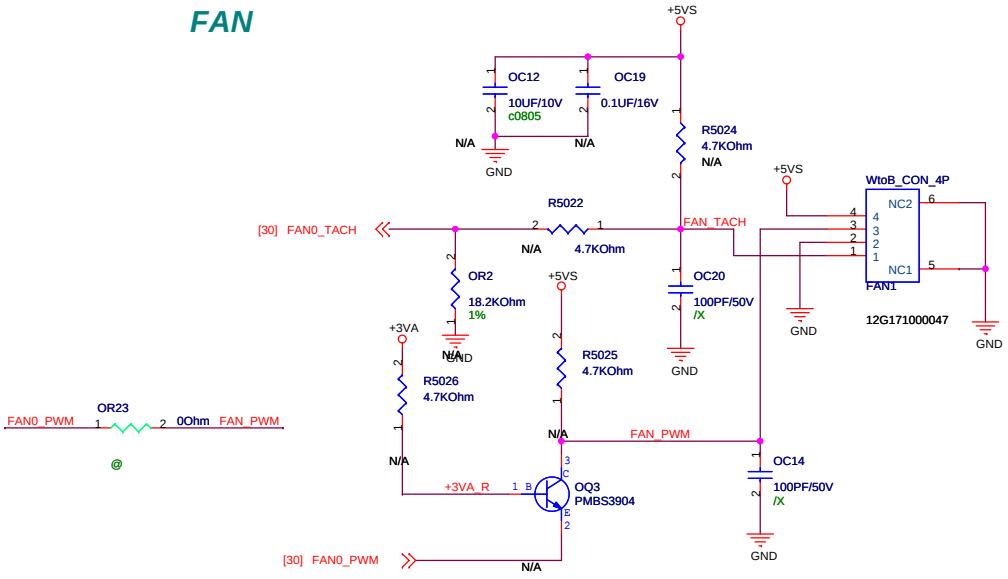

R1.1
R2.0a
50ohm
R1.1c
[12] CRT_RED
CRT_R_P
L4601
0.082UH
CRT_R_CON
R4601
140OHM
C4601
24PF/50V
c0402
C4602
10PF/50V
c0402
GND
50ohm
R1.1c
[12] CRT_GREEN
CRT_G_P
L4602
0.082UH
CRT_G_CON
R4602
150Ohm
C4603
24PF/50V
c0402
C4604
10PF/50V
c0402
50ohm
R1.1c
[12] CRT_BLUE
CRT_B_P
L4603
0.082UH
CRT_B_CON
R4603
150Ohm
C4605
24PF/50V
c0402
C4606
10PF/50V
c0402
PLACE ESD
Diodes near
VGA port
D4601
CRT_R_CON
CRT_G_CON
HSYNC_CON
CRT_B_CON
+3VS
C4618
0.1UF/10V
@
IP4223-CZ6
ESD PROTECTION IP4223-CZ6
07G028075010
D4602
VSYNC_CON
BAV99
R1.1c
[12,13] CRT_HSYNC
CRT_HSYNC_X
Q4602A
UM6K1N
HSYNC_L
U4601
74LVC1G32GV
@
HSYNC_L
R4610
22OHM
HSYNC_R
R4613
120Ohm/100Mhz
HSYNC_CON
C4613
47PF/50V
@
R1.1c
[12,13] CRT_VSYNC
CRT_VSYNC_X
Q4602B
UM6K1N
VSYNC_L
U4602
74LVC1G32GV
@
VSYNC_L
R4611
22OHM
VSYNC_R
R4612
120Ohm/100Mhz
VSYNC_CON
C4614
47PF/50V
@
+5VS_CRT
VGA1
CRT_R_CON
CRT_G_CON
CRT_B_CON
RED_RTN
RED
GREEN_RTN
GREEN
BLUE_RTN
BLUE
+5V
NC1
GND2
GND1
P_GND1
P_GND2
NC2
SDA
HSYNC
VSYNC
SCL
DDC_DAT_CON
HSYNC_CON
VSYNC_CON
DDC_CLK_CON
D_SUB_15P
12G10111515V
R1.13
R1.1c
[12] CRT_DDC_DATA
RX4607
33OHM
DDC_DAT_CON
C4615
22PF/50V
@
D4603
BAV99
@
R1.0d
+5VS_HDMI
4.7KOhm
RN4511A
4.7KOhm
RN4511B
C4616
0.1UF/10V
R1.14
[12] CRT_DDC_CLK
RX4608
33OHM
DDC_CLK_CON
C4617
22PF/50V
@
D4604
BAV99
@
R1.0d
PJP4601
1MM_OPEN_5MIL
/X
<Variant Name>
Title : Onboard VGA
ASUSTek Computer INC.
Engineer: N/A
Size A3
Project Name 1215T
Rev 1.0
Date: Tuesday, August 10, 2010
Sheet 45 of 80



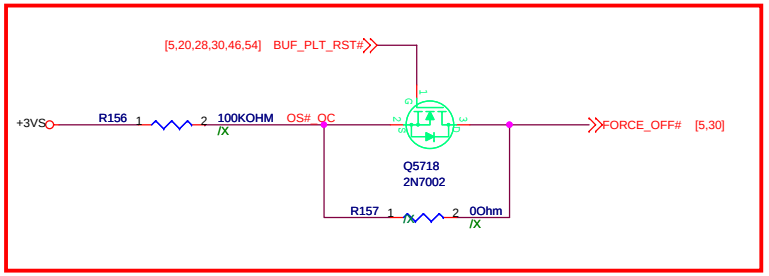
<variant_name>

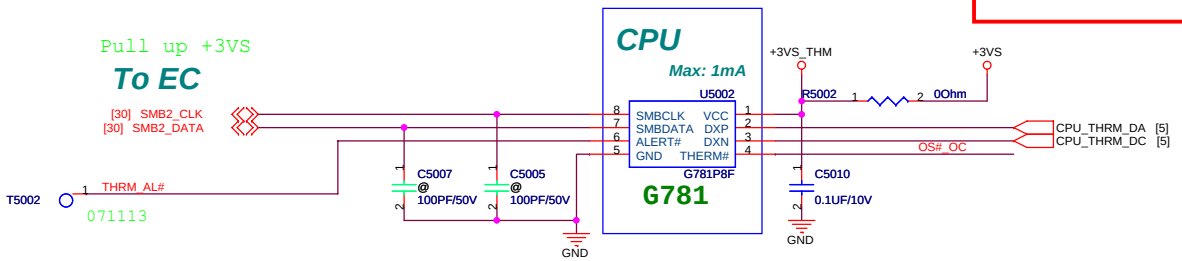
ASUSTek Computer INC.	Title : LVDS Conn	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 46 of 80	

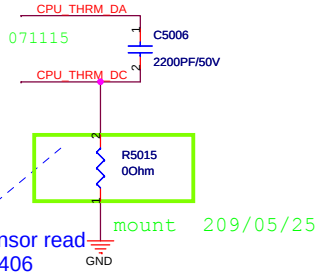
FAN



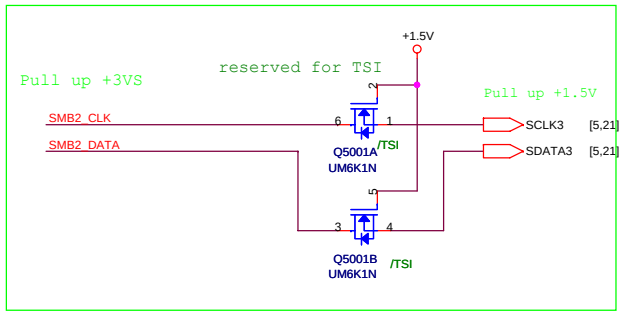
Thermal Sensor







Add R5014 for thermal sensor read wrong temp issue. 090406



<Variant Name>

ASUSTek Computer INC.	Title : FAN_THERMAL SENSOR	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 50 of 80	

<Variant Name>

Title : USB3.0 Fresco

ASUSTek Computer INC.

Engineer: N/A

Size	Project Name	Rev
C	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 51 of 80

Title : USB 3.0_PORT

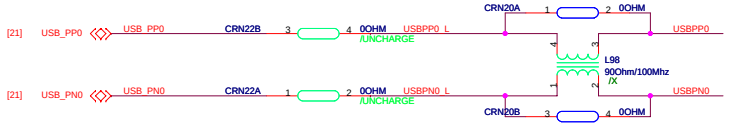
ASUSTeK COMPUTER INC. NB4

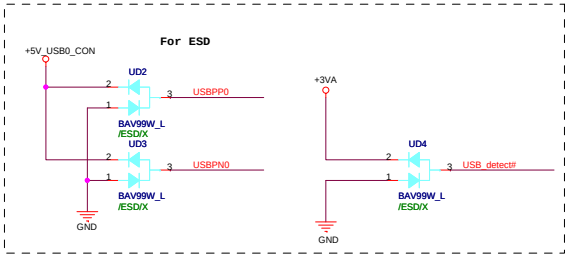
Engineer: NA

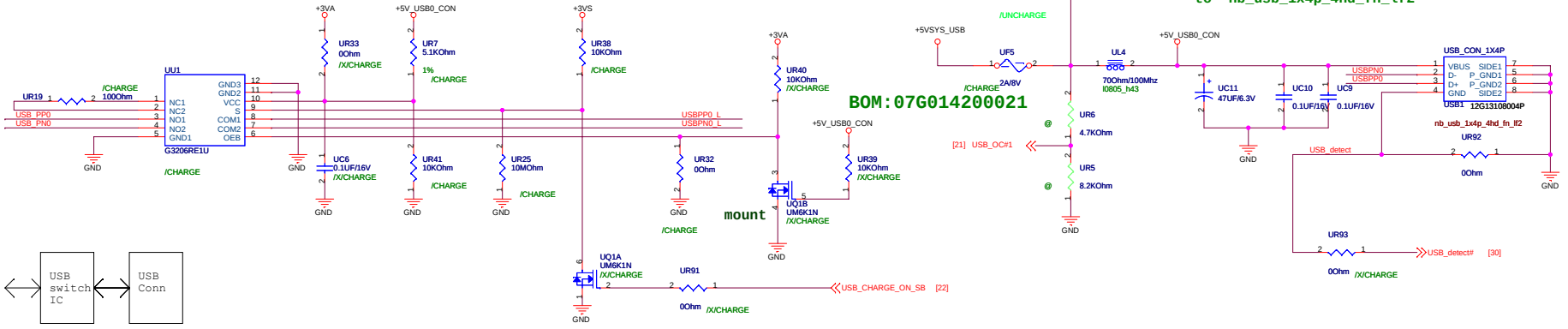
Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 52 of 80

USB2.0 with charge Connector(Optional)





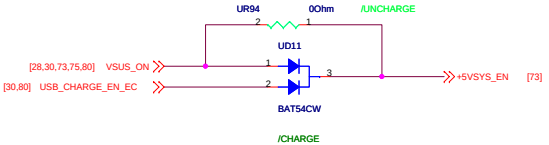


R1.1 USB1
change footprint from 'nb_usb_1x4p_4hod_ra_lf2'
to 'nb_usb_1x4p_4hd_fn_lf2'

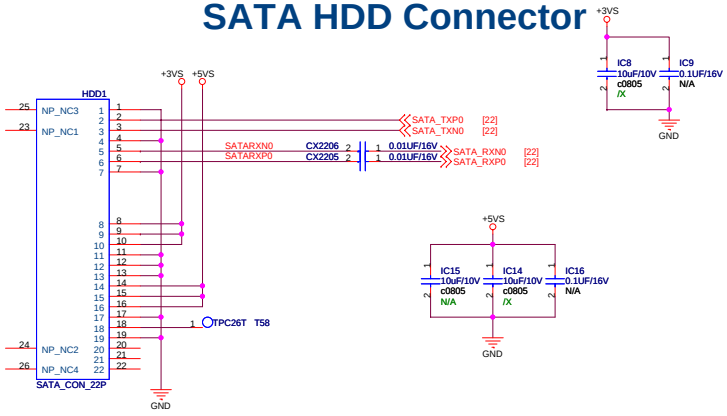
mount UQ1 in the BOM

Function Table

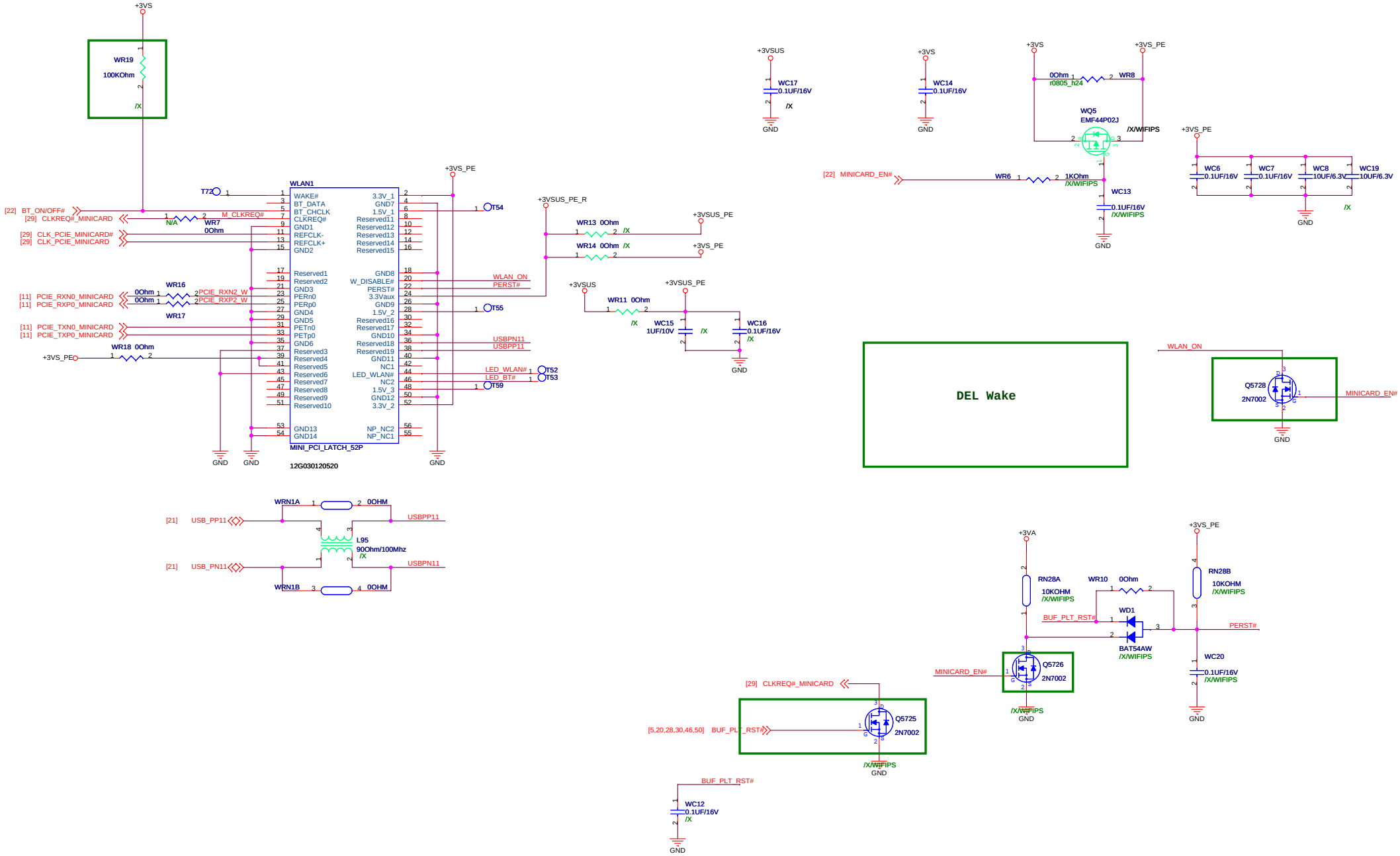
S	OEB	FUNCTION
X	H	Switch Disconnected
L	L	NC connected to Com
H	L	NO connected to Com



SATA HDD Connector



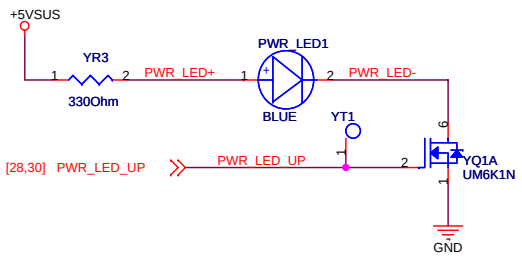
USB2.0 Connector



<Variant Name>

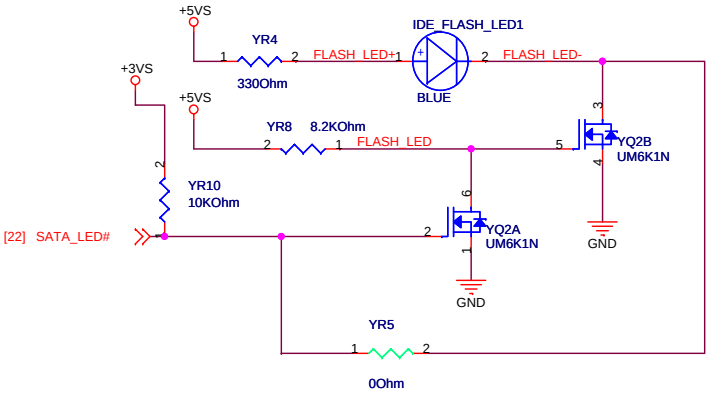
ASUSTek Computer INC.	Title : Mini WIFI	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 54 of 80	

For POWER LED

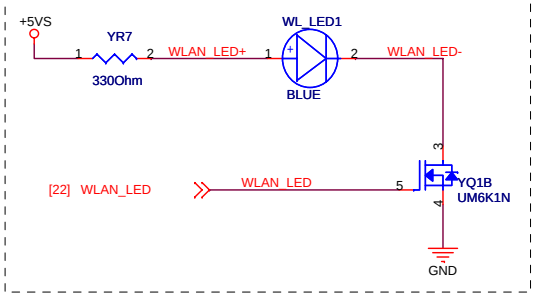


Mode / Scenario	Adapater Mode	Battery Mode
Battery power is between 100%~40%	Orange ON	Green ON
Battery power is between 40%~10%	Orange Blinking Slowly	Green Blinking Slowly
Battery power is less than 10%	Orange Blinking Quickly	OFF
S3/S5 Mode	Scenario the same as above	

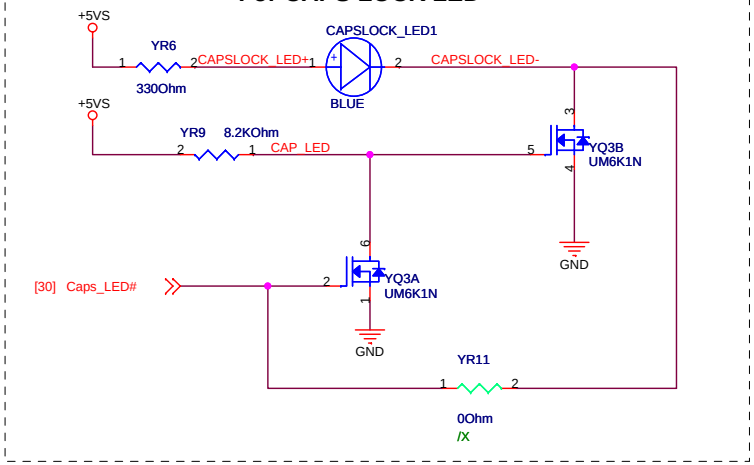
For IDE/SATA LED



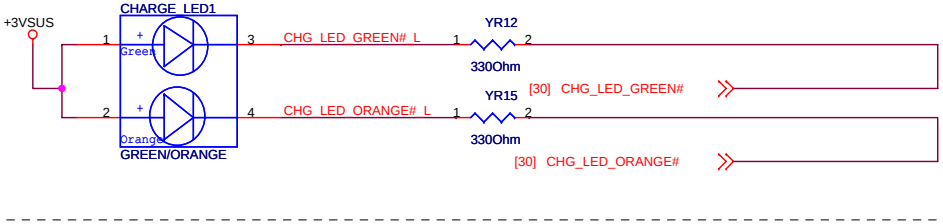
For WLAN LED



For CAPS LOCK LED



For CHARGE LED



<Variant Name>

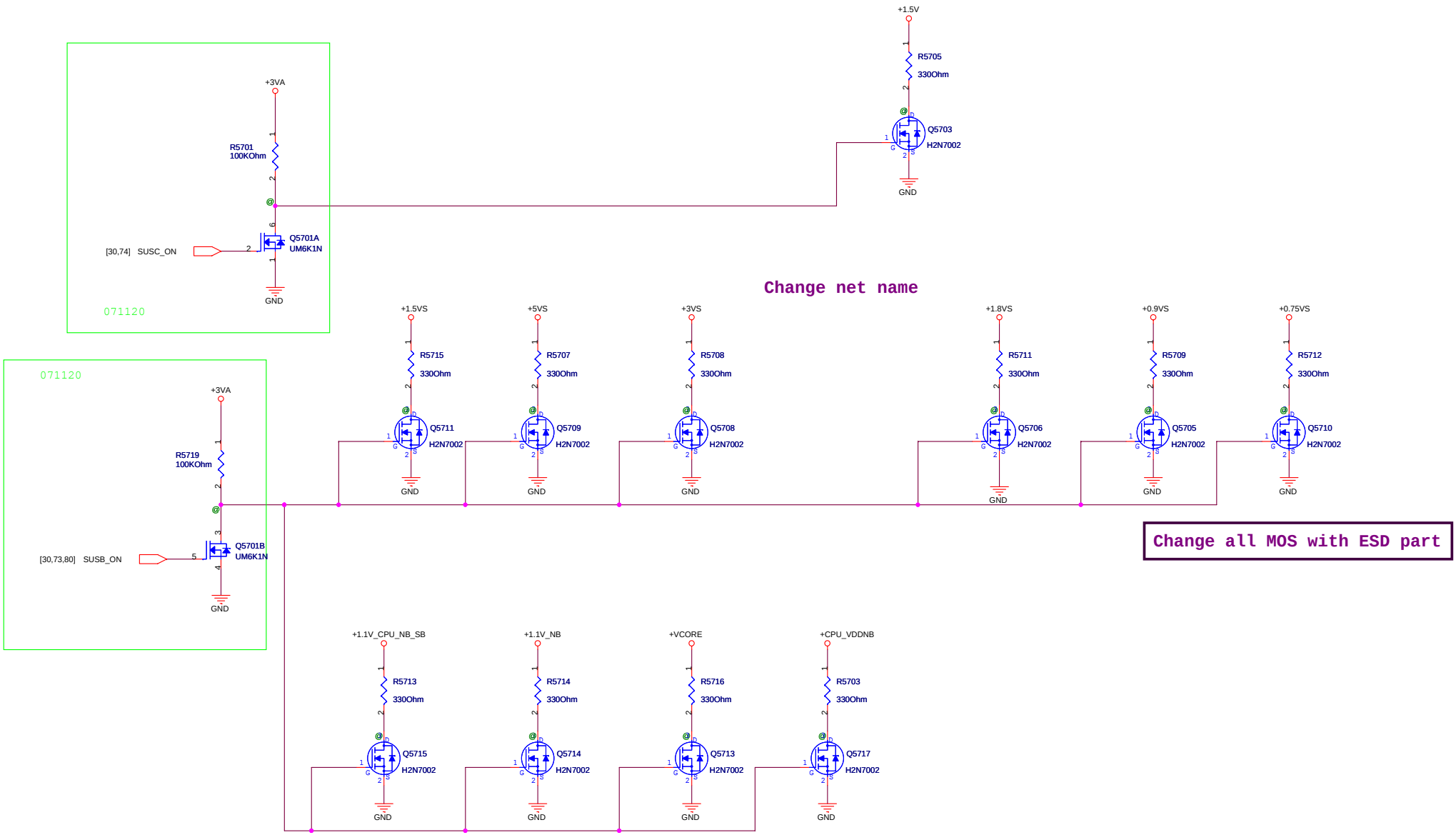
Title : LED/PWR SWICH

ASUSTeK COMPUTER INC

Engineer: NA

Size	Project Name	Rev
B	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 56 of 80



<Variant Name>

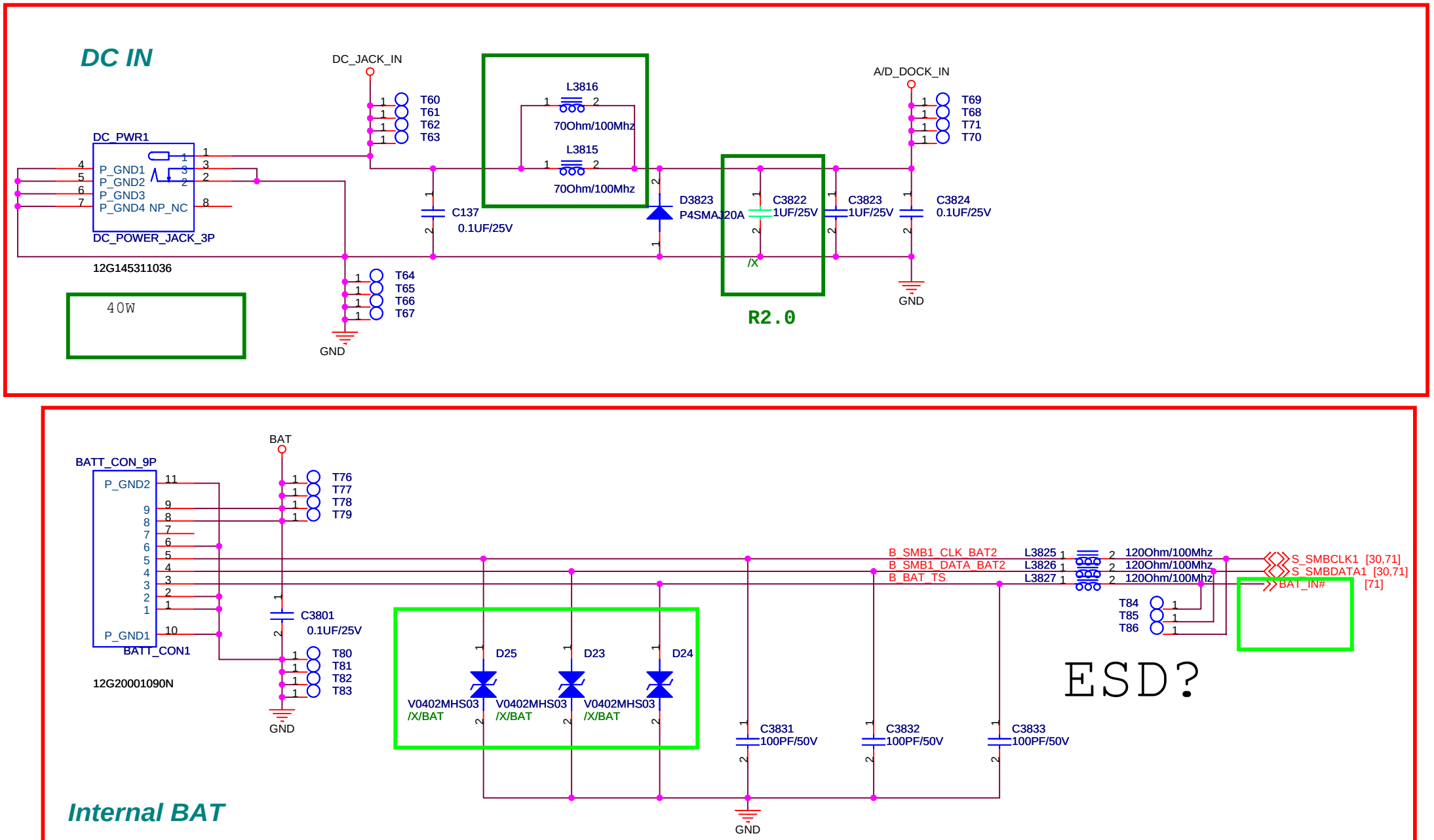
ASUSTeK COMPUTER INC

Title : DISCHARGE CKT

Engineer: N/A

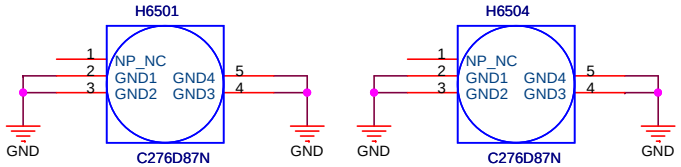
Size	Project Name	Rev
Custom	1215T	1.0

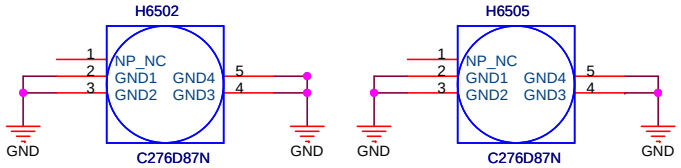
Date: Tuesday, August 10, 2010 Sheet 57 of 80

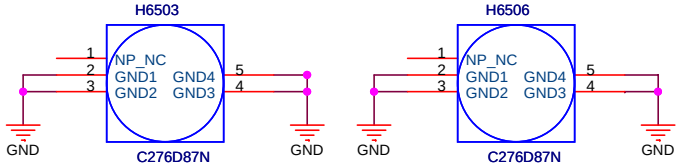


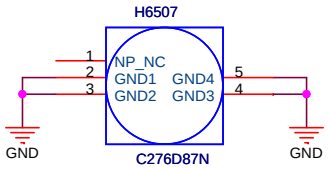
<Variant Name>

ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: N/A	
Size: A4	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 60 of 80	

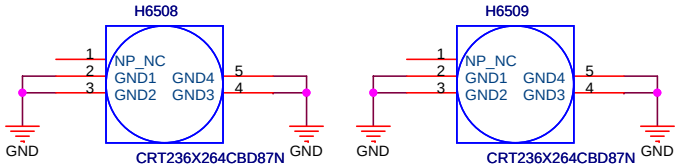




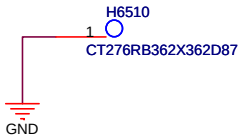




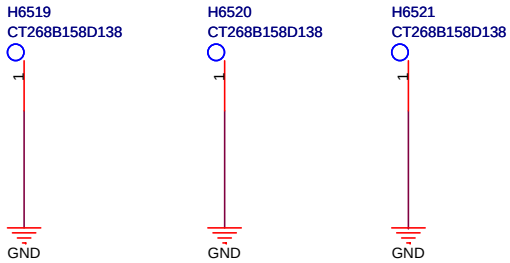
TYPE A SCREW HOLE



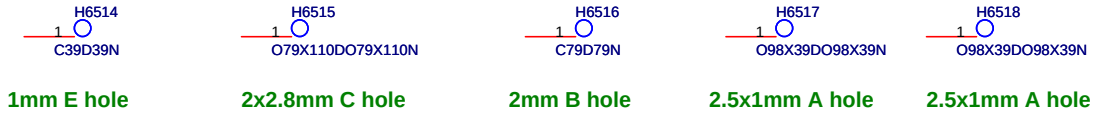
TYPE B SCREW HOLE



TYPE C SCREW HOLE

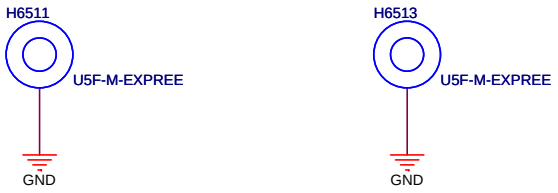


CPU Braket Hole



1mm E hole **2x2.8mm C hole** **2mm B hole** **2.5x1mm A hole** **2.5x1mm A hole**

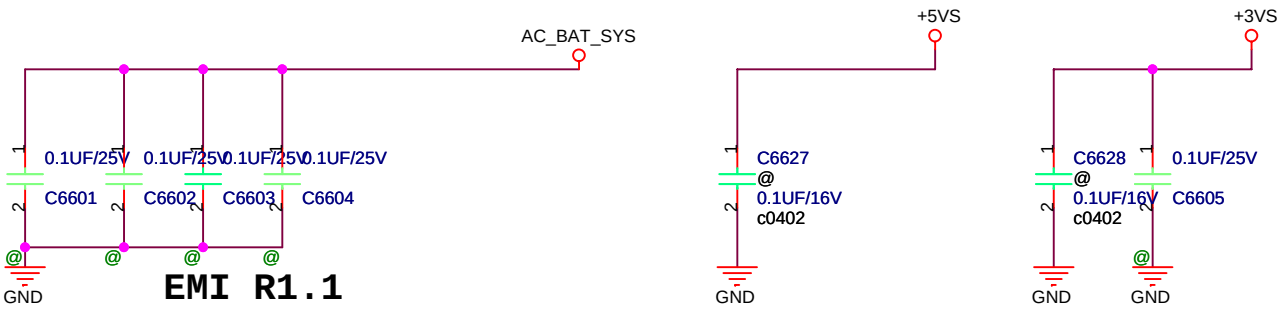
HOLE



NUT

<Variant Name>

ASUSTek Computer INC.	Title : Screw Hole	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 65 of 80	



<Variant Name>

ASUSTeK COMPUTER INC	Title : EMI	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 66 of 80	

ADD

0518：
add EMI Cap;
add R4806/R4807/Q4804

0520：
addT4601/PR167

DELETE

0520：
DEL PC85 PR107 PR12 PR87

MODIFY

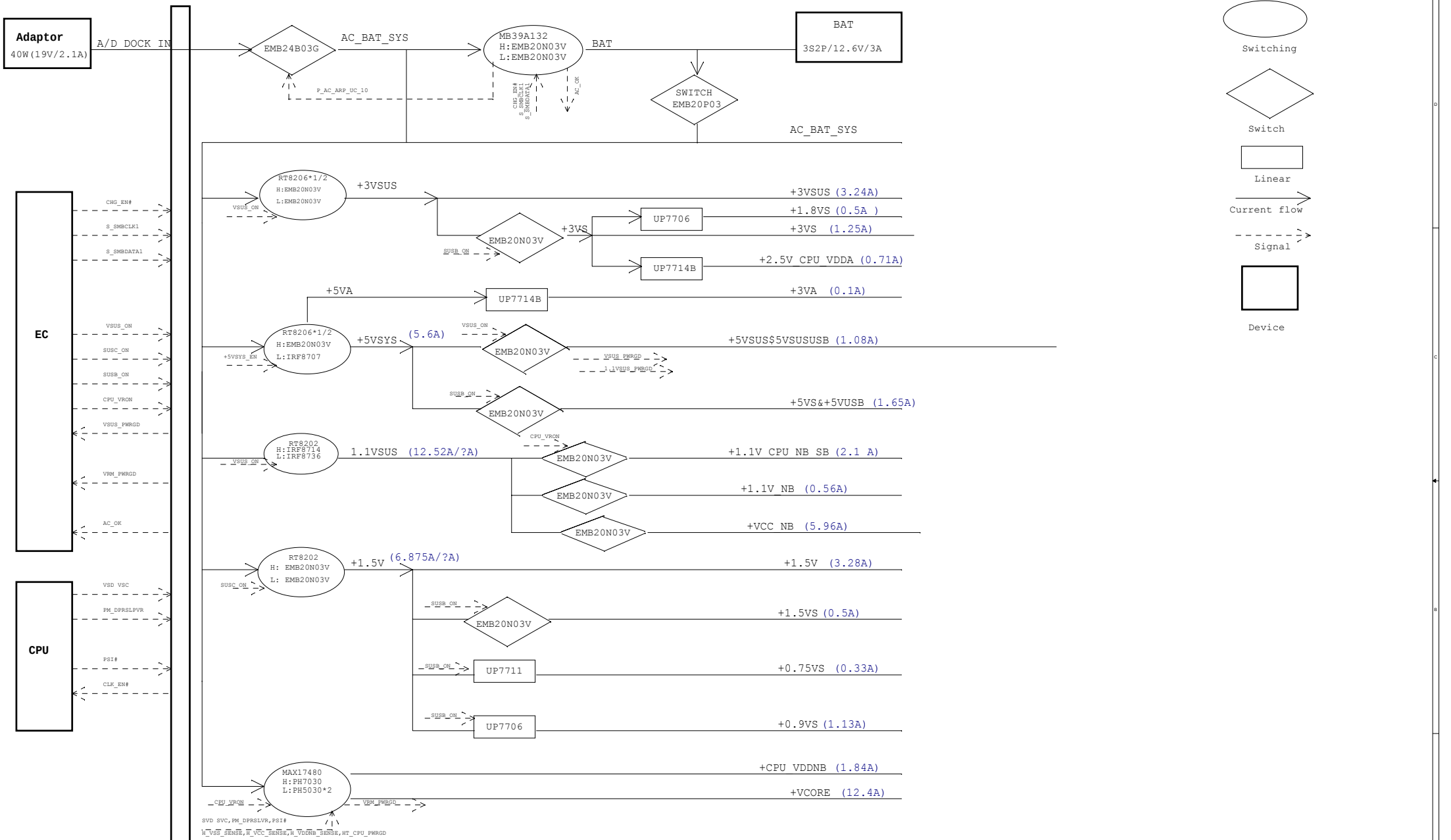
0517:
switch TP button PIN1 to PIN3;PIN2 to PIN4

<Variant Name>

ASUSTek Computer INC.	Title : History	
	Engineer: N/A	
Size: B	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 68 of 80	

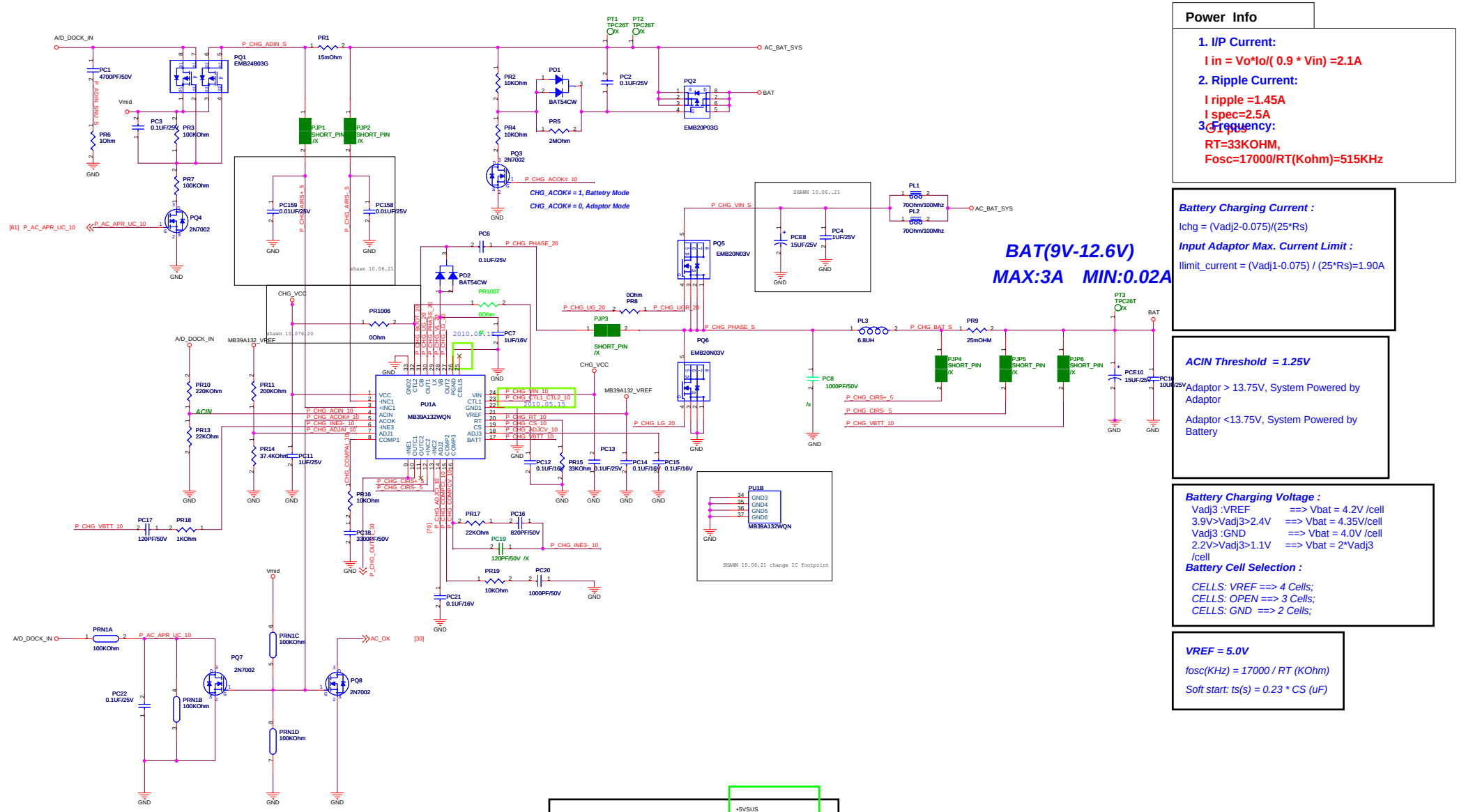
<Variant Name>

ASUSTek Computer INC.	Title : Small borad	
	Engineer: N/A	
Size: C	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 69 of 80	



<Variant Name>

ASUSTek Computer INC	Title : power flow	
	Engineer: N/A	
Size: A2	Project Name: 1015T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 70 of 80	



Power Info

1. I/P Current:
   I in = Vo*Io/(0.9 * Vin) =2.1A
2. Ripple Current:
   I ripple =1.45A
   I spec=2.5A
3. Frequency:
   RT=33KOHM,
   Fosc=17000/RT(Kohm)=515KHz

Battery Charging Current :

Ichg = (Vadj2-0.075)/(25*Rs)

Input Adaptor Max. Current Limit :

Ilimit_current = (Vadj1-0.075) / (25*Rs)=1.90A

ACIN Threshold = 1.25V

Adaptor > 13.75V, System Powered by Adaptor

Adaptor <13.75V, System Powered by Battery

Battery Charging Voltage :

Vadj3 :VREF ==> Vbat = 4.2V /cell
3.9V>Vadj3>2.4V ==> Vbat = 4.35V/cell
Vadj3 :GND ==> Vbat = 4.0V /cell
2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell

Battery Cell Selection :

CELLS: VREF ==> 4 Cells;
CELLS: OPEN ==> 3 Cells;
CELLS: GND ==> 2 Cells;

VREF = 5.0V

fosc(KHz) = 17000 / RT (KOhm)

*Soft start: ts(s) = 0.23 * CS (uF)*

<Variant Name>

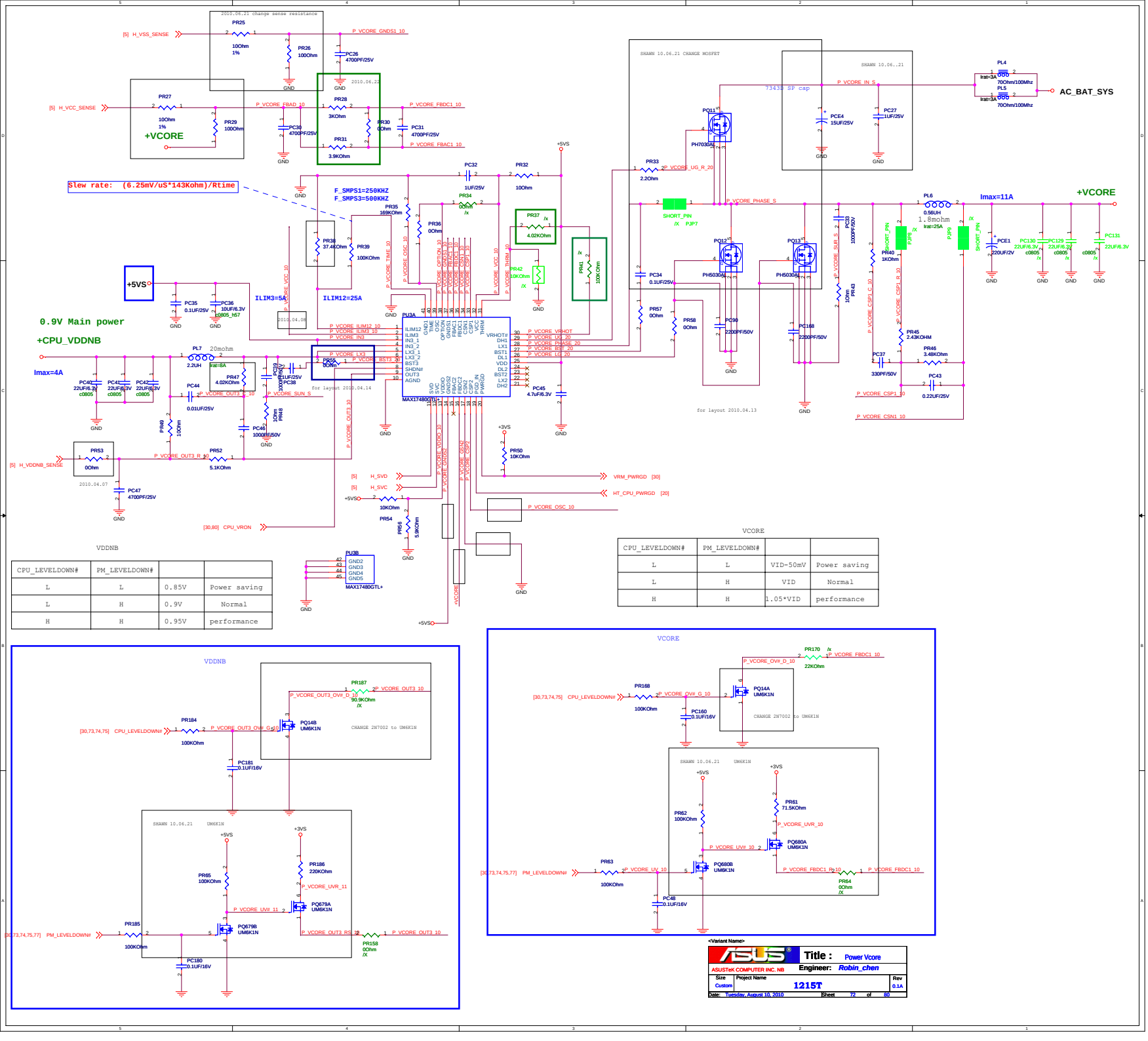
ASUSTek Computer INC

Title : Charger

Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.1

Date: Tuesday, August 10, 2010 Sheet 71 of 80



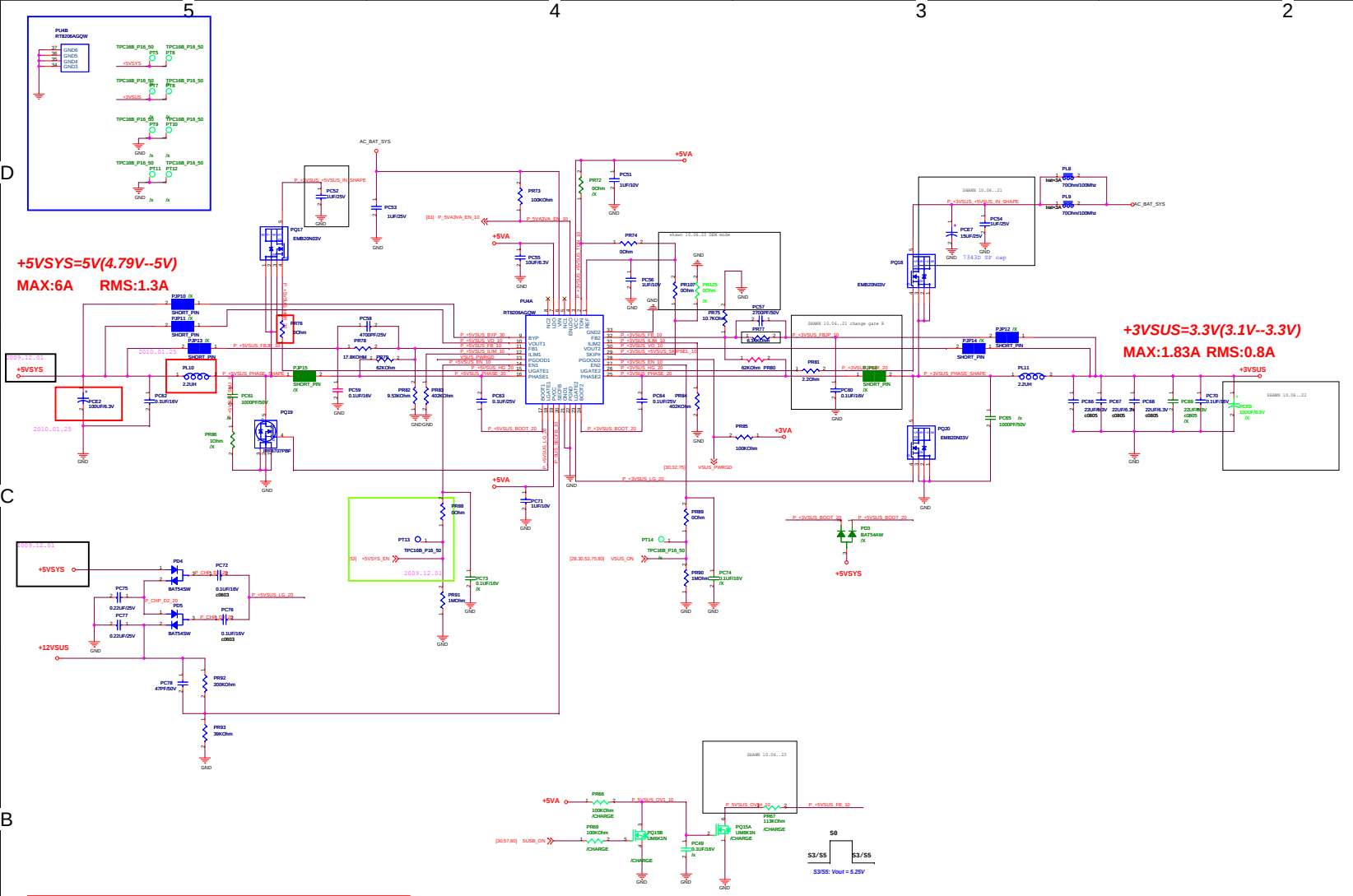
CPU_LEVELDOWN#	PM_LEVELDOWN#		
L	L	0.85V	Power saving
L	H	0.9V	Normal
H	H	0.95V	performance

VDDNB

CPU_LEVELDOWN#	PM_LEVELDOWN#		
L	L	VID-50mV	Power saving
L	H	VID	Normal
H	H	1.05*VID	performance

VCORE

<Variant Name>			
ASUSTeK COMPUTER INC. NB	Title : Power Vcore		
	Engineer: Robin_chen		
Size: Custom	Project Name: 1215T		Rev: 0.1A
Date: Tuesday, August 10, 2010	Sheet 72 of 80		



Power Info. +5VSUS

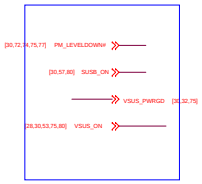
1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =2.082A
2. Ripple Current:
   I rip =1.482A
   I spec=2.5A
   ⊙1 pcs
3. Frequency:
   fosc=300KHz
4. OCP:
   locp=17A

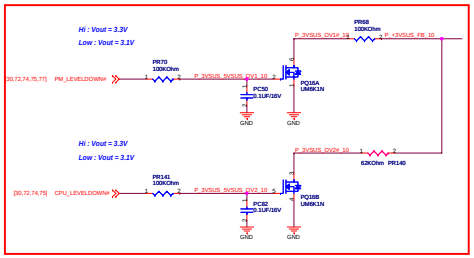
Power Info. +3VSUS

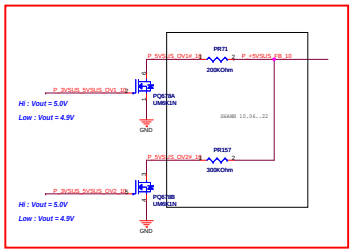
1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.832A
2. Ripple Current:
   I rip =1.92A
   I spec=2.5A
   ⊙1 pcs
3. Frequency:
   fosc=375KHz
4. OCP:
   locp=8.74A

Power Info. +3VA

1. Dropout Voltage:
   〉V= 210mV (Io=300m A)
2. Current Limit:
   I limit= 480mA
3. Pd:
   R thjc =5 C/W
   Pd =0.4W

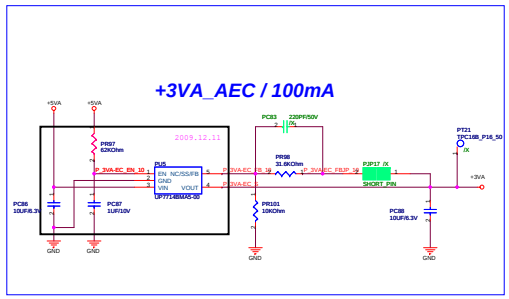






PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	4.8	Power Saving
H	L	5.0	Normal
H	H	5.2	Performance

PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	3.15	Power Saving
H	L	3.30	Normal
H	H	3.45	Performance



ASUSTeK Computer INC

Title : Power_+5SUS&+3VSUS&+12VS

Engineer: N/A

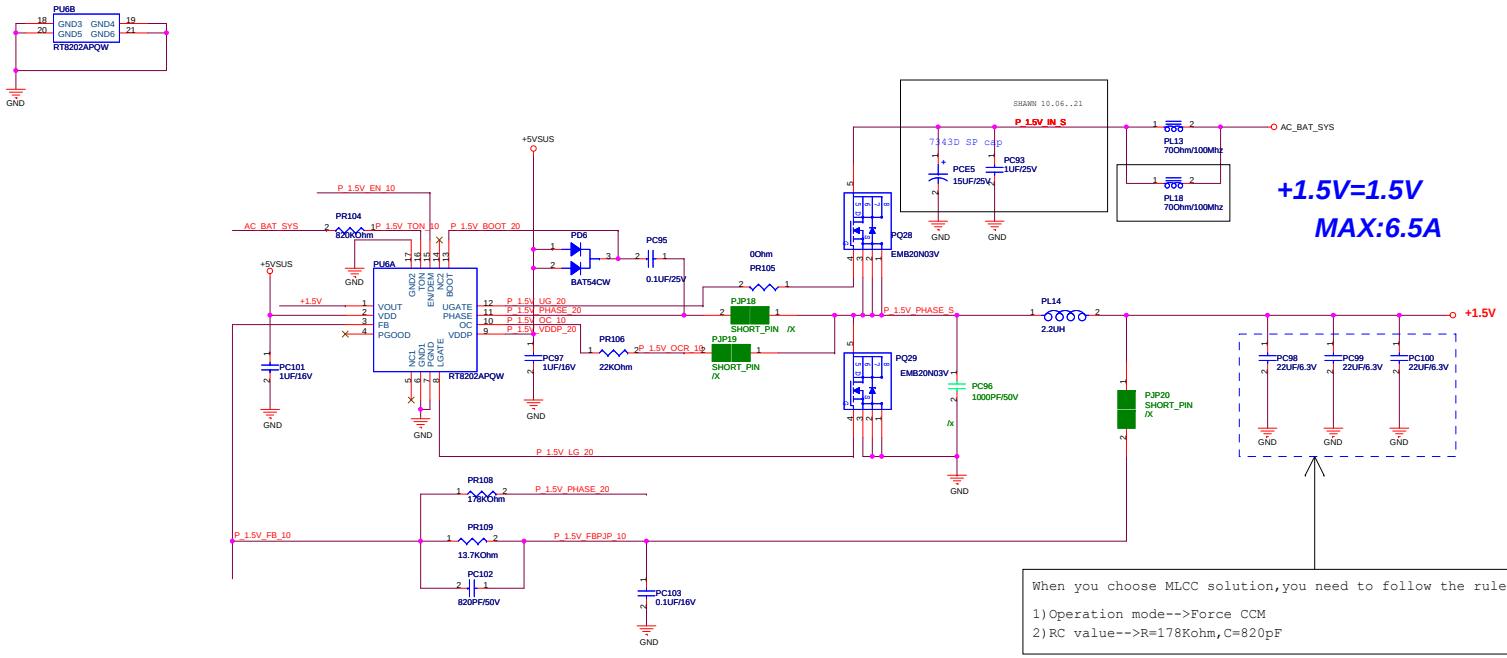
Size A1 | Project Name 1215T | Rev 2.0

Date: Tuesday, August 10, 2010 | Sheet 73 of 80

Power Info.

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =0.825A
2. Ripple Current:
   I rip =1.32A
   I spec=2.5A *
3. Dynamic:
   I peak=3.3A
   ESR=18 mohm
   〉V =59.4mV
4. Frequence
   Fosc=300KHz
5. OCP:
   6.45A

+1.5V=1.5V
MAX:6.5A

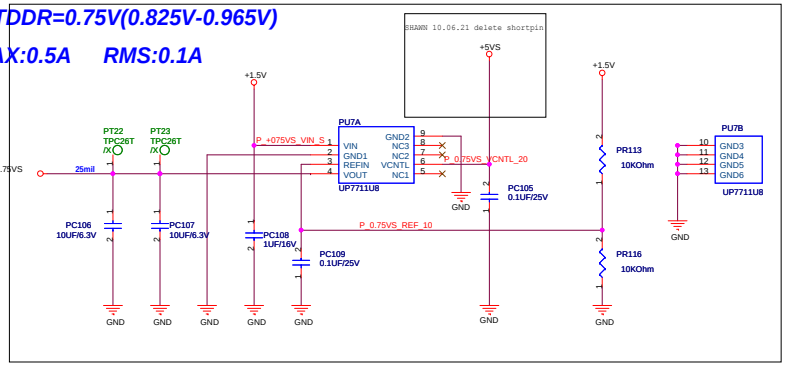


When you choose MLCC solution,you need to follow the rule:

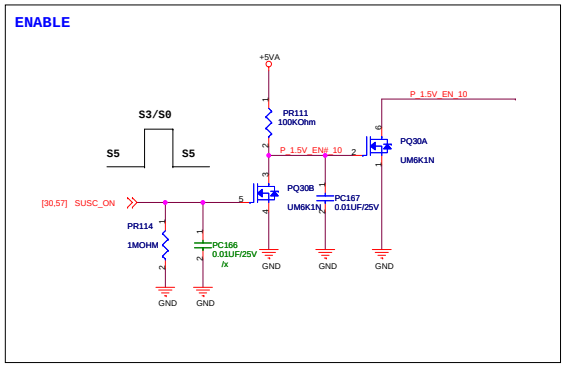
1)Operation mode-->Force CCM
2)RC value-->R=178Kohm,C=820pF

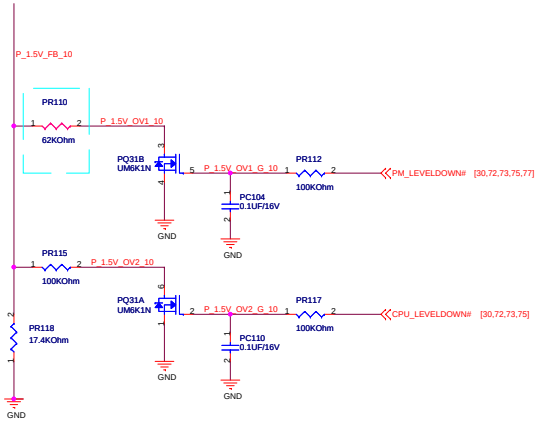
PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	1.4V	Power Saving
H	L	1.5V	Normal
H	H	1.6V	Performance

+VTTDDR=0.75V(0.825V-0.965V)
MAX:0.5A RMS:0.1A



ENABLE





<Variant Name>

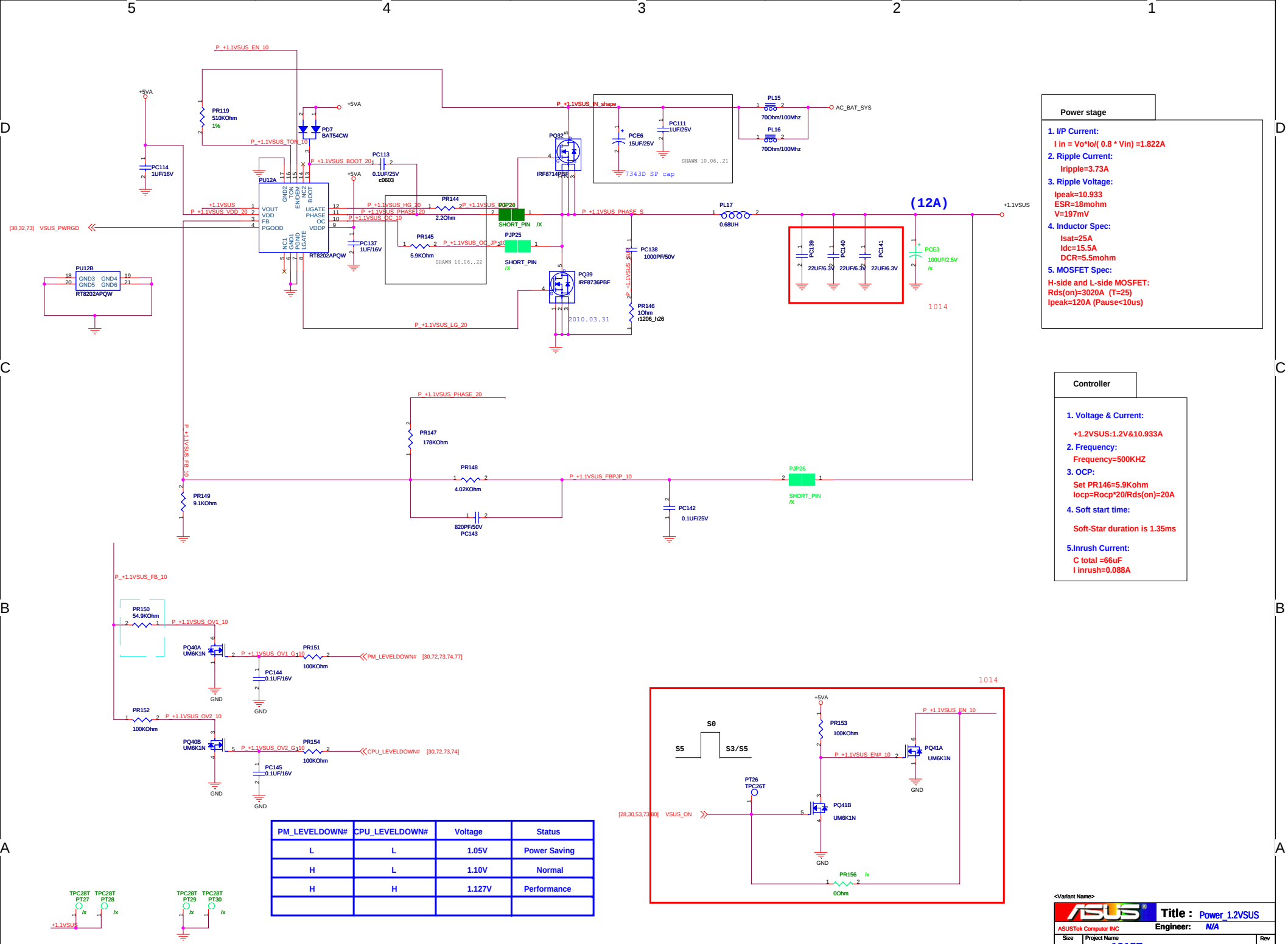
ASUSTek Computer INC

Title : +1.8V&VTTDDR

Engineer: N/A

Size	Project Name	Rev
A2	1215T	1.1

Date: Tuesday, August 10, 2010 Sheet 74 of 80



Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.822A
2. Ripple Current:
   Iripple=3.73A
3. Ripple Voltage:
   Ipeak=10.933
   ESR=18mohm
   V=197mV
4. Inductor Spec:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
5. MOSFET Spec:

H-side and L-side MOSFET:
Rds(on)=3020A (T=25)
Ipeak=120A (Pause<10us)

Controller

1. Voltage & Current:
   +1.2VSUS:1.2V&10.933A
2. Frequency:
   Frequency=500KHZ
3. OCP:
   Set PR146=5.9Kohm
   Iocp=Rocp*20/Rds(on)=20A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =66uF
   I inrush=0.088A

PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	1.05V	Power Saving
H	L	1.10V	Normal
H	H	1.127V	Performance

<Variant Name>

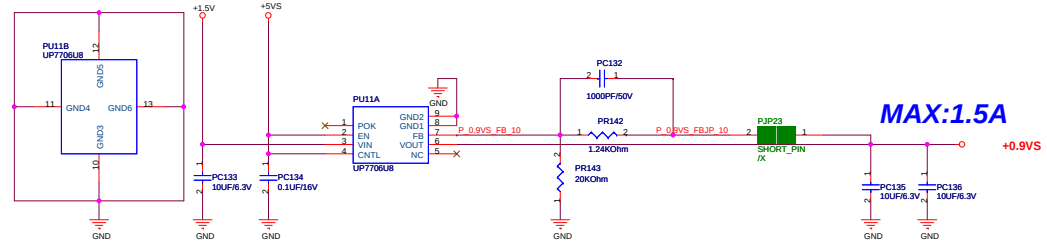
ASUSTek Computer INC

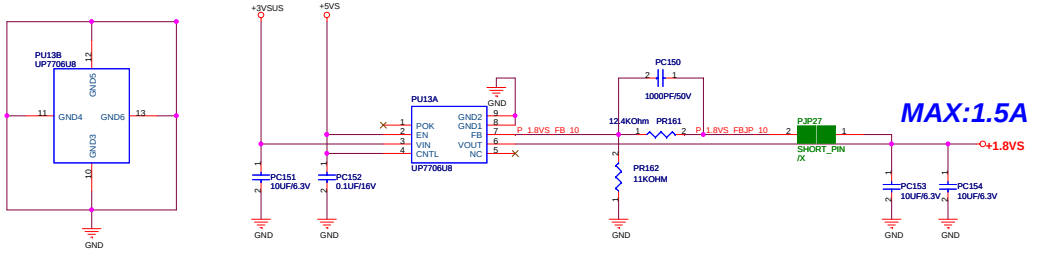
Title : Power_1.2VSUS

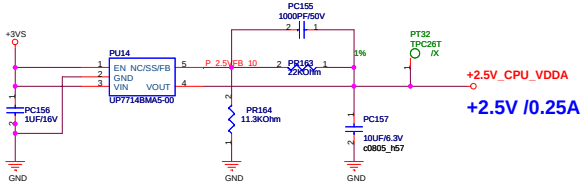
Engineer: N/A

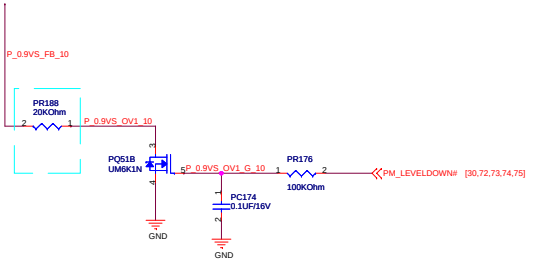
Size	Project Name	Rev
C	1215T	1.1

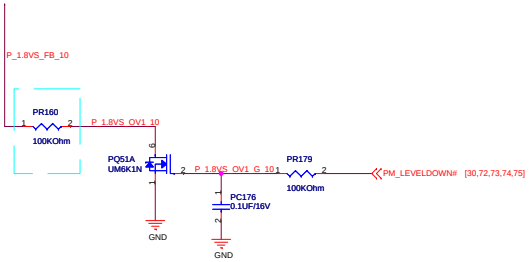
Date: Tuesday, August 10, 2010 Sheet 75 of 80











1. Dropout Voltage:
   〉 V= 300 mV (Io=2 A)
2. Current Limit:
   I limit= 2.8 A
3. Continue Current:
   I cont= 1A
4. Pd:
   R thjc =5 C/W
   Pd =1.9W
5. EN Voltage:
   V rising = 1.4 V
   V falling = 0.4 V
6. Supply Voltage:
   Vcc=5V
7. Inrush current:
   Tss = 4 ms
   C total = 20 uF
   I inrush= 7.5mA

+0.9VS

PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	0.85V	Power Saving
H	L	0.9V	Normal
H	H	0.95V	Performance

+1.8VS

PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	1.7V	Power Saving
H	L	1.8V	Normal
H	H	1.9V	Performance

2.5V @ 0.25A

1. Dropout Voltage:
   〉 V = 0.21V (Io =0.3A)
2. Current Limit:
   I limit =320mA
3. Continue Current:
   I cont = 300mA
4. Power Dissipation:
   Rthjc = 250 /W
   Pd = 0.4W
5. EN Voltage:
   V rising = 2V
   V falling = 0.8V
6. Supply Voltage:
   Vcc =3V
7. Inrush current:
   T ss = 400us
   C total =10uF
   I inrush = 0.063A

<Variant Name>

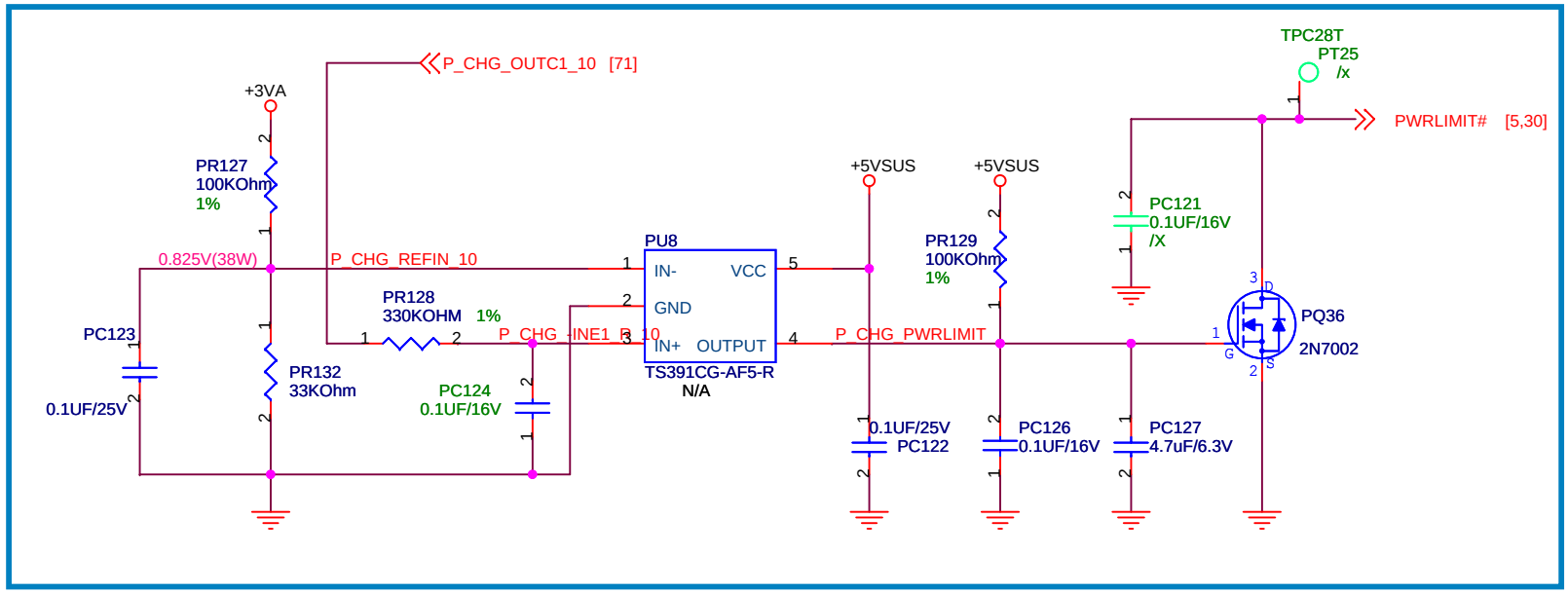
ASUSTek Computer INC

Title : +1.5VS & +2.5VS

Engineer: N/A

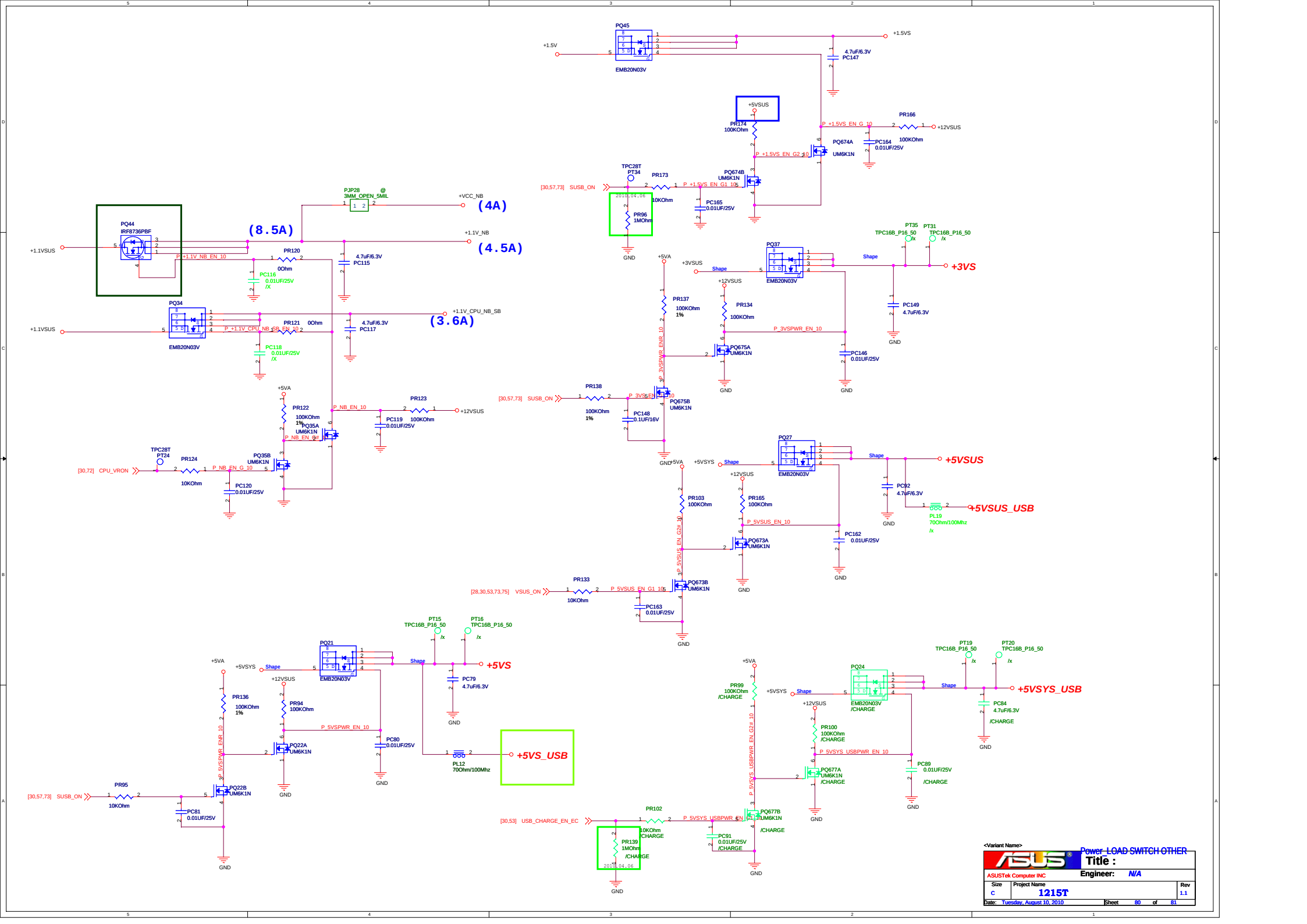
Size	Project Name	Rev
A2	1218T	1.1

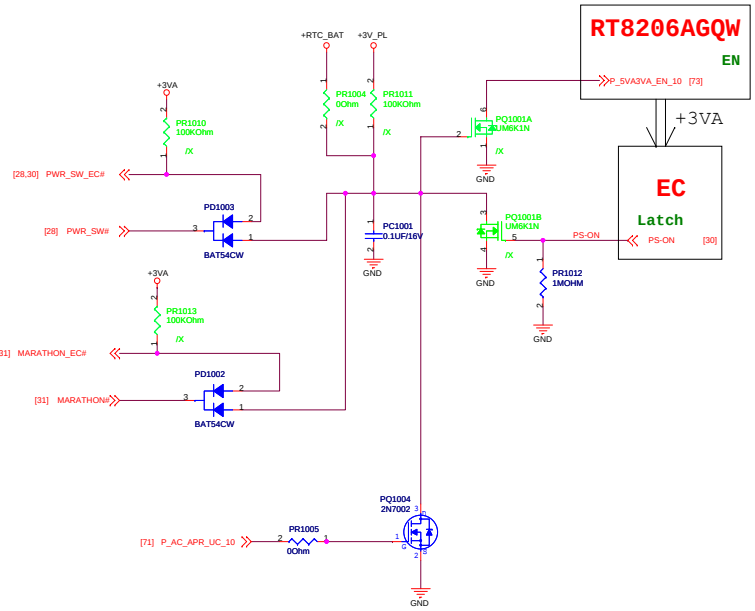
Date: Tuesday, August 10, 2010 Sheet 77 of 80

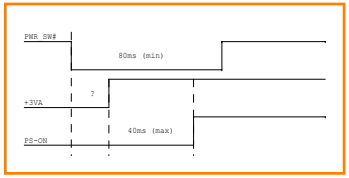


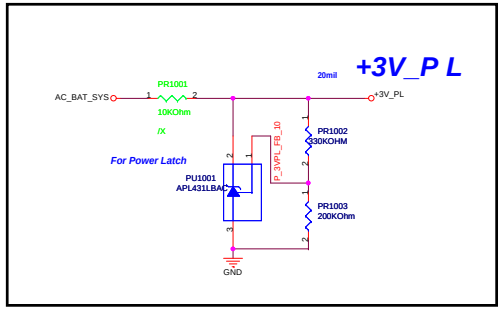
<Variant Name>

ASUSTek Computer INC	Title : Power Lim	
	Engineer: N/A	
Size: A4	Project Name: 1215T	Rev: 1.1
Date: Tuesday, August 10, 2010	Sheet 79 of 80	


PQ45
EMB20N03V
+1.5V
+1.5VS
4.7uF/6.3V
PC147
+5VSUS
PR174
100KOhm
P_+1.5VS_EN_G_10
PR166
+12VSUS
PQ674A
UM6K1N
PC164
100KOhm
0.01UF/25V
P_+1.5VS_EN_G2_10
TPC28T
PT34
PR173
[30,57,73] SUSB_ON
2010.04.06
10KOhm
PQ674B
UM6K1N
P_+1.5VS_EN_G1_10
PC165
0.01UF/25V
PR96
1MOhm
GND
PJP28
3MM_OPEN_5MIL
+VCC_NB
(4A)
PQ44
IRF8736PBF
(8.5A)
+1.1VSUS
+1.1V_NB
(4.5A)
P_+1.1V_NB_EN_10
PR120
0Ohm
4.7uF/6.3V
PC115
PC116
0.01UF/25V
/X
PQ34
EMB20N03V
PR121
0Ohm
+1.1V_CPU_NB_SB
(3.6A)
P_+1.1V_CPU_NB_SB_EN_10
4.7uF/6.3V
PC117
PC118
0.01UF/25V
/X
PT35
TPC16B_P16_50
/X
PT31
TPC16B_P16_50
/X
+3VS
PQ37
Shape
+3VSUS
+12VSUS
PR137
100KOhm
1%
PR134
100KOhm
P_3VSPWR_EN_10
P_3VSPWR_ENR_10
PQ675A
UM6K1N
PC149
4.7uF/6.3V
PC146
0.01UF/25V
+5VA
PR122
100KOhm
1%
PQ35A
UM6K1N
P_NB_EN_10
PR123
+12VSUS
PC119
100KOhm
0.01UF/25V
TPC28T
PT24
[30,72] CPU_VRON
PR124
10KOhm
P_NB_EN_G_10
PQ35B
UM6K1N
PC120
0.01UF/25V
[30,57,73] SUSB_ON
PR138
100KOhm
1%
P_3VSEN_10
PQ675B
UM6K1N
PC148
0.1UF/16V
PQ27
EMB20N03V
+5VSYS
+5VSUS
PC92
4.7uF/6.3V
+5VSUS_USB
PL19
70Ohm/100Mhz
/X
PR103
100KOhm
PR165
100KOhm
P_5VSUS_EN_10
P_5VSUS_EN_G2#_10
PQ673A
UM6K1N
PC162
0.01UF/25V
[28,30,53,73,75] VSUS_ON
PR133
10KOhm
P_5VSUS_EN_G1_10
PQ673B
UM6K1N
PC163
0.01UF/25V
PT15
TPC16B_P16_50
/X
PT16
TPC16B_P16_50
/X
PQ21
EMB20N03V
+5VS
PC79
4.7uF/6.3V
PR136
100KOhm
1%
PR94
100KOhm
P_5VSPWR_EN_10
P_5VSPWR_ENR_10
PQ22A
UM6K1N
PC80
0.01UF/25V
PL12
70Ohm/100Mhz
+5VS_USB
[30,57,73] SUSB_ON
PR95
10KOhm
PQ22B
UM6K1N
PC81
0.01UF/25V
PR99
100KOhm
/CHARGE
PQ24
EMB20N03V
/CHARGE
PT19
TPC16B_P16_50
/X
PT20
TPC16B_P16_50
/X
+5VSYS_USB
PC84
4.7uF/6.3V
/CHARGE
PR100
100KOhm
/CHARGE
P_5VSYS_USBPWR_EN_10
P_5VSYS_USBPWR_EN_G2#_10
PQ677A
UM6K1N
/CHARGE
PC89
0.01UF/25V
/CHARGE
[30,53] USB_CHARGE_EN_EC
PR102
10KOhm
/CHARGE
P_5VSYS_USBPWR_EN
PQ677B
UM6K1N
/CHARGE
PR139
1MOhm
/CHARGE
PC91
0.01UF/25V
/CHARGE
2010.04.06
<Variant Name>
Power_LOAD SWITCH OTHER
Title :
ASUSTek Computer INC
Engineer: N/A
Size C
Project Name 1215T
Rev 1.1
Date: Tuesday, August 10, 2010
Sheet 80 of 81



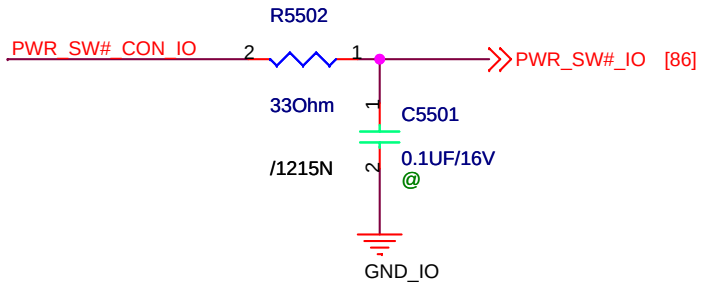


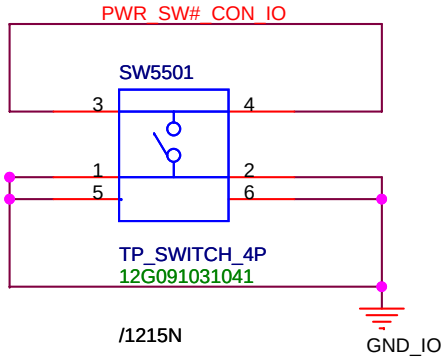


<variant_name>

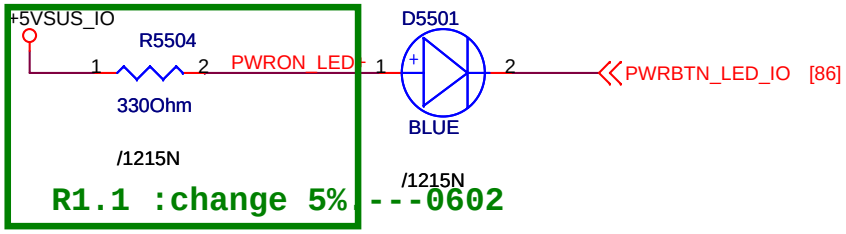
ASUSTek Computer INC	Title : Power Lim	
	Engineer: N/A	
Size: A2	Project Name: 1015T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 81 of 82	

PWR SW





For POWER ON LED



0521:change +5V_USB_IO to +5VSUS_IO

ASUSTEK COMPUTER INC	Title : PWR_BUTTON_LED	
	Engineer: Anndy_wang	
Size: A	Project Name: 1215N_IO	Rev: 1.3
Date: Tuesday, August 10, 2010	Sheet 82 of 92	

R1.7 ALC269-VB2 Issue
PD# is internal pull-up to 5VS_AUDIO & VIH=3.3V
Add R3602 &R3613 of PD# to make sure the PD# is higher than 3.3V when power up speaker amplifier

269VA USE 0 ohm/0603

[84] DLY_OP_SD# — R3613 10KOhm /269_VB2 — R3612 10KOhm /269_VB2 — Q3601 PMBS3904 — R3614 0Ohm /269_VA/269_VB5 — DLY_OP_SD#_R

DLY_OP_SD# "L" ==> PD# = 0.37V"H" ==> PD# = 3.55V

DVDD_IO — C3612 0.1UF/16V — C3611 10UF/10V — GND_IO

+5VS_AMP_IO — L3601 80Ohm/100Mhz — +5VS_IO

C3619 10UF/10V — C3620 1UF/10V — C3621 0.1UF/16V — GND_IO

5/26

269_VA 02G611005006
269_VB 02G611005010
269_VB5 02G611005015

6/29 DesignIP R1.3

+5VS_IO — R3609 0Ohm /269_VB — +5VS_AUDIO_IO

D3601 AZ2015-01H.R7F

U3601 UP7714BMT5-00 — EN NC/SS/FB GND VIN VOUT — Vref = 0.8V

C3606 1UF/16V c0603 /269_VA — C3622 100PF/50V /269_VA — R3605 49.9KOhm 1% — +5VS_AUDIO_SENSE — R3602 10KOhm 1% /269_VA — C3607 1UF/16V c0603 /269_VA — R3622 0Ohm /269_VA — GND_AUDIO_IO

UP7714BMT5-00 (P/N:06G029330020)
Vout=0.8*(1+(49.9K/10K))
=4.792V

EMI 07/03

+3VS_IO — JP3602 SGL_JUMP — +1.5VS_IO — JP3601 SGL_JUMP

C3625 0.1UF/16V — C3604 0.1UF/16V — C3605 10UF/10V — GND_IO

JP3603 SGL_JUMP — [84] EAPD — DVDD_IO

H_SPKR+ — H_SPKR- — H_SPKL- — H_SPKL+ — H_SPKR+ [84] — H_SPKR- [84] — H_SPKL- [84] — H_SPKL+ [84]

+5VS_AUDIO_IO — C3602 0.1UF/16V — C3603 0.1UF/16V — GND_AUDIO_IO

U3602B — GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 — ALC269Q-VA6-GR

U3602A — GND SPDIFO EAPD/SPDIFO2 PVDD2 SPK_OUT_R- SPK_OUT_R+ PVSSR SPK_OUT_L- SPK_OUT_L+ PVDD1 AVDD AVSS

DVDD GPIO0/DMIC_DATA GPIO1/DMIC_CLK PD# SDATA_OUT BCLK DVSS SDATA_IN DVDD_IO SYNC RESET# BEEP

[86] AZ_DMIC_DATA_IO — R3615 20Ohm — AZ_DMIC_DATA_IO_R
[86] AZ_DMIC_CLK_IO — R3616 20Ohm — AZ_DMIC_CLK_IO_R
DLY_OP_SD#_R
[86] AZ_SDOUT_AUD_IO
[86] AZ_BCLK_AUD_IO
[86] AZ_SDIN0_AUD_IO — R3604 33Ohm — AZ_SDIN0_AUD_IO_R
[86] AZ_SYNC_AUD_IO
[84,86] AZ_RST#_AUD_IO
T3605 PC_BEEP — TPC26T — GND_IO

Place R3606 near U3602

Digital

GND
GND_AUDIO

CBP CBN CPVEE HPOUT_R HPOUT_L CPVREF MIC1_VREFO_R MIC2_VREFO MIC1_VREFO_L VREF AVSS AVDD

C3617 2.2UF/10V — CPVEE — AC_HP_R — AC_HP_L — AC_HP_R [84] — AC_HP_L [84]
MIC_VREFOUT_L — MIC1_VREFOUT_R — MIC2_VREFOUT — LDO_CAP — VREF_CODEC — MIC1_VREFOUT_R [84]

C3618 2.2UF/10V — C3615 1UF/10V — C6719 10UF/10V — @

T3601 — +5VS_AUDIO_IO — C3608 10UF/10V — C3609 0.1UF/16V — GND_AUDIO_IO

ALC269Q-VA6-GR

For VIA VT1802P
C3627 C3628 Change to 2.2UF/10V (P/N 11G233322536360)

For VIA VT1802P
C3615 Change to 0.1uF (P/N 11G233310432340)
C3608 may improve the audio performance

R1.5 Co-lay for 269_VB

MIC_VREFOUT_L — R3606 0Ohm /269_VB — MIC1_VREFOUT_L [84]
R3611 0Ohm /269_VA — GND_AUDIO_IO
LDO_CAP — R3610 0Ohm /269_VA — MIC1_VREFOUT_L
C3624 10UF/10V /269_VB — GND_AUDIO_IO

[84] MIC1_JD — R3607 20KOhm
[84] LINE2_JD — R3603 39.2KOhm
MIC2_VREFOUT — C3626 1UF/10V — GND_AUDIO_IO
R3608 0Ohm /269_VA

AZ_DMIC_DATA_IO — R3617 0Ohm — AZ_DMIC_DATA_IO_RA
C3627 1UF/10V c0603 @ — INTMIC_L
C3628 1UF/10V c0603 @ — INTMIC_R
GND_AUDIO_IO

R3601 20KOhm — C6717 100PF/50V @

MONO_OUT — JDREF

For VIA VT1802P
R3601 Change to 5.1Kohm (P/N 10G2125101140030)

T3602
[84] MIC_IN_AC_E — TPC26T — 2.2UF/10V — C3613 — MIC_IN_AC_E_L
[84] MIC_IN_AC_R_E — 2.2UF/10V — C3614 — MIC_IN_AC_E_R

RealTek recommend change C3615 from 2.2uF to 1uF
New project — Please use the 1uF for VREF_CODEC
On going project — Please keep 2.2uF for VREF_CODEC if speaker have not S3 S4 resume issue.

For EMI — EMI 05/26

R3618 0Ohm
R3619 0Ohm
R3620 0Ohm
R3621 0Ohm
C3630 100PF/50V
R3623 0Ohm
GND_IO — GND_AUDIO_IO

EMI 05/26

AZ_BCLK_AUD_IO — C3623 10PF/50V @ — GND_IO
06/19 remove PC beep

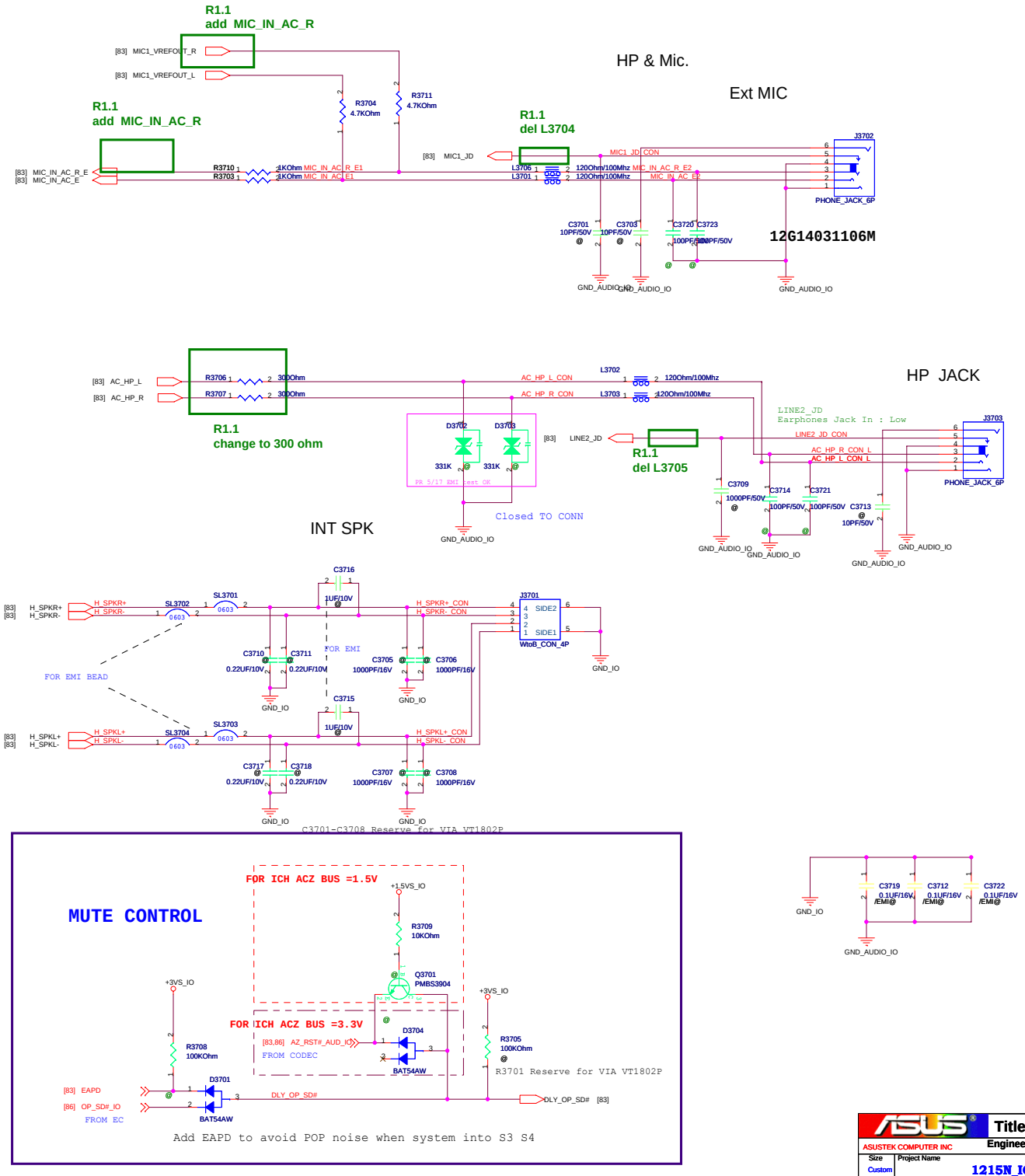
AZ_DMIC_CLK_IO_R — C3629 0.1UF/16V @/EMI — GND_IO

For VIA VT1802P
Please reserve 11G232022004320 for AC2_BCLK_AUD at PCH (SB) side

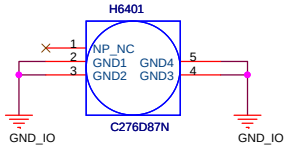
<Variant Name>

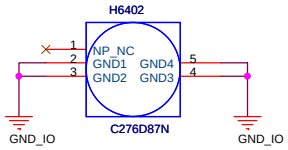
ASUSTEK COMPUTER INC

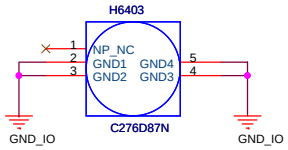
Title : ALC269-1
Engineer: Anndy_wang
Size: C | Project Name: 1215N_IO | Rev: 1.3
Date: Tuesday, August 10, 2010 | Sheet 83 of 92



ASUSTEK COMPUTER INC	Title : ALC269-2 (I/O)		
	Engineer: Anndy_wang		
Size: Custom	Project Name: 1215N_IO		Rev: 1.3
Date: Tuesday, August 10, 2010	Sheet 84 of 92		



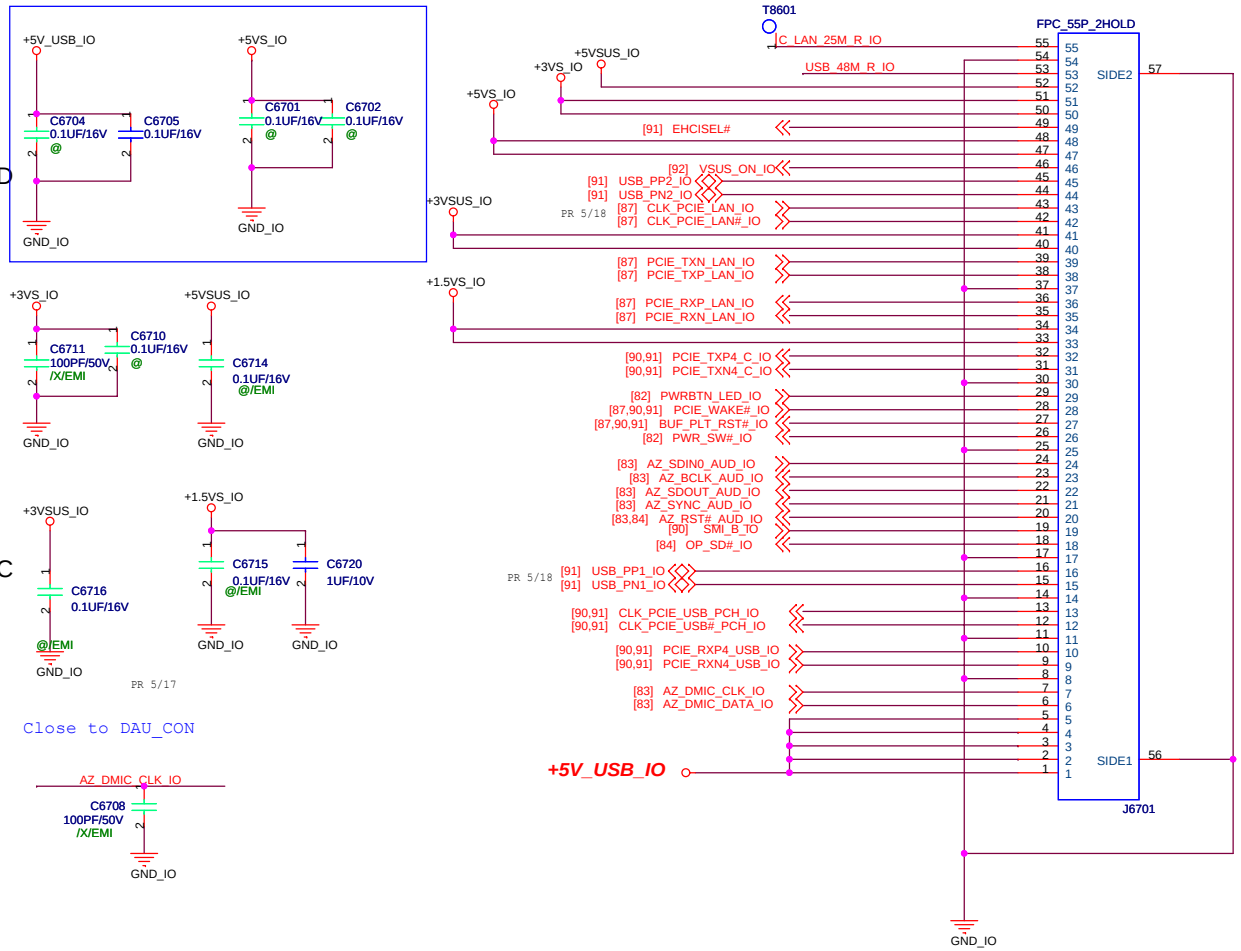




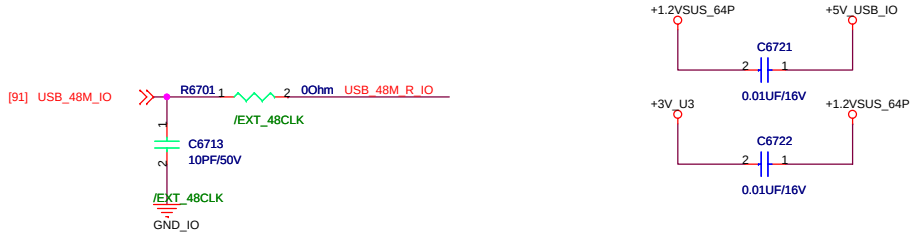




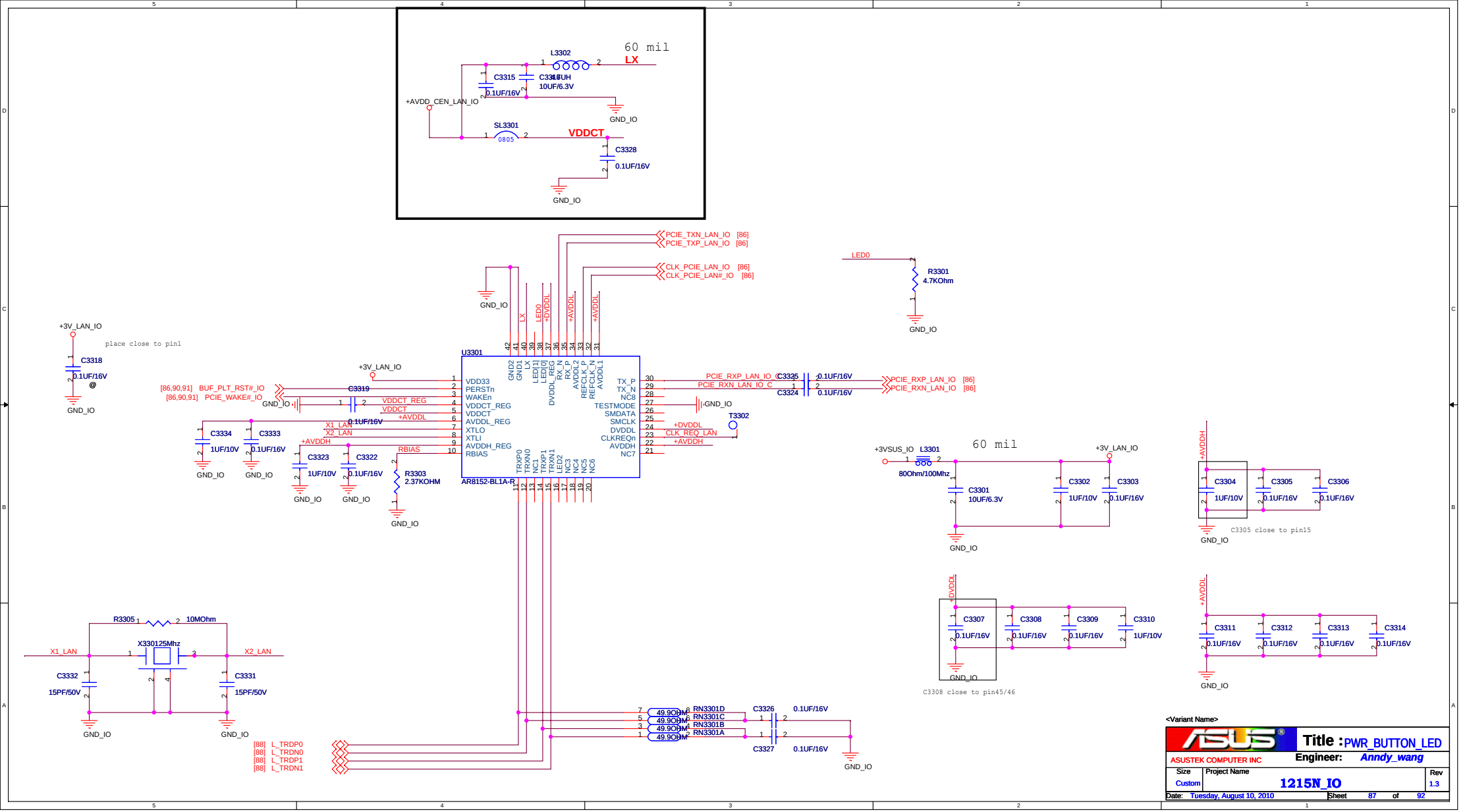
ASUSTEK COMPUTER INC	Title : Srew Hole	
	Engineer: Anndy_wang	
Size: A3	Project Name: 1215N_IO	Rev: 1.3
Date: Tuesday, August 10, 2010	Sheet 85 of 92	

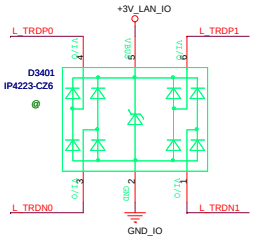


0524: remove 25CLK from MB

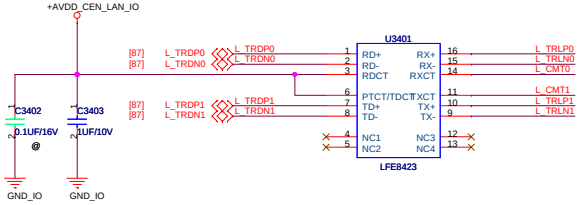


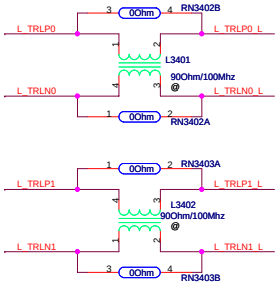
ASUSTEK COMPUTER INC	Title : USB Port	
	Engineer: Anndy_wang	
Size: A3	Project Name: 1215N_IO	Rev: 1.3
Date: Tuesday, August 10, 2010	Sheet 86 of 92	

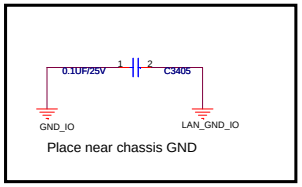

60 mil
L3302
LX
C3315
0.1UF/16V
10UF/6.3V
+AVDD_CEN_LAN_IO
GND_IO
SL3301
0805
VDDCT
C3328
0.1UF/16V
PCIE_TXN_LAN_IO [86]
PCIE_TXP_LAN_IO [86]
CLK_PCIE_LAN_IO [86]
CLK_PCIE_LAN#_IO [86]
LED0
R3301
4.7KOhm
+3V_LAN_IO
place close to pin1
C3318
0.1UF/16V
@
U3301
AR8152-BL1A-R
VDD33
PERSTn
WAKEn
VDDCT_REG
VDDCT
AVDDL_REG
XTLO
XTLI
AVDDH_REG
RBIAS
TX_P
TX_N
NC8
TESTMODE
SMDATA
SMCLK
DVDDL
CLKREQn
AVDDH
NC7
[86,90,91] BUF_PLT_RST#_IO
[86,90,91] PCIE_WAKE#_IO
C3319
VDDCT_REG
VDDCT
+AVDDL
X1_LAN
X2_LAN
+AVDDH
RBIAS
C3334
C3333
C3323
C3322
1UF/10V
0.1UF/16V
R3303
2.37KOHM
PCIE_RXP_LAN_IO_C
PCIE_RXN_LAN_IO_C
C3325
C3324
PCIE_RXP_LAN_IO [86]
PCIE_RXN_LAN_IO [86]
T3302
CLK_REQ_LAN
+DVDDL
+3VSUS_IO
L3301
80Ohm/100Mhz
C3301
10UF/6.3V
C3302
C3303
C3304
C3305
C3306
C3305 close to pin15
C3307
C3308
C3309
C3310
C3311
C3312
C3313
C3314
C3308 close to pin45/46
R3305
10MOhm
X330125Mhz
X1_LAN
X2_LAN
C3332
C3331
15PF/50V
RN3301D
RN3301C
RN3301B
RN3301A
49.9OHM
C3326
C3327
[88] L_TRDP0
[88] L_TRDN0
[88] L_TRDP1
[88] L_TRDN1
<Variant Name>
Title : PWR_BUTTON_LED
ASUSTEK COMPUTER INC
Engineer: Anndy_wang
Size Custom
Project Name 1215N_IO
Rev 1.3
Date: Tuesday, August 10, 2010
Sheet 87 of 92

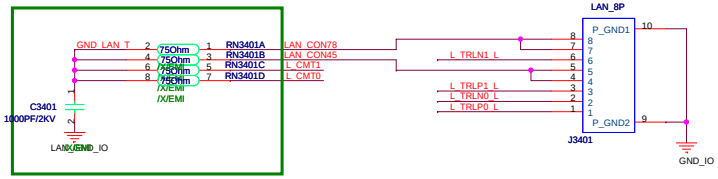


GND_LAN_T 竅わ ヴ：築ン





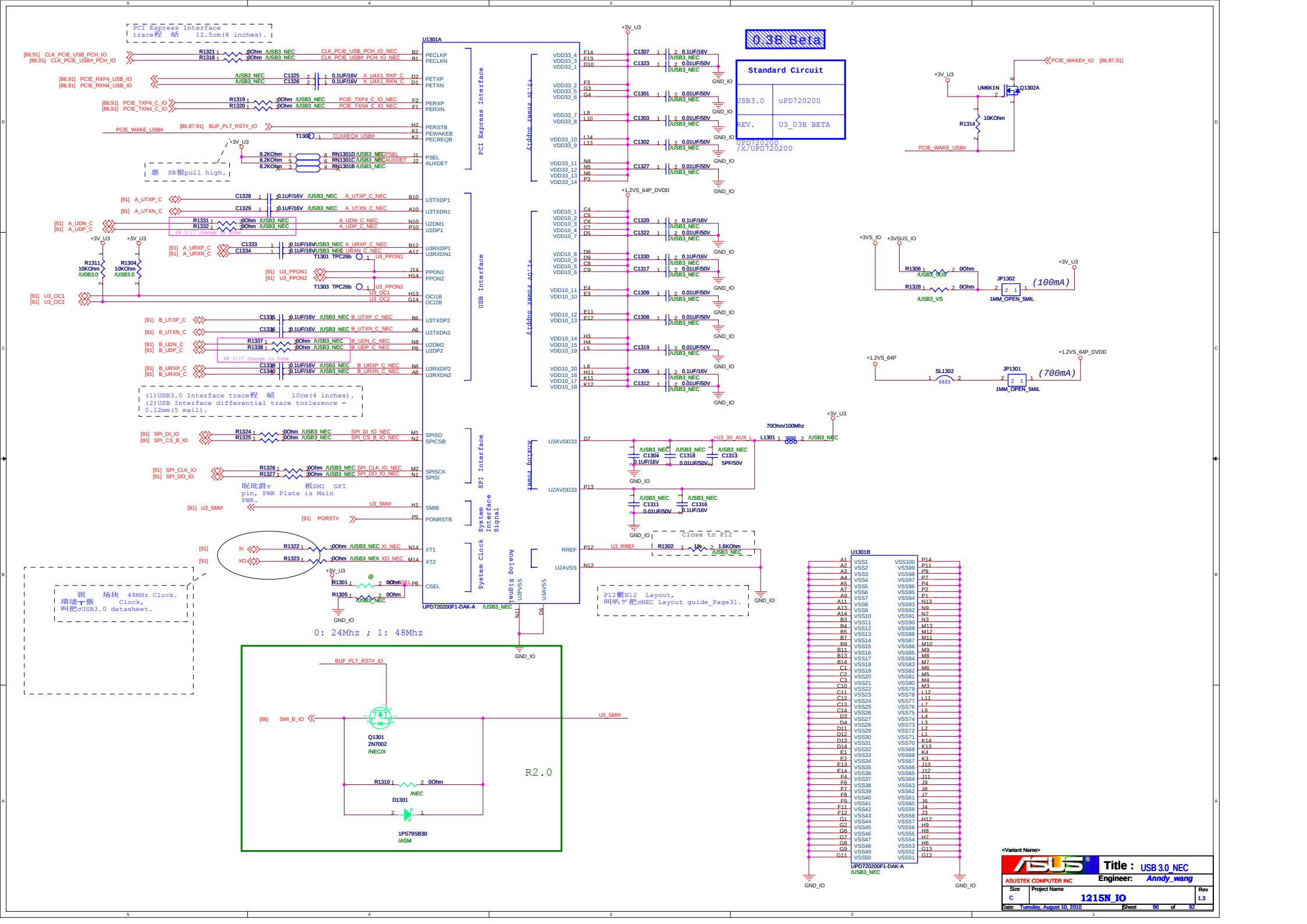




R1.1 EMI

ASUSTEK COMPUTER INC	Title : PWR_BUTTON_LED		
	Engineer: Anndy_wang		
Size: C	Project Name: 1215N_IO		Rev: 1.3
Date: Tuesday, August 10, 2010	Sheet 88 of 92		

ASUSTEK COMPUTER INC	Title : EMI		
	Engineer: Anndy_wang		
Size A3	Project Name 1215N_IO		Rev 1.3
Date: Tuesday, August 10, 2010	Sheet 89 of 92		



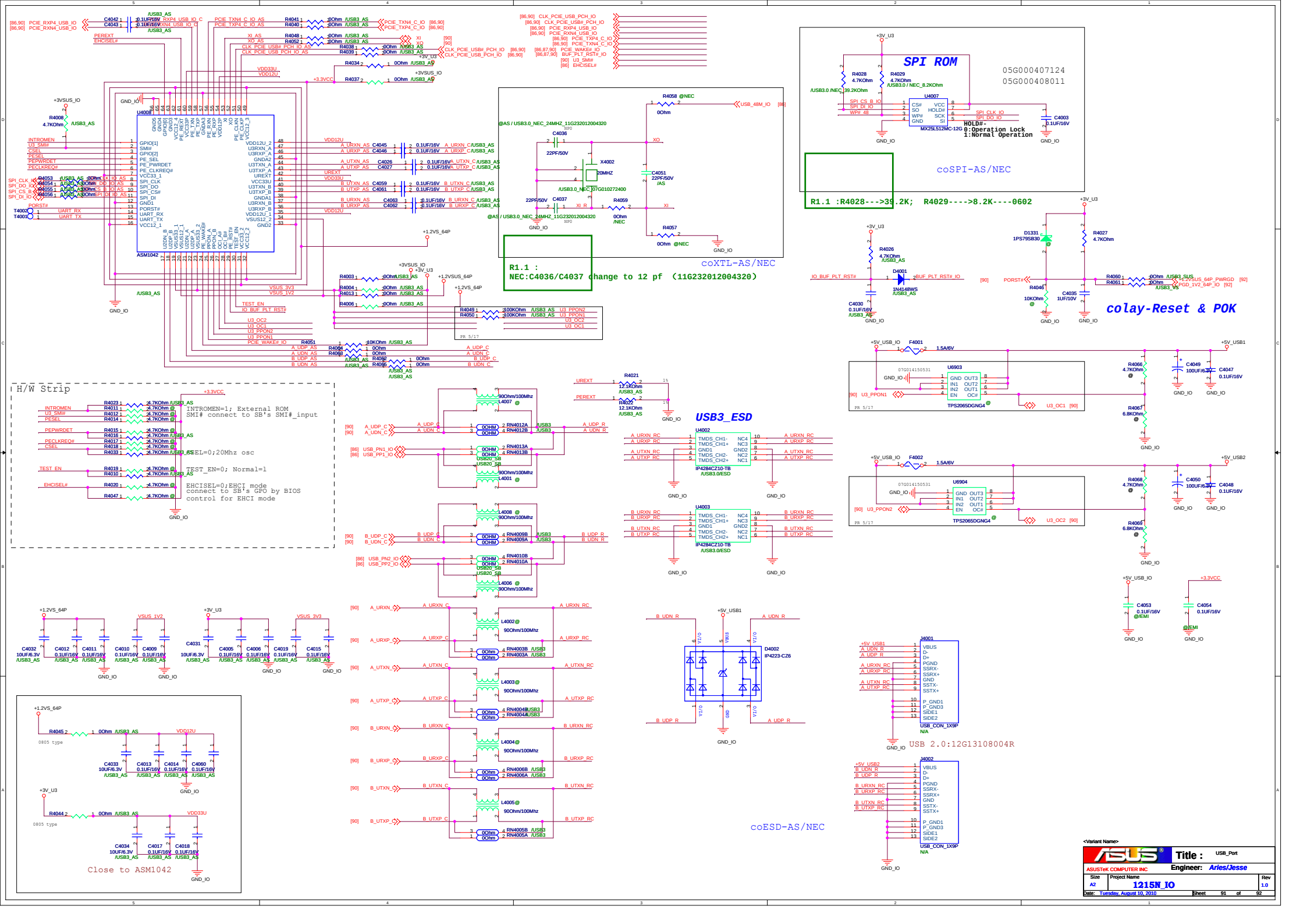
ASUSTEK COMPUTER INC

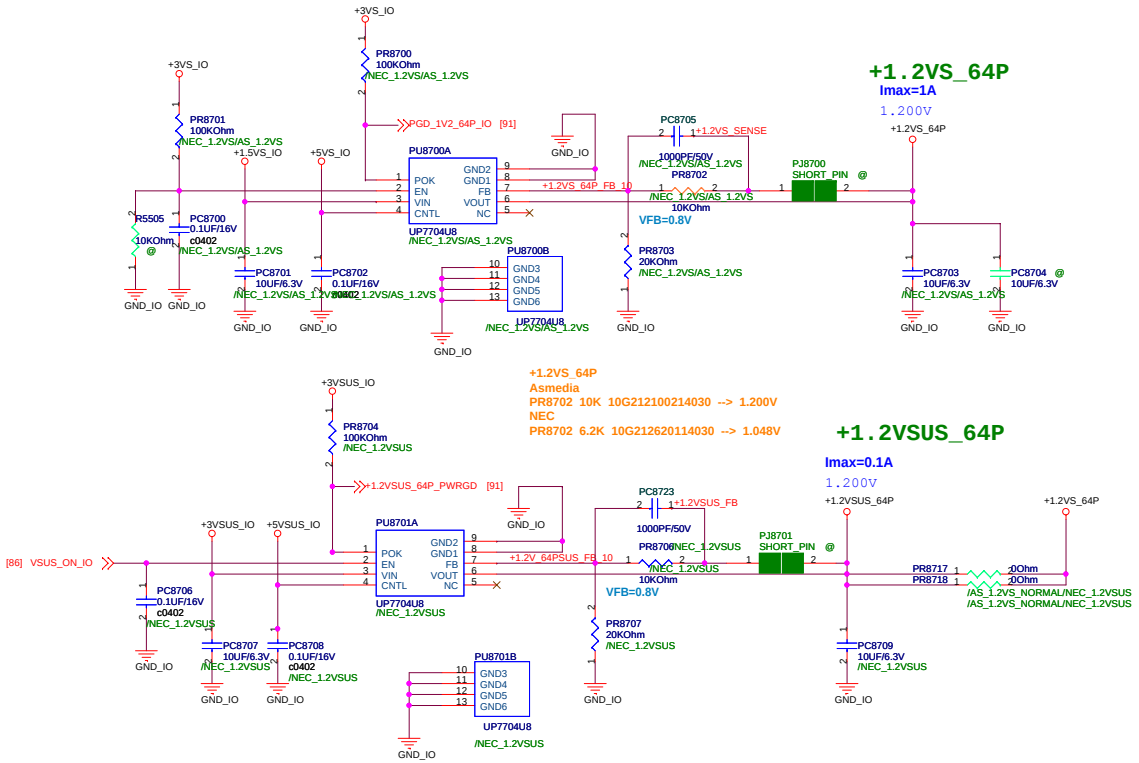
Title : USB 3.0_NEC

Engineer: Anndy_wang

Size	Project Name	Rev
C	1215N_IO	1.3

Date: Tuesday, August 10, 2010 Sheet 90 of 92


SPI ROM
05G000407124
05G000408011
coSPI-AS/NEC
R1.1 :R4028--->39.2K; R4029---->8.2K----0602
colay-Reset & POK
coXTL-AS/NEC
R1.1 :
NEC:C4036/C4037 change to 12 pf (116232012004320)
USB3_ESD
coESD-AS/NEC
USB 2.0:12G13108004R
H/W Strip
INTROMEN=1; External ROM
SMI# connect to SB's SMI#_input
TEST_EN=0; Normal=1
EHCISEL=0;EHCI mode
connect to SB's GPO by BIOS
control for EHCI mode
Close to ASM1042
ASM1042
Title : USB_Port
ASUSTeK COMPUTER INC
Engineer: Aries/Jesse
Project Name 1215N_IO
Rev 1.0
Date: Tuesday, August 10, 2010
Sheet 91 of 92



Dual_layout BOM_table	OPTIONAL CHOICE	Voltage(NEC=1.05V;ASM=1.2V)
NEC (Normal)	/NEC_1.2VS/AS_1.2VS	NEC PR8702 6.2K 10G212620114030 --> 1.048V
NEC(SUS)	/NEC_1.2VSUS	NEC PR8706 6.2K 10G212620114030 --> 1.048V
ASM1042(Normal)	/NEC_1.2VS/AS_1.2VS /AS_1.2VS_ALL NORMAL	Asmedia PR8702 10K 10G212100214030 --> 1.200V
ASM1042(Normal +SUS)	/NEC_1.2VS/AS_1.2VS /NEC_1.2VSUS	Asmedia PR8702 10K 10G212100214030 --> 1.200V Asmedia PR8706 10K 10G212100214030 --> 1.200V

Dual_layout BOM_table	BOM(USB interface)	BOM(PCIE interface)	BOM(XTL interface)	BOM(SPI interface)
ASM only (USB3.0) (USB2.0)	C4045, C4046, C4026, C4027, C4059, C4061, C4062, C4063, C4064, C4065, C4066, C4067, RN4012A, RN4012B	R4038, R4039, R4040, R4041, C4042, C4043	X4002(20MHZ, 07G010012000), @C4036,C4037(22pF,11G232022004030), C4051, R4032, @C4052	R4053, R4054, R4055, R4056, R4028/ R4029 (4.7K, 10G212472004030), C4003, U4007
NEC only (USB3.0) (USB2.0)	C1328, C1329, C1331, C1332, C1333, C1334, C1335, C1336, C1337, C1338, C1339, C1340, RN4012A, RN4012B	R1318, R1319, R1320, R1321, C1325, C1326	X4002(24MHZ,11G232027004070), C4036,C4037(12pF,11G232012004320), @C4051, R1317, @R1315, @R1316	R1324, R1325, R1326, R1327, R4028(8.2K, 10G212822004030), R4029(39.2K, 10G212392214031), C4003, U4007
PCH only (USB2.0)	RN4013A, RN4013B			
ASM+PCH (USB3.0) (USB2.0)	C4045, C4046, C4026, C4027, C4059, C4061, C4062, C4063, C4064, C4065, C4066, C4067, RN4012A, RN4012B, RN4013A, RN4013B	R4038, R4039, R4040, R4041, C4042, C4043		
NEC+PCH (USB3.0) (USB2.0)	C1328, C1329, C1331, C1332, C1333, C1334, C1335, C1336, C1337, C1338, C1339, C1340, RN4012A, RN4012B, RN4013A, RN4013B	R1318, R1319, R1320, R1321, C1325, C1326		

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : N/A

Engineer: Aaron_Lin

Size	Project Name	Rev
Custom	1215N_IO	1.0

Date: Tuesday, August 10, 2010 Sheet 92 of 92

1215N_IO 1.3G

2009_1102_1100

01.Block Diagram
02.PWR_BUTTON_LED
03.ALC269-1
04.ALC269-2(I/O)
05.ALC269-3(I/O)
06.DAU_HDD_CON
07.LAN
08.LAN CONN.
09.USB3.0_ASM1042
10.USB_Port
11.Srew Hole
12.EMI

ASUSTek Computer INC.	Title : Block Diagram	
	Engineer: ERICH_LEE	
Size: A4	Project Name: 1215N_IO	Rev: 1.3
Date: Tuesday, August 10, 2010	Sheet 93 of 93	

www.s-manuals.com