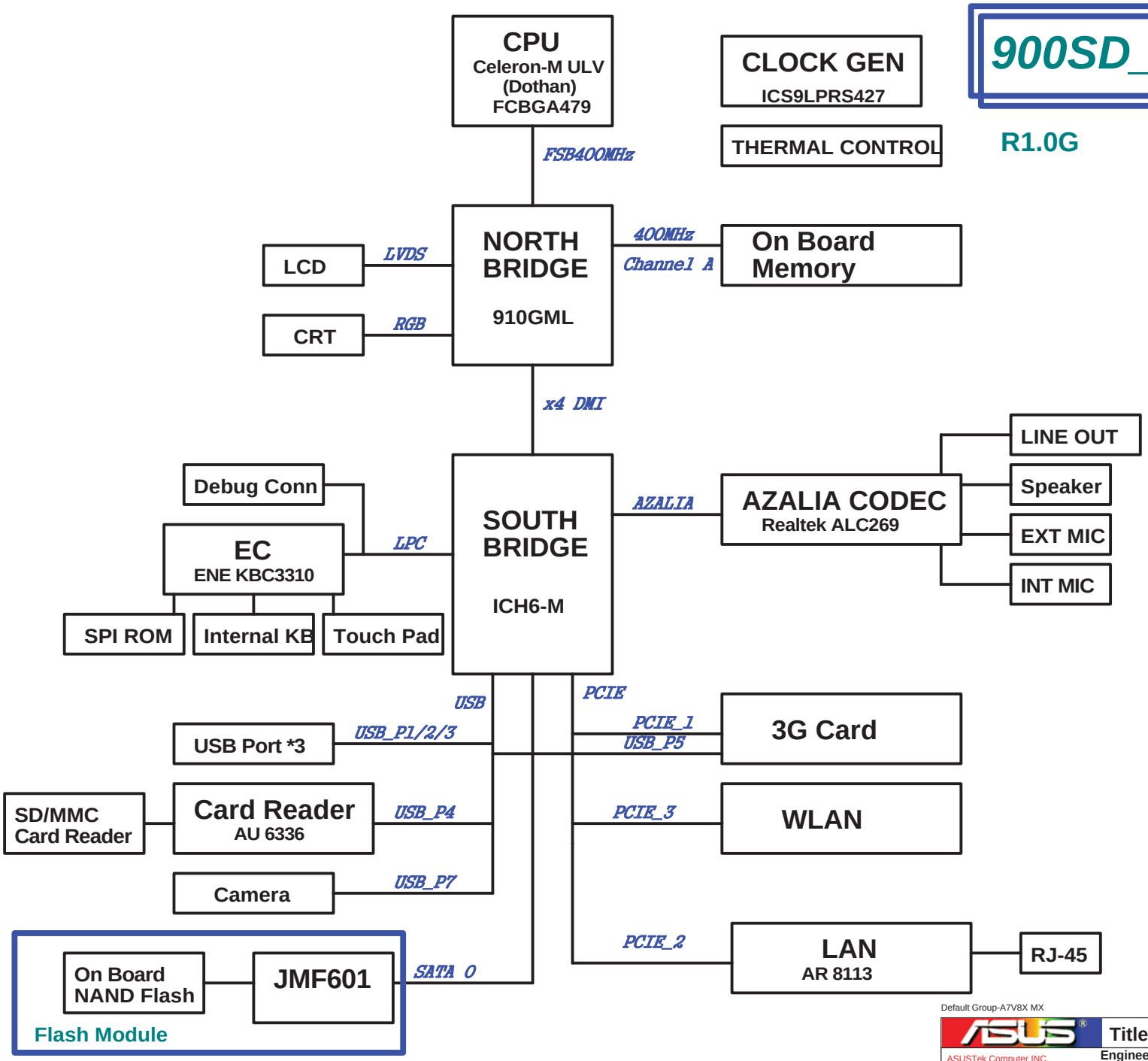
01_Block Diagram
02_System Setting
03_Power Sequence
04_EC Pin Define
05_HISTORY
06_Clock Gen
07_Dothan_HOST
08_Dothan_PWR_GND
09_910GML_HOST_DMI
10_910GML_DRAM
11_910GML_VGA_LVDS_TV
12_910GML_PWR
13_910GML_GND
14_ICH6-M_Azalia_GPIO_PCI_LAN
15_ICH6-M_USB_PCIE_DMI_IDE_SATA
16_ICH6-M_PWR_GND
17_Onboard DRAM_Bottom A1
18_Onboard DRAM_Top A1
19_Onboard DRAM_Bottom A2
20_Onboard DRAM_Top A2
21_DDR2_Termination
22_ONBOARD_VGA
23_LCD-CONN
24_3G Module
25_WLAN
26_LAN
27_RJ45
28_Flash_Ctrl_JMF601
29_On Board NAND Flash
30_USB_PORT
31_CARD_READER
32_CAMERA
33_ALC269-1
34_ALC269-2
35_ALC269-3
36_EC_ENE KB3310
37_Switch_SPI ROM_Debug Conn
38_KB_Touch Pad
39_Thermal Sensor
40_LED
41_Discharge
42_PWR Jack
43_Srew Hole
44_EMI
45_POWER FLOW
46_CHARGER
47_VCORE
48_+3VO_+5VO
49_VTT_DDR_+1.8V_HD
50_+1.8V
51_VCCP
52_1.5_2.5V



Default Group-A7V8X MX

ASUSTek Computer INC.

Title : Block Diagram

Engineer: Hauld_Zhou

Size	Project Name	Rev
A3	900SD_MB	R1.0G

Date: Monday, November 10, 2008 Sheet 1 of 51

ICH6 GPIO SETTING

Pin	Pin Name	Connect to	Type	Input/Output Set
B7	GPI0/REQ6#	10K Pull +3V	I	fixed as Input only
E8	GPI1 / REQ5#	10K Pull +3V	I	fixed as Input only
D9	GPI2 / PIRQE#	10K Pull +3V	I	fixed as Input only
C7	GPI3 / PIRQF#	10K Pull +3V	I	fixed as Input only
C6	GPI4 / PIRQG#	10K Pull +3V	I	fixed as Input only
M3	GPI5 / PIRQH#	10K Pull +3V	I	fixed as Input only
AD19	GPI6 / BMBUSY#	NB BMBUSY#	I	Input
AE19	GPI7	NC	GPI	fixed as Input only
R1	GPI8	EC KBC_SCI#	GPI	fixed as Input only
C23	GPI9/OC4#	10K Pull +3V	I	Input
D23	GPI10/OC5#	10K Pull +3V	I	Input
W6	GPI11 / SMBALERT#	10K Pull +3V	I	Input
M2	GPI12	NC	GPI	fixed as Input only
R6	GPI13	EC EXTSMI#	GPI	fixed as Input only
C25	GPI14/OC6#	10K Pull +3V	I	Input
C24	GPI15 /OC7#	10K Pull +3V	I	Input
D8	GPO16/GTN6#	NC	O	Output
F6	GPO17 / GNT5#	NC	O	Output
AC21	GPO18 / STP_PCI#	Clock GEN STP_PCI#	O	Output
AB21	GPO19	WLAN_LED#	GPO	fixed as Output only
AD22	GPO20 / STP_CPU#	STP_CPU#	O	Output
AD20	GPO21	NC	GPO	
NA	GPIO22	NA	NA	NA
AD21	GPO23	NC	GPO	fixed as Output only
V3	GPIO24	3G	I/O	Output
P5	GPIO25	NC	I/O	Output

Pin	Pin Name	Connect to	Type	Input/Output Set
AF17	GPI26/SATA0GP	NC	GPI	(GPI)Input
R3	GPIO27	NC	I/O	Output
T3	GPIO28	NC	I/O	Output
AE18	GPI29 / SATA1GP	PCBVER0	GPI	(GPI)Input
AF18	GPI30 / SATA2GP	NC	GPI	(GPI)Input
AG18	GPI31 / SATA3GP	PCBVER1	GPI	(GPI)Input
AF19	GPIO32 / CLKRUN#	10K Pull +3V	I/O	Input
AF20	GPIO33	NC	I/O	Output
AC18	GPIO34	NC	I/O	Output
NA	GPIO35	NA	NA	NA
NA	GPIO36	NA	NA	NA
NA	GPIO37	NA	NA	NA
NA	GPIO38	NA	NA	NA
NA	GPIO39	NA	NA	NA
F7	GPI40 / REQ4#	10K Pull +3V	I	Input
P4	GPI41 / LDRQ1#	NC	I	Input
NA	GPIO42	NA	NA	NA
NA	GPIO43	NA	NA	NA
NA	GPIO44	NA	NA	NA
NA	GPIO45	NA	NA	NA
NA	GPIO46	NA	NA	NA
NA	GPIO47	NA	NA	NA
E7	GPO48 /GNT4#	NC	O	Output
AC25	GPO49 / CPUPWRGD	CPU Power Ok	O	Output

fixed as Output only

Default Group-A7V8X MX

ASUSTek Computer INC.

Title : System Setting

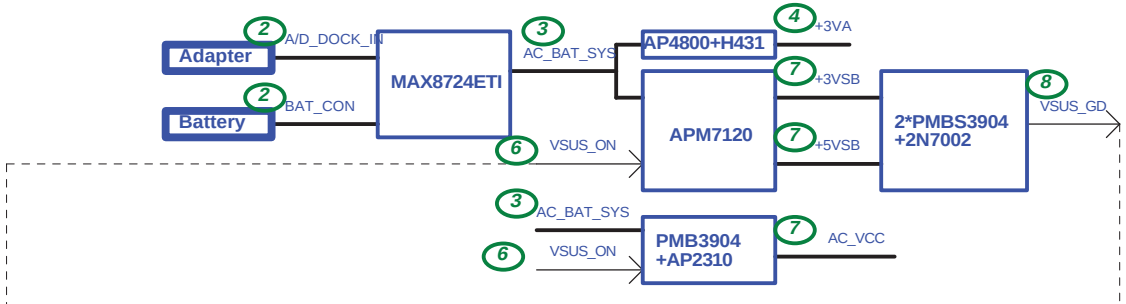
Engineer: Kell_Huang

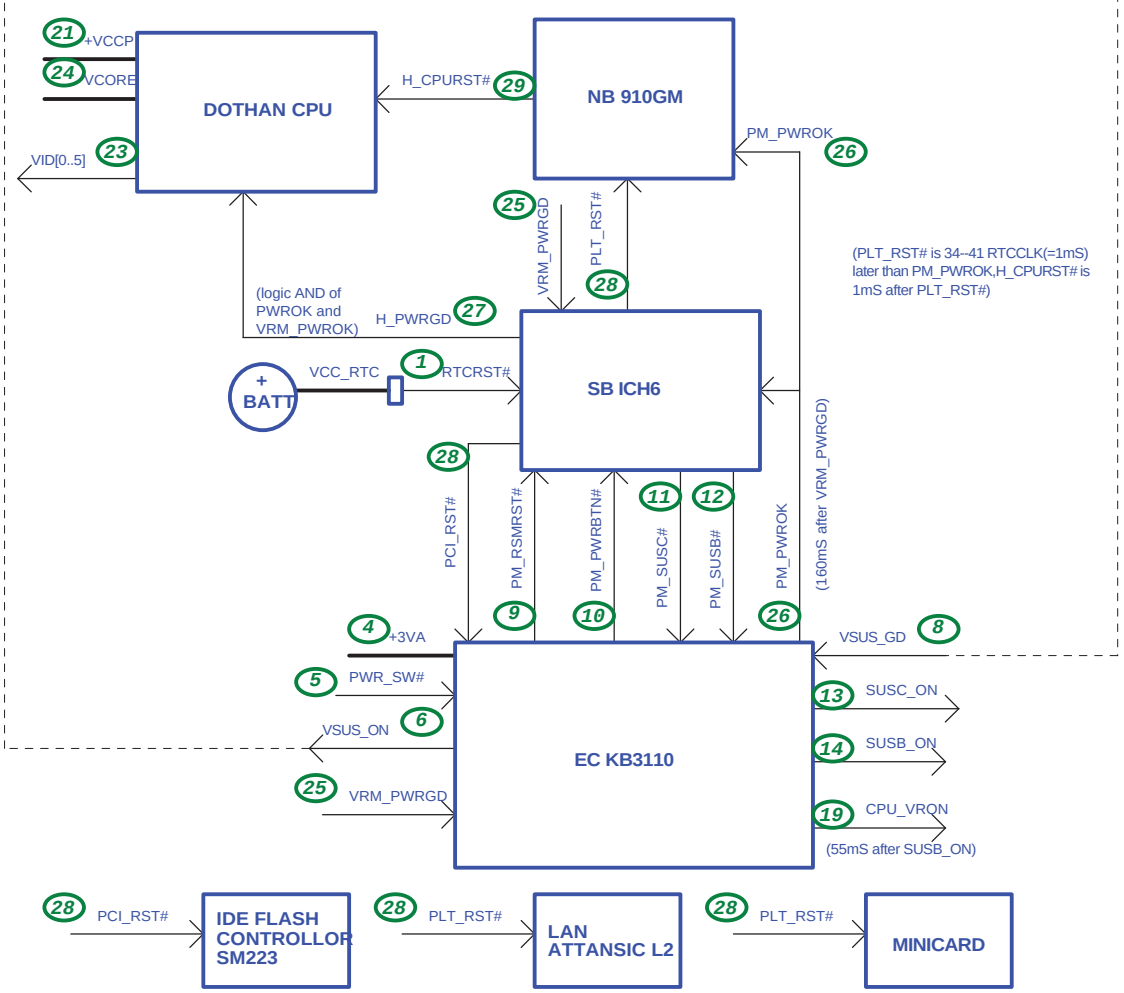
Size	Project Name	Rev
A3	900SD_MB	R1.0G

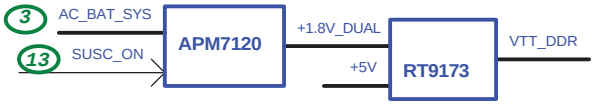
Date: Monday, November 10, 2008 Sheet 2 of 51

*This sequence is for Battery Plug-in and no Adapter,
if Adapter Plug-in,the sequence change to:
A/D_DOCK_IN--->AC_BAT_SYS--->+3VA--->VSUS_ON--->+3VSB & +5VSB
--->VSUS_GD--->PM_REMRST#--->PWR_SW#--->PM_PWRBTN--->PM_SUSC#--->PM_SUSB#

	Signal	S0/S1	S3	S4/S5	Power
Only Battery	VSUS_ON	H	H	L	VSB
Adapter In	VSUS_ON	H	H	H	VSB
	SUSB_ON	H	L	L	Main
	SUSC_ON	H	H	L	DUAL





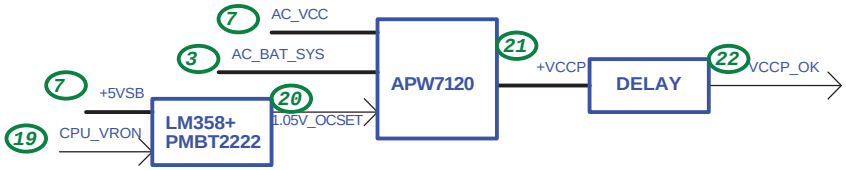


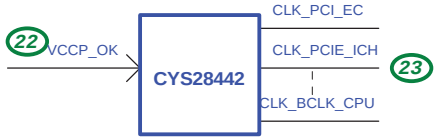


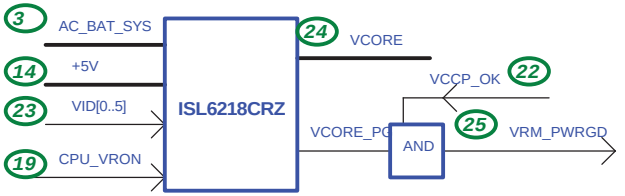












Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Power Sequence	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 3 of 51	

EC KB3310 GPIO SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
1	GA20	A20GATE	O	A20GATE
2	KBRST#	RC_IN#	O	KBRST#
6	GPIO04	CTRL_CAMER_PWR	I	Default : High
13	PCIRST#	PCI_RST#	I	PCI Reset
14	GPIO07	N.C	O	Reserved
15	GPIO08	EXTSMI#	O	EXTSMI#, 10K Pull +3VSUS
16	GPIO0A	LID_EC#	I	LID_EC#, *
17	GPIO0B	LCD_CSB	O	LCD chip select
18	GPIO0C	LCD_SDA	I/O	LCD Data
19	GPIO0D	DISTP_SW#	I	Touch Pad Disabled,*
20	SCI#	KBC_SCI#	O	KBC_SCI#, 10K Pull +3VSUS
21	PWM1	BL_PWM_DA	O	LCD Light Switch
23	PWM2	LCD_SCL	O	LCD clock
25	GPIO11	PM_PWRBTN#	OD	Power Button to SB, *
26	FANPWM1	FAN0_PWM	O	CPU Fan(Unused)
27	FANPWM2	FAN1_PWM	O	VGA Fan(Unused)
28	FANFB1	FAN0_TACH	I	CPU FanTach(Unused)
29	FANFB2	FAN1_TACH	I	VGA FanTach(Unused)
30	GPIO16	E51_TX	O	RS232 debug port
31	GPIO17	N.C	O	Reserved
32	GPIO18	PWR_SW#	I	power button, *
34	GPIO19	MAIL_LED#	O	Mail LED(Unused)
36	GPIO1A	CTRL_Mincard_PWR	O	Default : High
38	CLKRUN#	N.C	O	Reserved
39	KSO0	KSO0	O	For Keyboard interface
40	KSO1	KSO1	O	For Keyboard interface
41	KSO2	KSO2	O	For Keyboard interface
42	KSO3	KSO3	O	For Keyboard interface
43	KSO4	KSO4	O	For Keyboard interface
44	KSO5	KSO5	O	For Keyboard interface
45	KSO6	KSO6	O	For Keyboard interface
46	KSO7	KSO7	O	For Keyboard interface
47	KSO8	KSO8	O	For Keyboard interface
48	KSO9	KSO9	O	For Keyboard interface
49	KSO10	KSO10	O	For Keyboard interface
50	KSO11	KSO11	O	For Keyboard interface
51	KSO12	KSO12	O	For Keyboard interface
52	KSO13	KSO13	O	For Keyboard interface
53	KSO14	KSO14	O	For Keyboard interface
54	KSO15	KSO15	O	For Keyboard interface
55	KSI0	KSI0	I	For Keyboard interface
56	KSI1	KSI1	I	For Keyboard interface
57	KSI2	KSI2	I	For Keyboard interface
58	KSI3	KSI3	I	For Keyboard interface
59	KSI4	KSI4	I	For Keyboard interface
60	KSI5	KSI5	I	For Keyboard interface
61	KSI6	KSI6	I	For Keyboard interface
62	KSI7	KSI7	I	For Keyboard interface
63	AD0	P_PMON_10	I	Sense Power Loading
64	AD1	BAT_IN	I	sense Battery
65	AD2	N.C	I	Reserved
66	AD3	N.C	I	Reserved
68	GPO3C	DOC	O	Trigger Clock Gen

Pin No.	Pin Name	Signal Name	Type	NOTE
70	GPO3D	LCD_BACKOFF#	O	LCD_BACKOFF#
71	GPO3E	CLK_PWRSAVE#	O	Active when BAT_IN=1 and AC_OK=0(Unused)
72	GPO3F	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K Pull GND
75	GPIO42	N.C	O	Reserved
76	GPIO43	N.C	O	Reserved
77	SCL1	SMB0_CLK	I/OD	4.7K Pull +3VA_EC
78	SDA1	SMB0_DAT	I/OD	4.7K Pull +3VA_EC
79	SCL2	SMB1_CLK	I/OD	10K Pull +3VS
80	SDA2	SMB1_DAT	I/OD	10K Pull +3VS
81	KSO16	N.C	O	Reserved
82	KSO17	N.C	O	Reserved
83	PSCLK1	N.C	O	Reserved
84	PSDAT1	N.C	O	Reserved
85	PSCLK2	N.C	O	Reserved
86	PSDAT2	N.C	O	Reserved
87	PSCLK3	TP_CLK	I/OD	10K Pull +3VS
88	PSDAT3	TP_DAT	I/OD	10K Pull +3VS
89	GPIO50	BATSEL_3S	O	Battery series. Hi:3S, Lo:4S(Unused)
90	GPIO52	CHG_LED_UP#	O	charger LED
91	GPIO53	CTRL_L2_PWR	O	Default : High
92	GPIO54	PWR_LED_UP	O	EC H/W blinking
93	GPIO55	SCRL_LED#	O	EC H/W controls
95	GPIO56	PWR4G_SW#	I	*
97	GPXOA00	SPI_MODE#	O	"HW Strap for SPI Flash deExternal Pull Down 100K ohm to GND"
98	GPXOA01	SUSC_ON	O	
99	GPXOA02	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH8_PWROK	O	
103	GPXOA06	N.C	O	Reserved
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0	BATSEL_2P#	O	Battery parallel. Hi:1P, Lo:2P~3P
110	GPXID1	N.C	O	Reserved
112	GPXID2	THRO_CPU	O	Active if Battery Temperature is
114	GPXID3	SUSB#	I	Pull Down 100K ohm to GND
115	GPXID4	SUSC#	I	Pull Down 100K ohm to GND
116	GPXID5	CPUPWR_GD	I	10K Pull +3VS
117	GPXID6	VSUS_GD	I	Disabled **
118	GPXID7	N.C	O	Reserved
121	GPIO57	INTERNET#	I	*
126	SPICLK	SPI_CLK	O	SPI Clock
127	GPIO59	N.C	O	Reserved

EC KB3310 Other Pin SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
3	SERIRQ	INT_SERIRQ	I/OD	8.2K Pull +3VS
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	Add 100K ohm to GND
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#	SPI_SO	I	
120	WR#	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	K_V18R		Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#	SPI_CE#	O	

Default Group-A7V8X MX

ASUSTek Computer INC.

Title : EC Pin Define

Engineer: Kell_Huang

Size	Project Name	Rev
A3	900SD_MB	R1.0G

Date: Monday, November 10, 2008 Sheet 4 of 51

CIRCUIT UPDATED HISTORY

Rev	Date	Description
900SD 1.0G	2008.10.15	Initial Release

Default Group-A7V8X MX

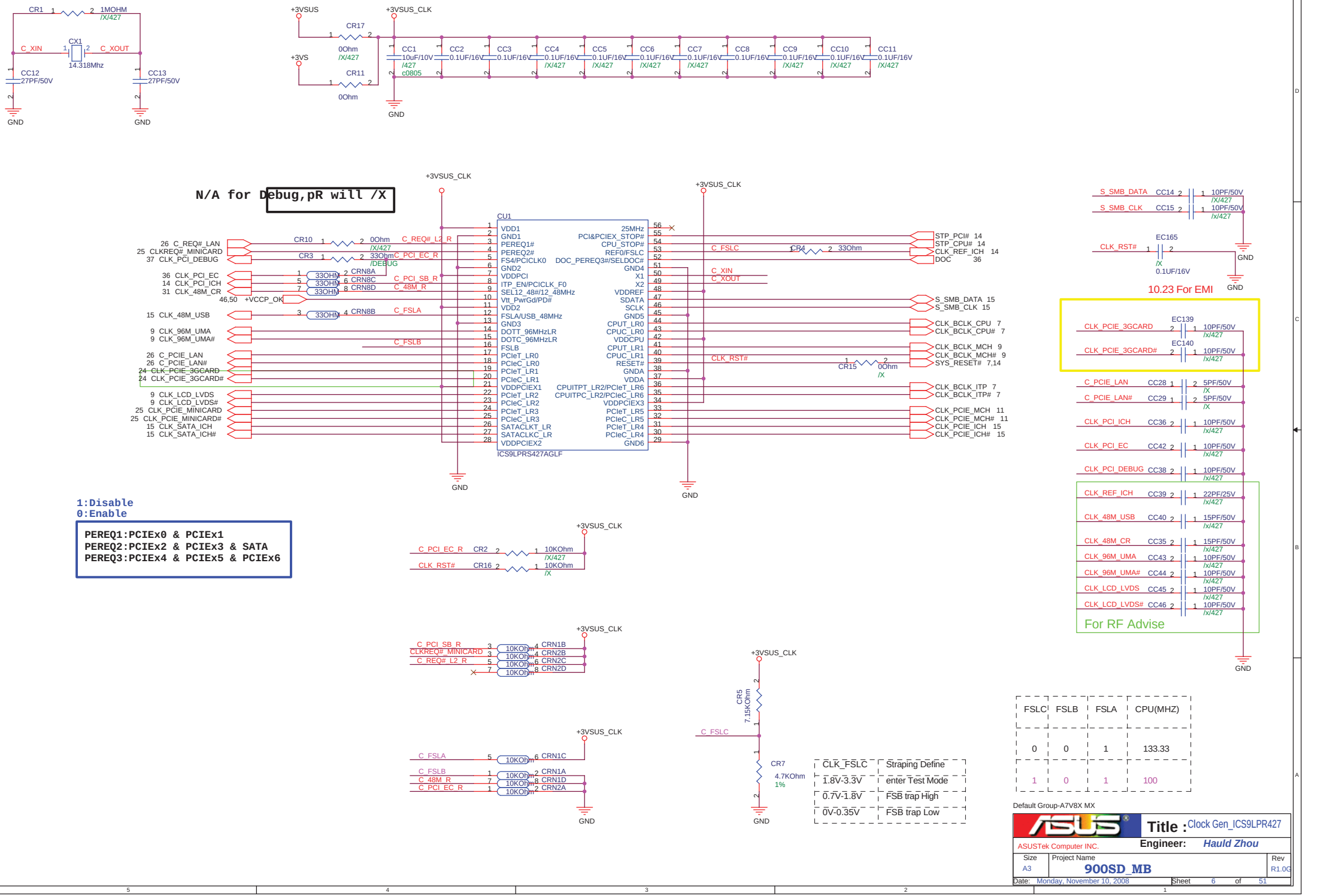
ASUSTek Computer INC.

Title : History

Engineer: Hauld Zhou

Size	Project Name	Rev
A3	900SD_MB	R1.0G

Date: Monday, November 10, 2008 Sheet 5 of 51



CLK_FSLC	Straping Define
1.8V-3.3V	enter Test Mode
0.7V-1.8V	FSB trap High
0V-0.35V	FSB trap Low

FSLC	FSLB	FSLA	CPU(MHZ)
0	0	1	133.33
1	0	1	100

Default Group-A7V8X MX

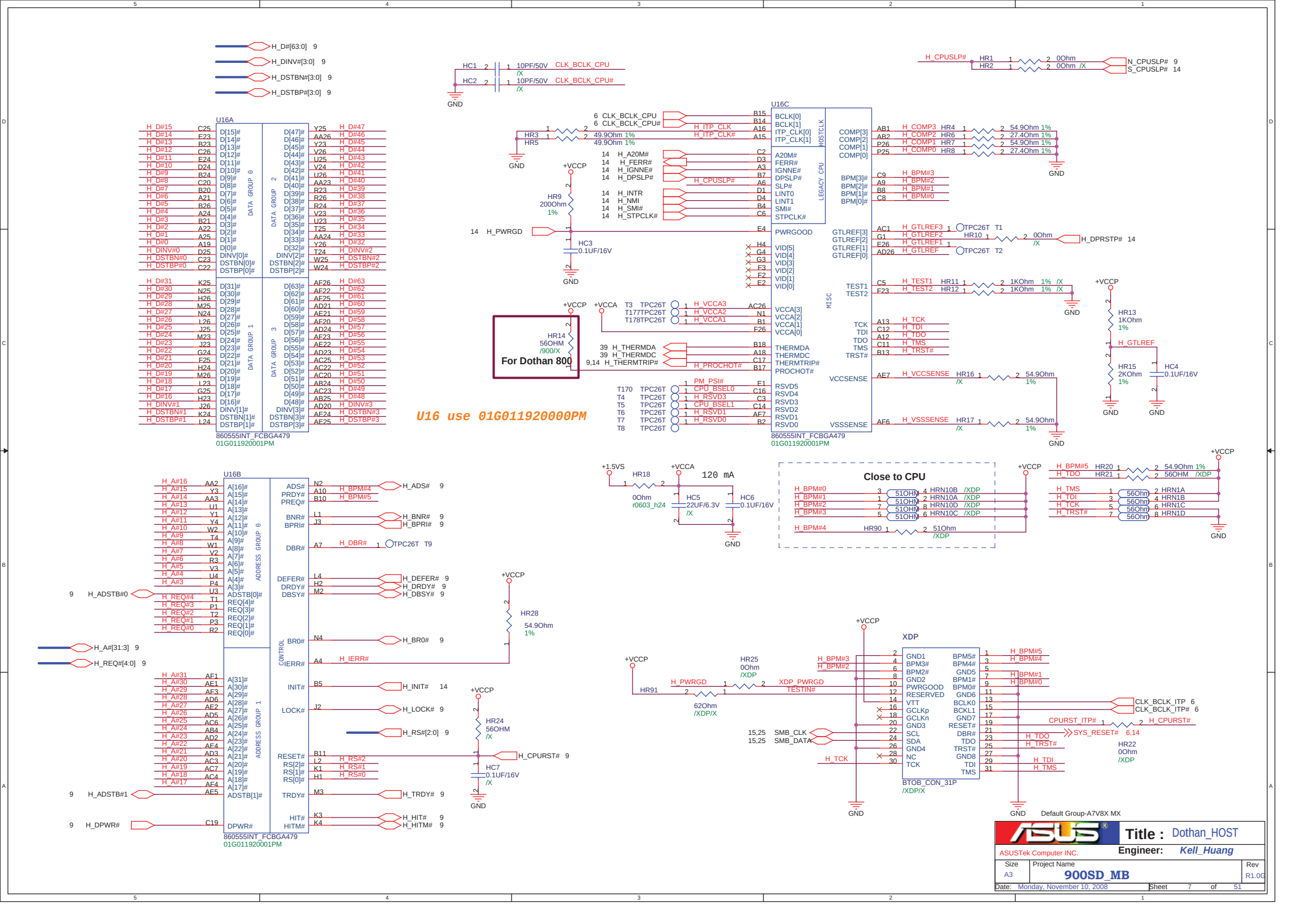
ASUSTek Computer INC.

Title : Clock Gen_ICS9LPR427

Engineer: Hauld Zhou

Size	Project Name	Rev
A3	900SD_MB	R1.0G

Date: Monday, November 10, 2008 Sheet 6 of 51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H_DINV#[3:0] 9
H_DSTBN#[3:0] 9
H_DSTBP#[3:0] 9
U16A
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
860555INT_FCBGA479
01G011920001PM
HC1 10PF/50V CLK_BCLK_CPU /X
HC2 10PF/50V CLK_BCLK_CPU# /X
GND
U16C
HOSTCLK
LEGACY CPU
MISC
HR3 49.9Ohm 1%
HR5 49.9Ohm 1%
HR9 200Ohm 1%
HC3 0.1UF/16V
HR14 56OHM /900/X
For Dothan 800
HR10 0Ohm /X
HR11 1KOhm 1% /X
HR12 1KOhm 1% /X
HR13 1KOhm 1%
HR15 2KOhm 1%
HC4 0.1UF/16V
HR16 54.9Ohm 1% /X
HR17 54.9Ohm 1% /X
H_CPUSLP# HR1 HR2 0Ohm /X
N_CPUSLP# 9
S_CPUSLP# 14
H_DPRSTP# 14
U16 use 01G011920000PM
U16B
ADDRESS GROUP 0
ADDRESS GROUP 1
CONTROL
HR18 0Ohm r0603_h24
HC5 22UF/6.3V /X
HC6 0.1UF/16V
120 mA
Close to CPU
HR90 51Ohm /XDP
HR20 54.9Ohm 1%
HR21 56OHM /XDP
HR28 54.9Ohm 1%
HR24 56OHM /X
HC7 0.1UF/16V /X
HR25 0Ohm /XDP
HR91 62Ohm /XDP/X
XDP
BTOB_CON_31P
/XDP/X
HR22 0Ohm /XDP
Default Group-A7V8X MX
ASUSTek Computer INC.
Title : Dothan_HOST
Engineer: Kell_Huang
Size A3
Project Name 900SD_MB
Rev R1.0G
Date: Monday, November 10, 2008
Sheet 7 of 51

+VCCP 2.5 A

+VCORE

Celeron-M(Dothan) ULV max 7 A

U16D

VCC

860555INT_FCBGA479
01G011920001PM

+VCORE

HCE1 10UF/6.3V N/A c0805

HCE2 100U/2.5V /CAP/X

+VCCP

HCE3 10UF/6.3V /X c0603

HCE4 100U/2.5V /CAP/X

GND

900SD R1.0G

0.1U All X7R

+VCORE

HC23 0.1UF/16V /CAP/X

HC24 0.1UF/16V

HC26 0.1UF/16V /CAP/X

GND

+VCCP

HC27 10UF/6.3V

HC28 10UF/6.3V /CAP/X

HC29 10UF/6.3V

HC20 0.1UF/16V

HC21 0.1UF/16V

HC22 0.1UF/16V /CAP/X

HC25 0.1UF/16V

GND

U16E

GND

860555INT_FCBGA479
01G011920001PM

GND

+VCORE

HC10 10UF/6.3V /CAP/X

HC11 10UF/6.3V /CAP/X

HC12 10UF/6.3V

HC13 10UF/6.3V

HC14 10UF/6.3V /CAP/X

HC15 10UF/6.3V /CAP/X

HC16 10UF/6.3V /CAP/X

HC17 10UF/6.3V /CAP/X c0805

HC18 10UF/6.3V /CAP/X

GND

Default Group-A7V8X MX

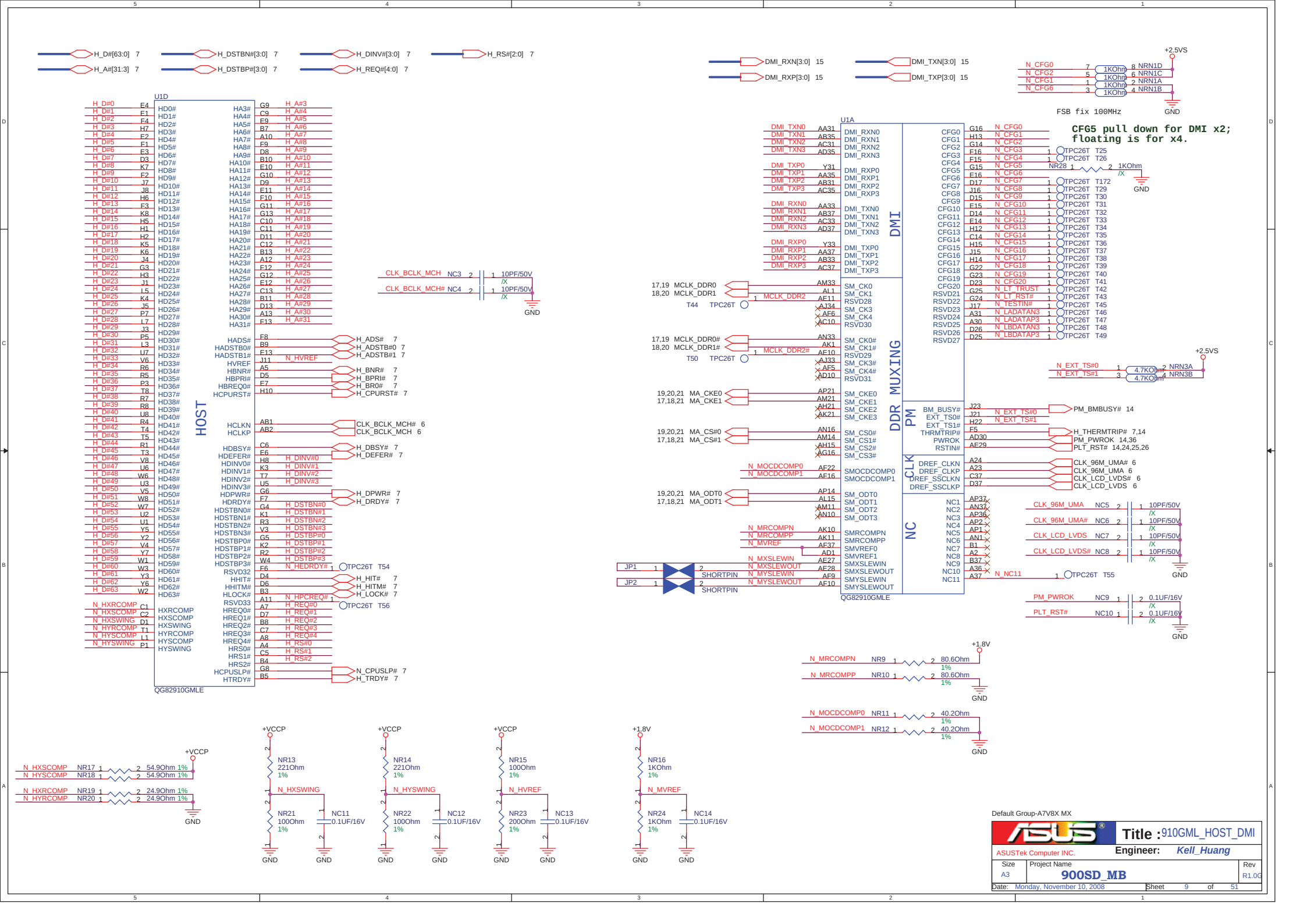
ASUSTek Computer INC.

Title : Dothan_PWR_GND

Engineer: Kell_Huang

Size	Project Name	Rev
A3	900SD_MB	R1.0G

Date: Monday, November 10, 2008 Sheet 8 of 51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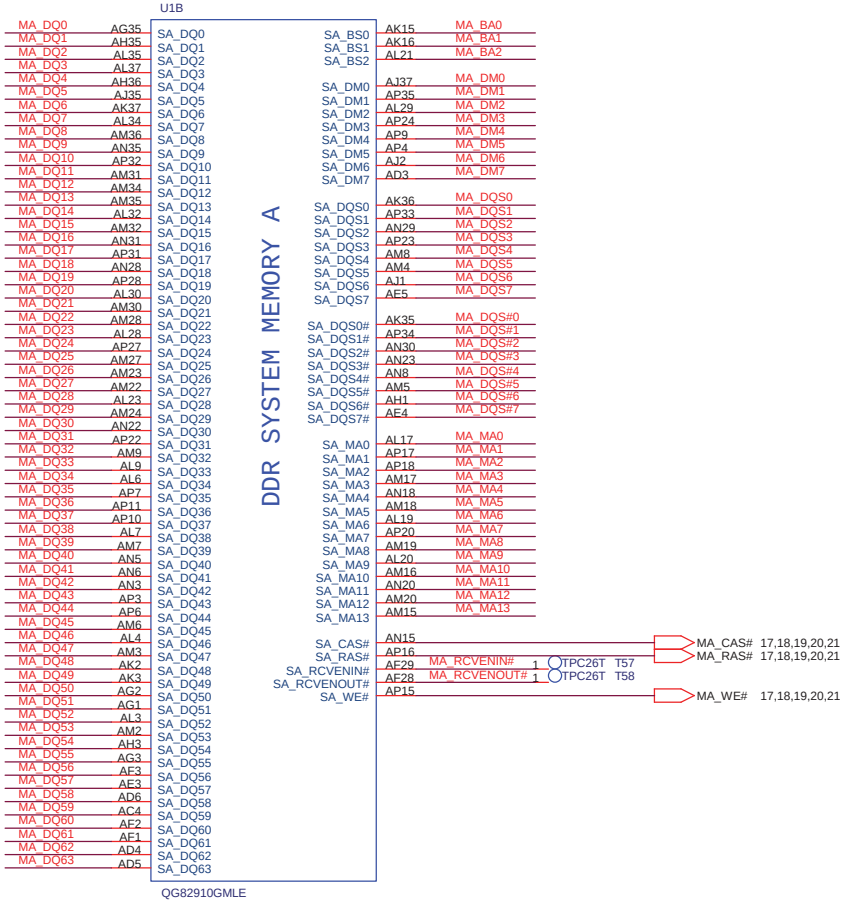
H_A#[31:3] 7
H_DSTBN#[3:0] 7
H_DSTBP#[3:0] 7
H_DINV#[3:0] 7
H_REQ#[4:0] 7
H_RS#[2:0] 7
DMI_RXN[3:0] 15
DMI_RXP[3:0] 15
DMI_TXN[3:0] 15
DMI_TXP[3:0] 15
U1D
HOST
QG82910GMLE
U1A
DMI
DDR MUXING
PM
CLK
NC
QG82910GMLE
FSB fix 100MHz
CFG5 pull down for DMI x2; floating is for x4.
+2.5VS
+1.8V
+VCCP
GND
Default Group-A7V8X MX
ASUSTek Computer INC.
Title : 910GML_HOST_DMI
Engineer: Kell_Huang
Size A3
Project Name 900SD_MB
Rev R1.0C
Date: Monday, November 10, 2008
Sheet 9 of 51

MA_DQ[63:0] 17,18,19,20
MA_DQS[7:0] 17,18,19,20
MA_DQS#[7:0] 17,18,19,20
MA_DM[7:0] 17,18,19,20
MA_MA[13:0] 17,18,19,20,21
MA_BA[2:0] 17,18,19,20,21





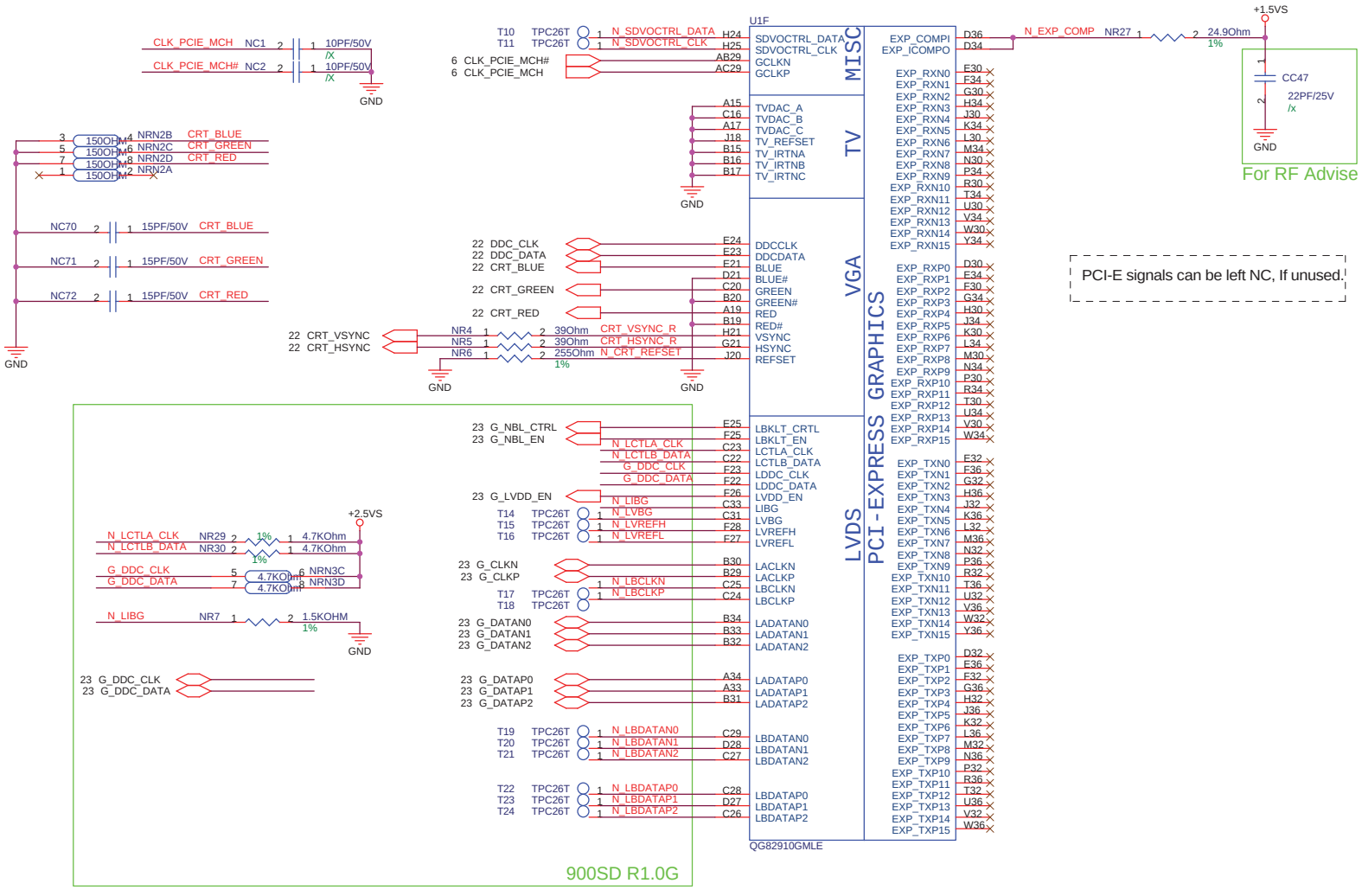
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : 910GML_DRAM	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 10 of 51	

SDVO SMbus have internal pull down

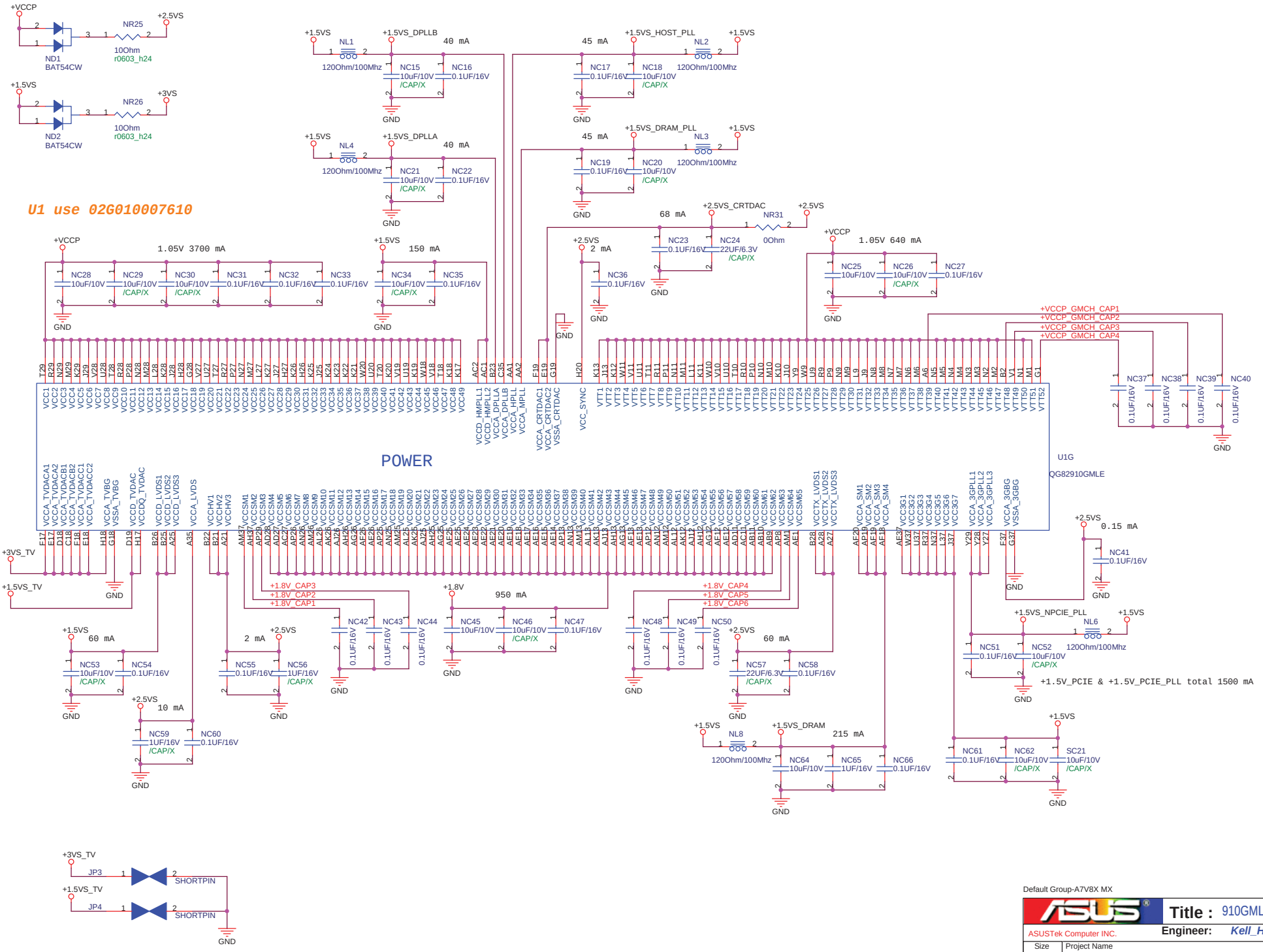
SDVOCRTL_DATA Int PD
0 : No SDVO device
1 : SDVO device present

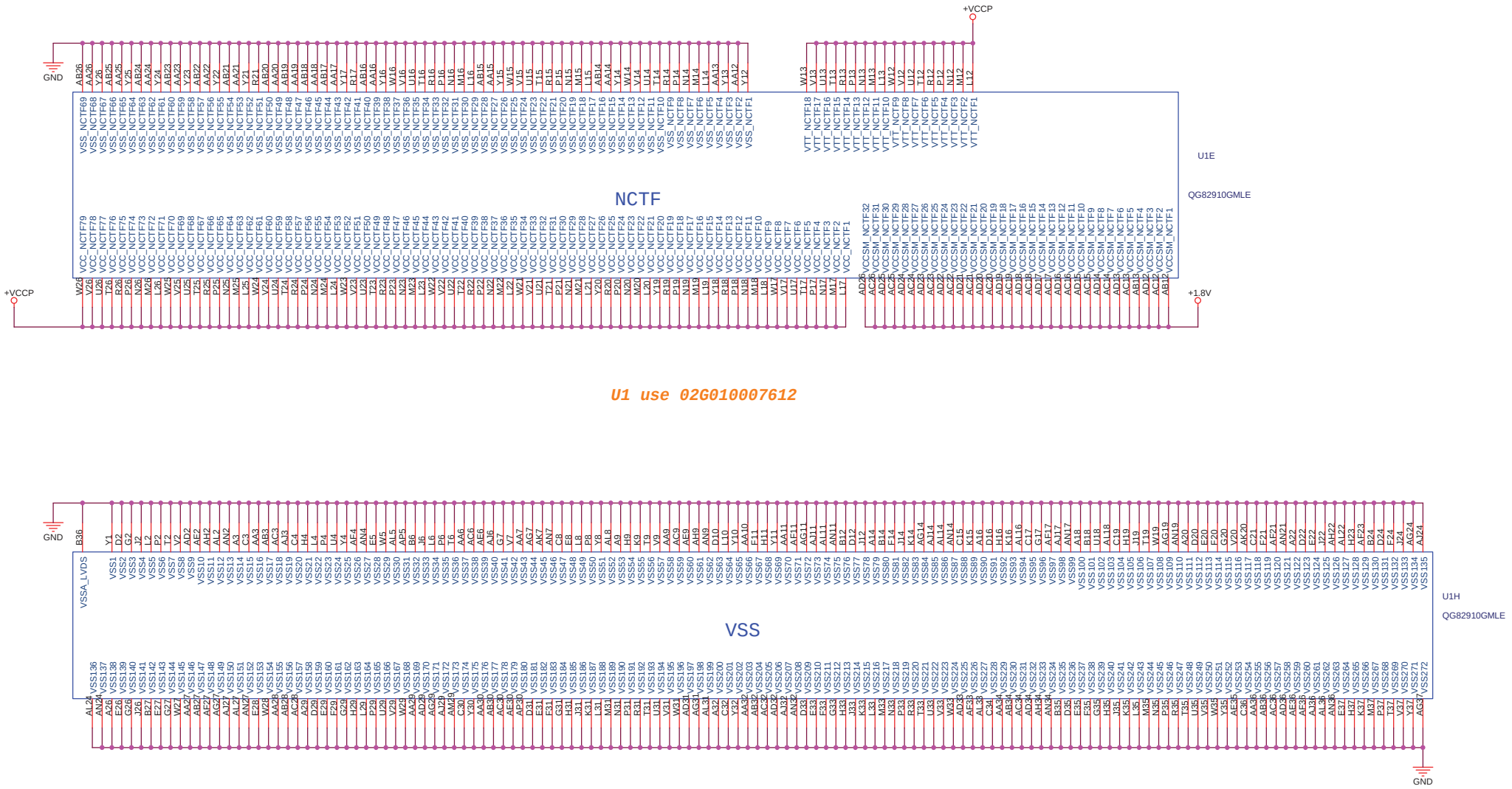
U1 use 02G010007610



Default Group-A7V8X MX

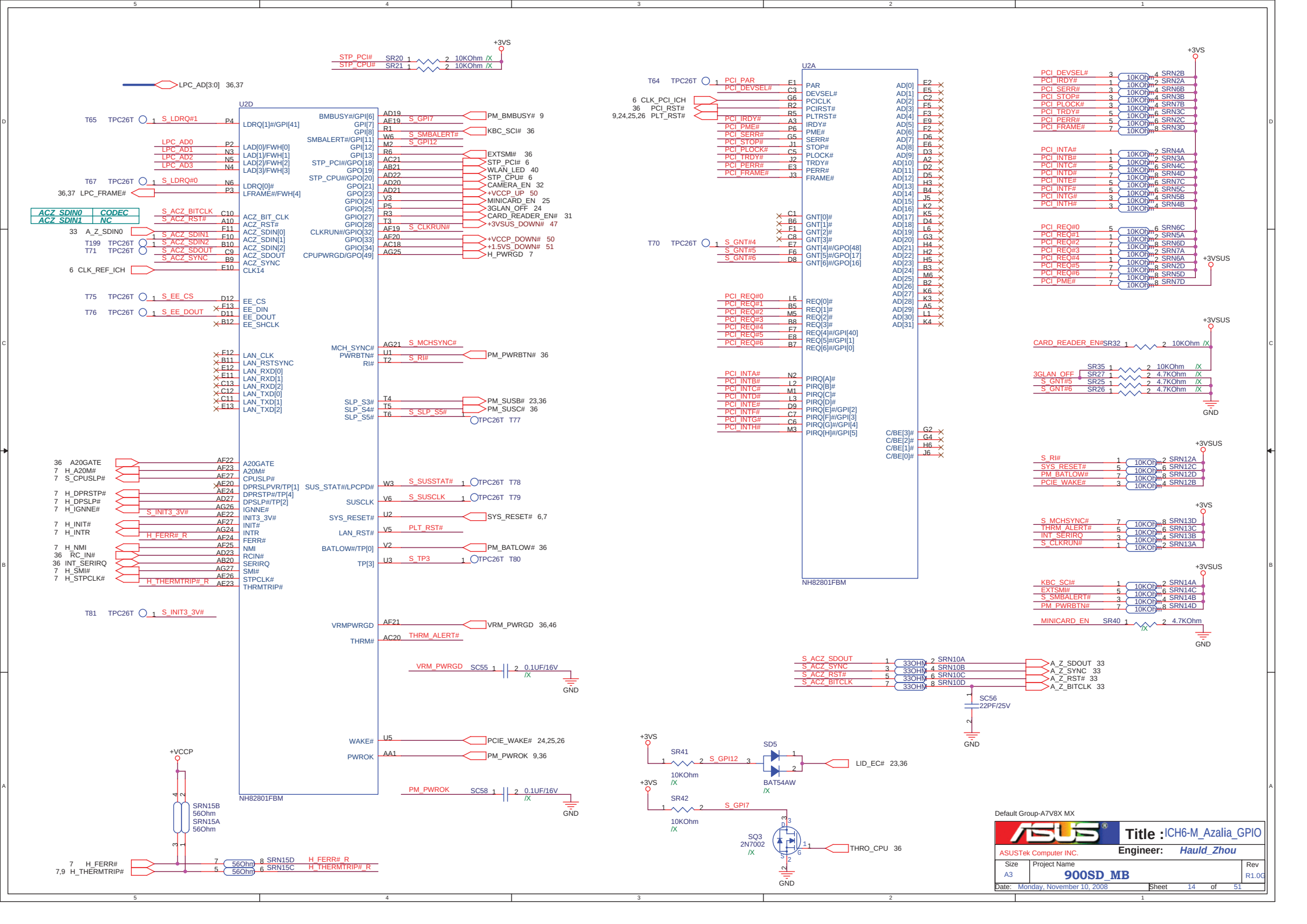
ASUSTek Computer INC.	Title : 910GML_VGA_LVDS	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 11 of 51	


U1 use 02G010007610
POWER
U1G
QG82910GMLE
+VCCP
+2.5VS
+3VS
+1.5VS
+3VS_TV
+1.5VS_TV
GND
ND1 BAT54CW
ND2 BAT54CW
NR25
NR26
10Ohm r0603_h24
+1.5VS_DPLLB
+1.5VS_DPLLA
+1.5VS_HOST_PLL
+1.5VS_DRAM_PLL
+2.5VS_CRTDAC
NL1
NL2
NL3
NL4
120Ohm/100Mhz
40 mA
45 mA
68 mA
150 mA
2 mA
1.05V 3700 mA
1.05V 640 mA
NR31
0Ohm
+VCCP_GMCH_CAP1
+VCCP_GMCH_CAP2
+VCCP_GMCH_CAP3
+VCCP_GMCH_CAP4
+1.8V_CAP1
+1.8V_CAP2
+1.8V_CAP3
+1.8V_CAP4
+1.8V_CAP5
+1.8V_CAP6
+1.8V
950 mA
0.15 mA
60 mA
10 mA
215 mA
+1.5VS_NPCIE_PLL
+1.5V_PCIE & +1.5V_PCIE_PLL total 1500 mA
+1.5VS_DRAM
JP3
JP4
SHORTPIN
Default Group-A7V8X MX
ASUSTek Computer INC.
Title : 910GML_PWR
Engineer: Kell_Huang
Size A3
Project Name 900SD_MB
Rev R1.0G
Date: Monday, November 10, 2008
Sheet 12 of 51



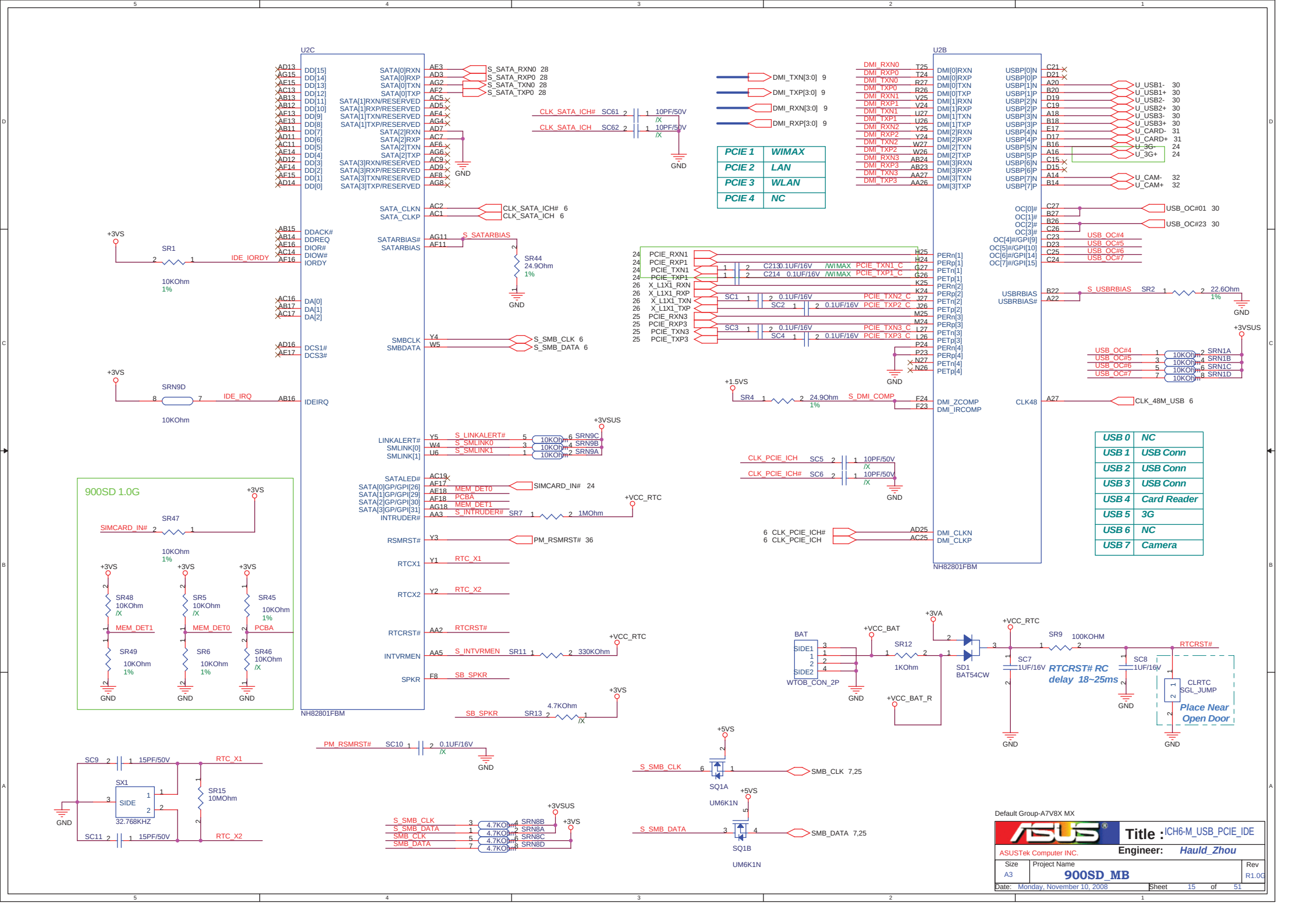
Default Group-A7V8X MX

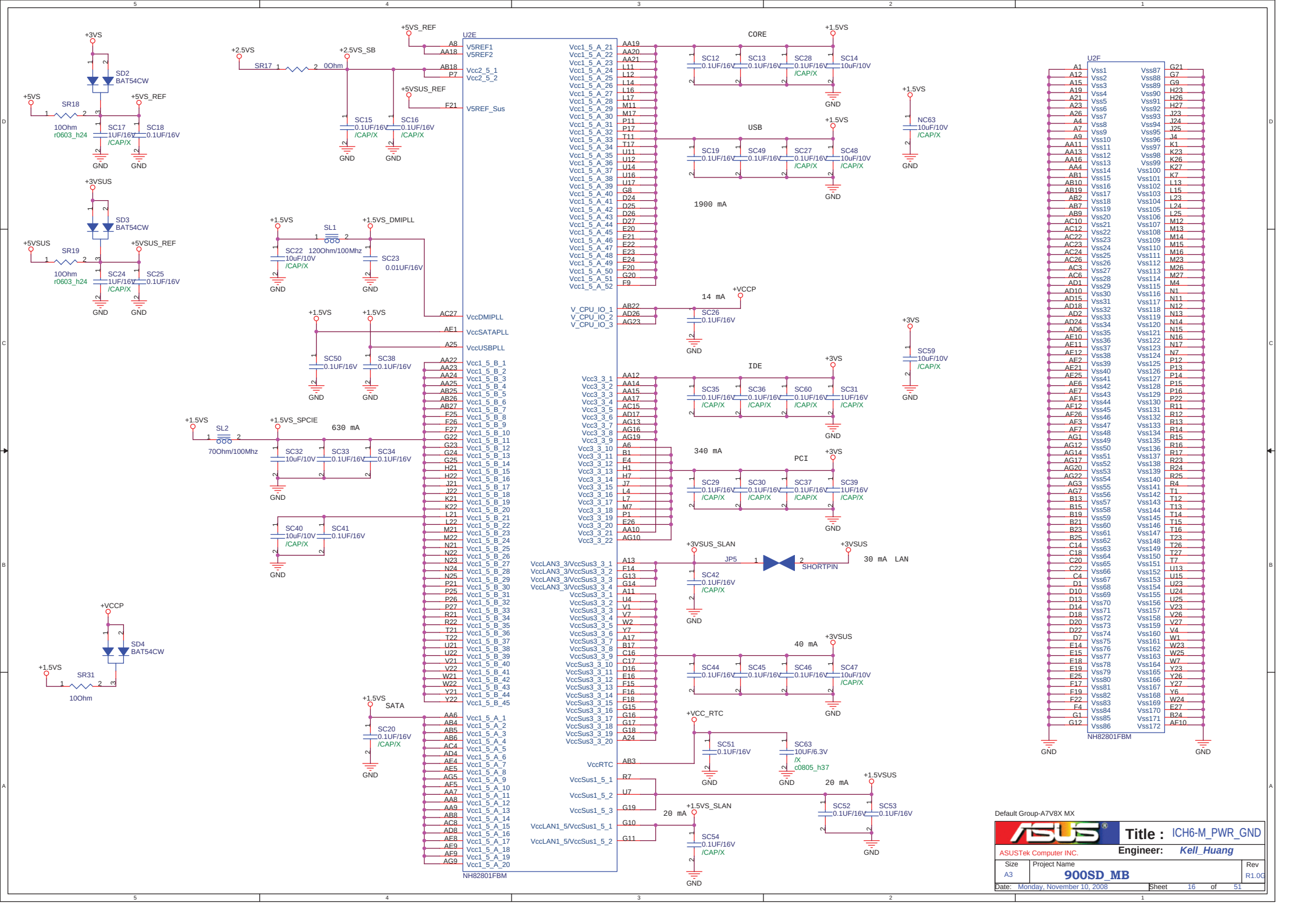
ASUSTek Computer INC.	Title : 910GML_GND	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 13 of 51	



Default Group-A7V8X MX

ASUSTek Computer INC.	Title : ICH6-M_Azalia_GPIO	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 14 of 51	


U2C
NH82801FBM
U2B
NH82801FBM
900SD 1.0G
PCIE 1 WIMAX
PCIE 2 LAN
PCIE 3 WLAN
PCIE 4 NC
USB 0 NC
USB 1 USB Conn
USB 2 USB Conn
USB 3 USB Conn
USB 4 Card Reader
USB 5 3G
USB 6 NC
USB 7 Camera
RTCRST# RC delay 18~25ms
Place Near Open Door
Default Group-A7V8X MX
Title : ICH6-M_USB_PCIE_IDE
ASUSTek Computer INC.
Engineer: Hauld_Zhou
Size A3
Project Name 900SD_MB
Rev R1.0G
Date: Monday, November 10, 2008
Sheet 15 of 51



Default Group-A7V8X MX

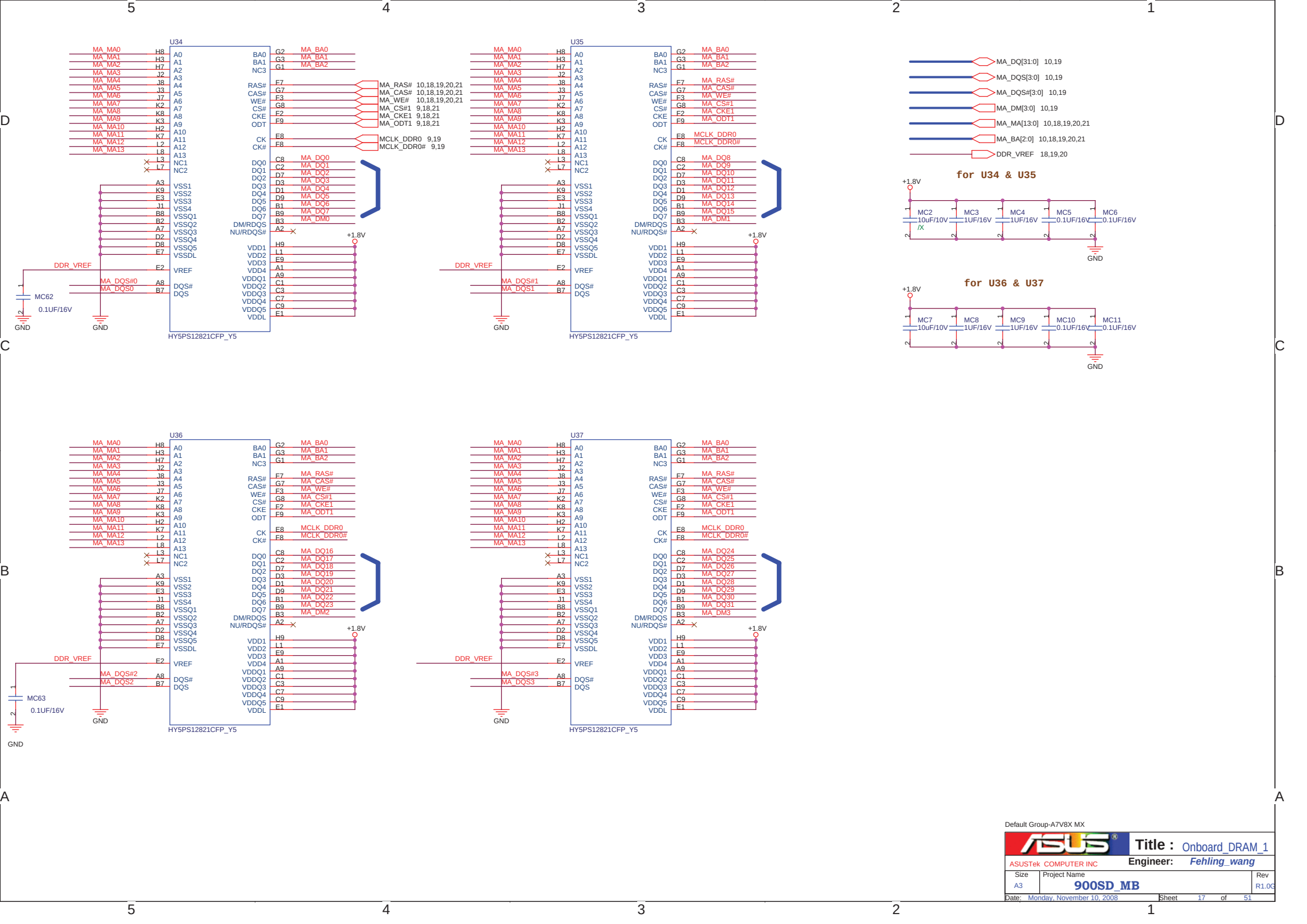
ASUSTek Computer INC.

Title : ICH6-M_PWR_GND

Engineer: Kell_Huang

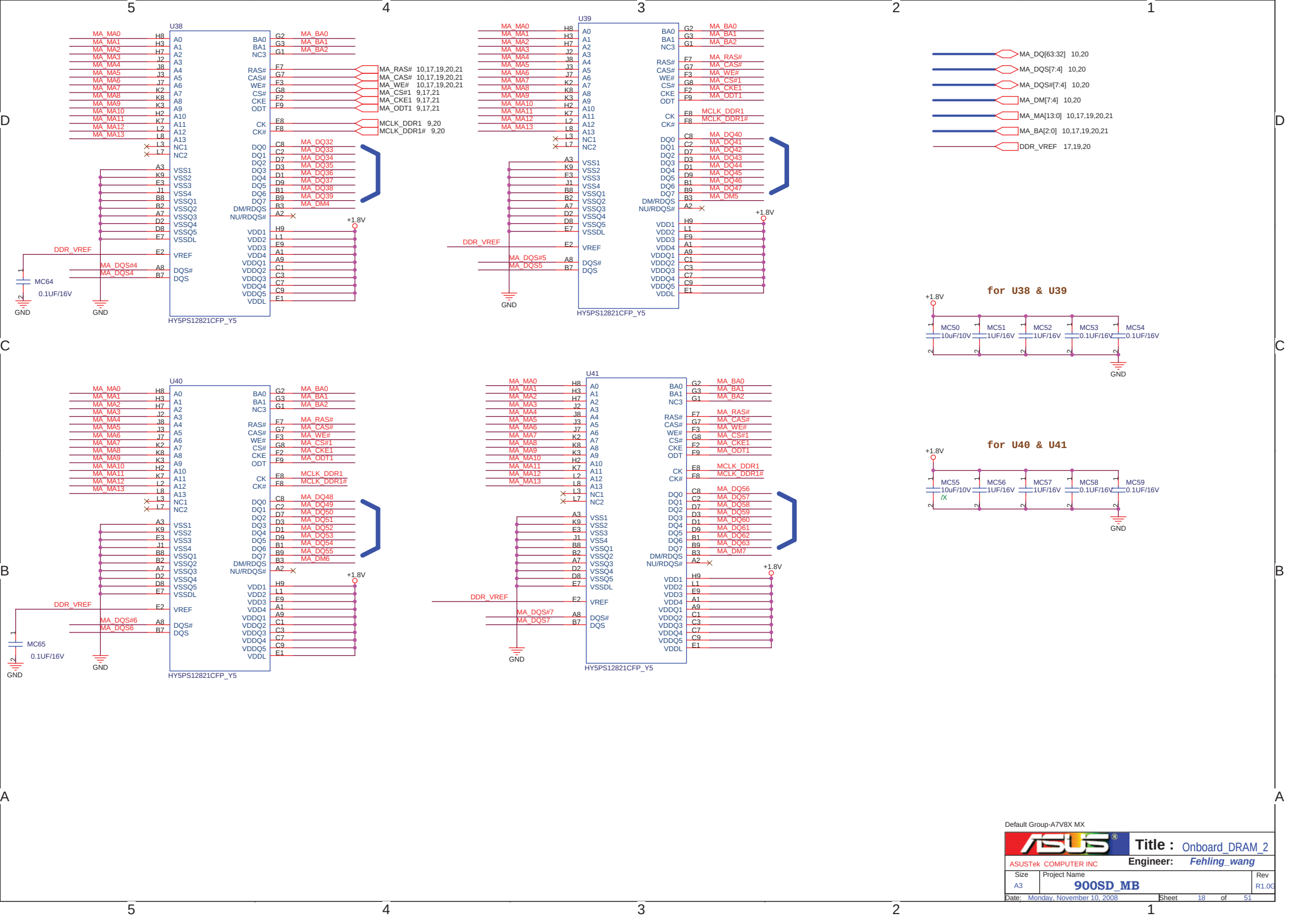
Size	Project Name	Rev
A3	900SD_MB	R1.0G

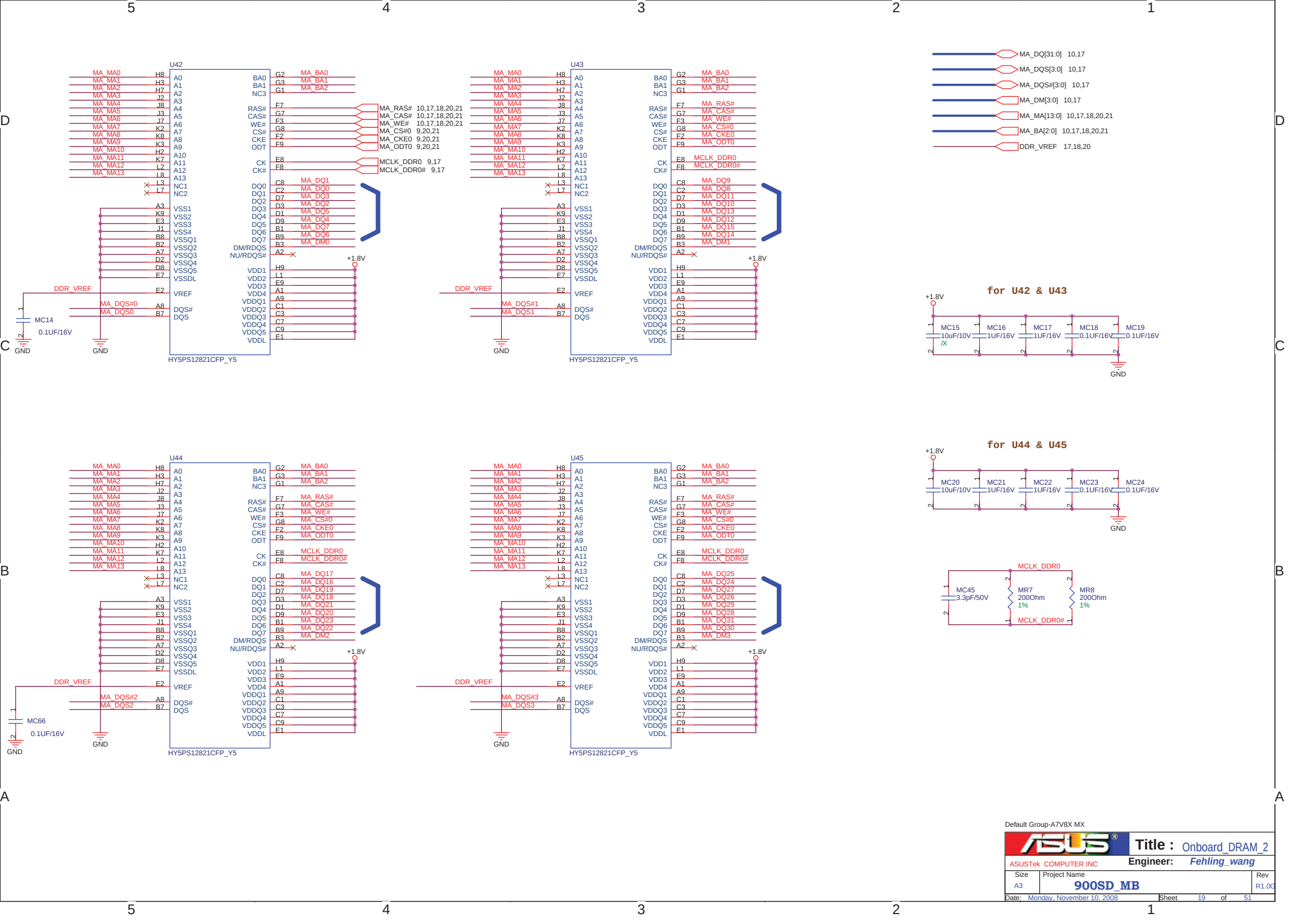
Date: Monday, November 10, 2008 Sheet 16 of 51



Default Group-A7V8X MX

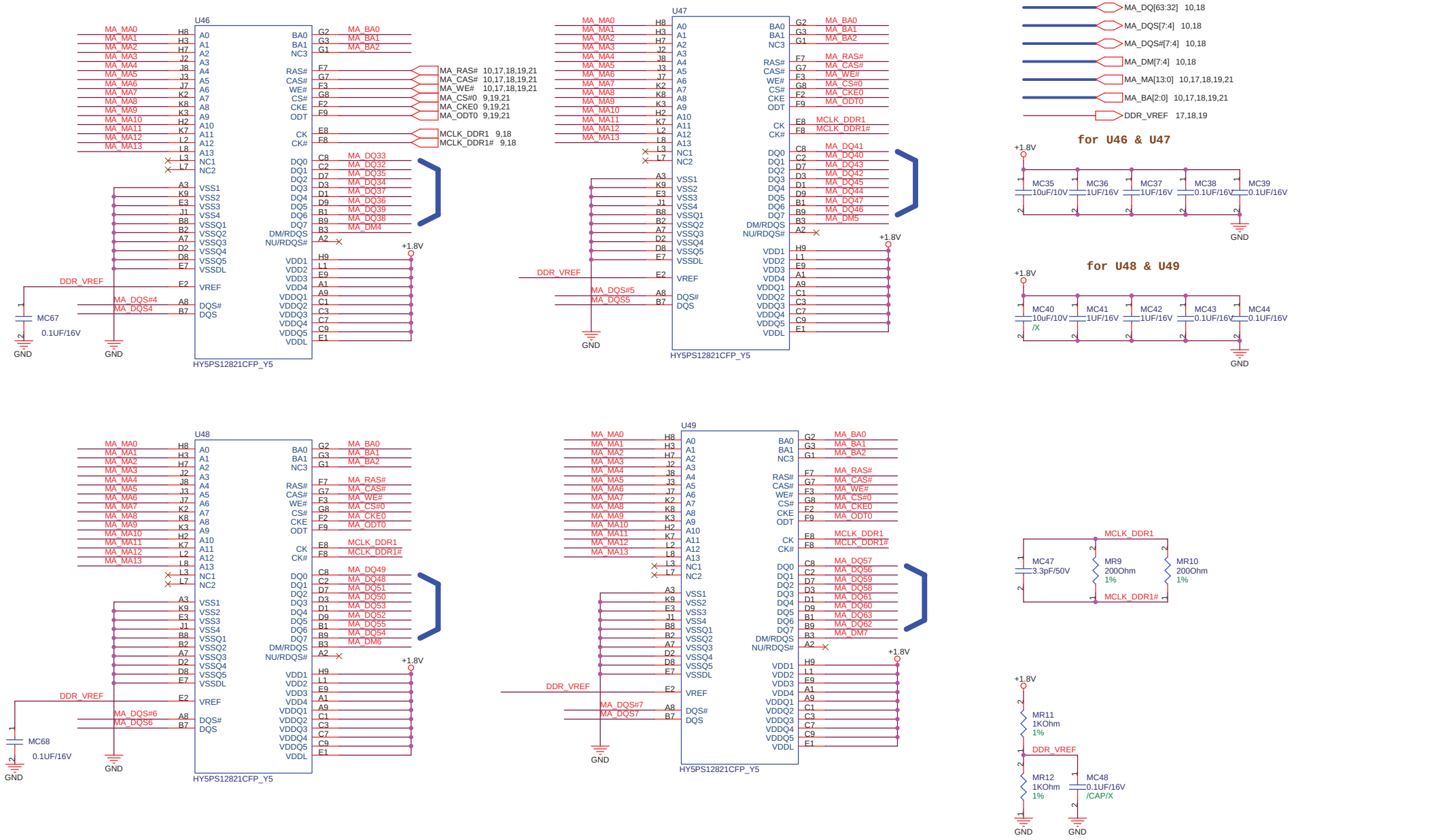
ASUSTek COMPUTER INC	Title : Onboard_DRAM_1	
	Engineer: Fehling_wang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 17 of 51	


U38
U39
U40
U41
HY5PS12821CFP_Y5
MA_DQ[63:32] 10,20
MA_DQS[7:4] 10,20
MA_DQS#[7:4] 10,20
MA_DM[7:4] 10,20
MA_MA[13:0] 10,17,19,20,21
MA_BA[2:0] 10,17,19,20,21
DDR_VREF 17,19,20
MA_RAS# 10,17,19,20,21
MA_CAS# 10,17,19,20,21
MA_WE# 10,17,19,20,21
MA_CS#1 9,17,21
MA_CKE1 9,17,21
MA_ODT1 9,17,21
MCLK_DDR1 9,20
MCLK_DDR1# 9,20
for U38 & U39
for U40 & U41
MC64
MC65
0.1UF/16V
MC50
MC51
MC52
MC53
MC54
MC55
MC56
MC57
MC58
MC59
10uF/10V
1UF/16V
0.1UF/16V
/X
+1.8V
GND
Default Group-A7V8X MX
Title : Onboard_DRAM_2
ASUSTek COMPUTER INC
Engineer: Fehling_wang
Size A3
Project Name 900SD_MB
Rev R1.0G
Date: Monday, November 10, 2008
Sheet 18 of 51



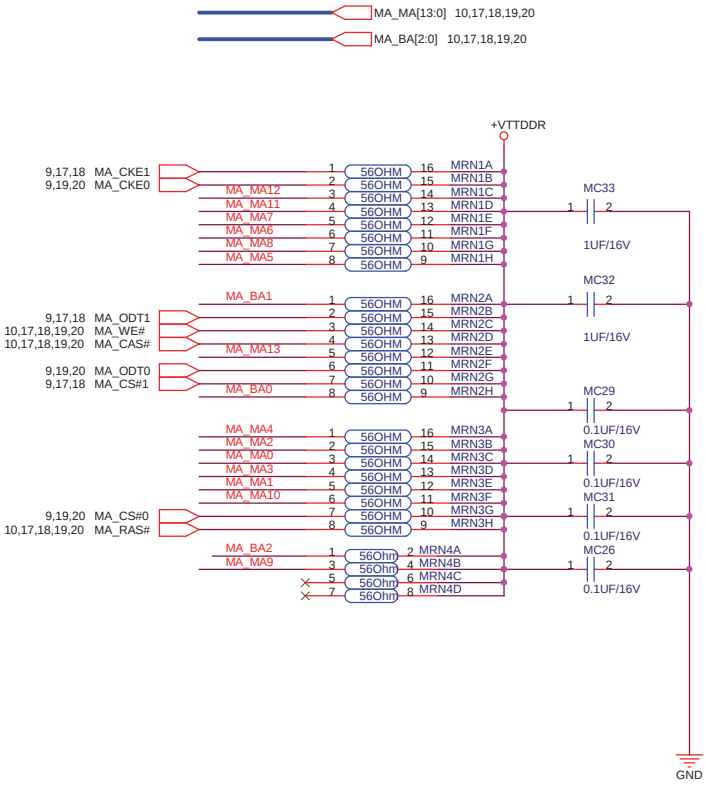
Default Group-A7V8X MX

ASUSTek COMPUTER INC	Title : Onboard_DRAM_2	
	Engineer: Fehling_wang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 19 of 51	



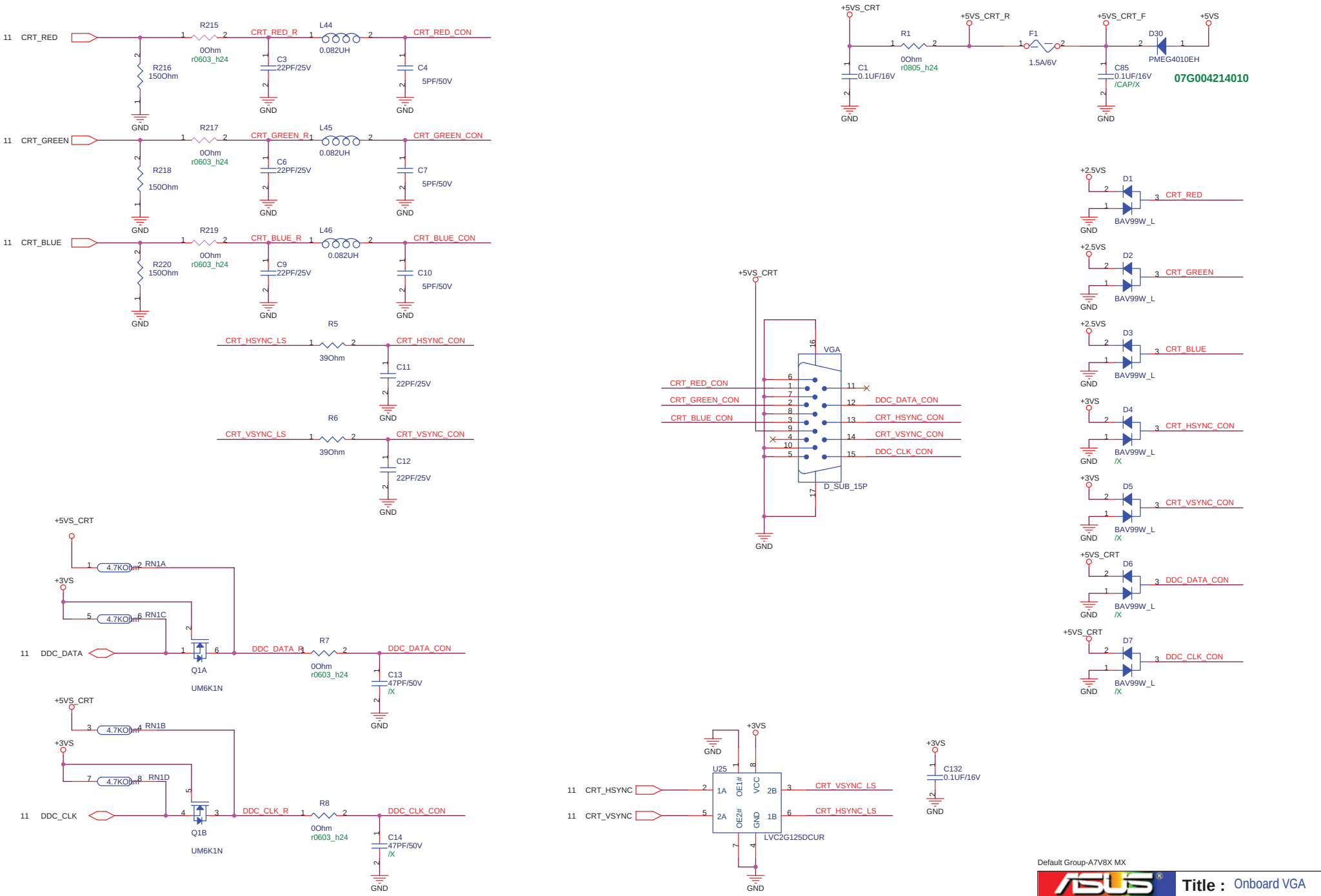
Default Group-A7V8X MX

ASUSTek COMPUTER INC	Title : Onboard_DRAM_1	
	Engineer: Fehling_wang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 20 of 51	



Default Group-A7V8X MX

ASUSTek Computer INC.	Title : DDR2_Termination	
	Engineer: *Kell_Huang*	
Size: A3	Project Name: **900SD_MB**	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 21 of 51	



Default Group-A7V8X MX

ASUSTek Computer INC.

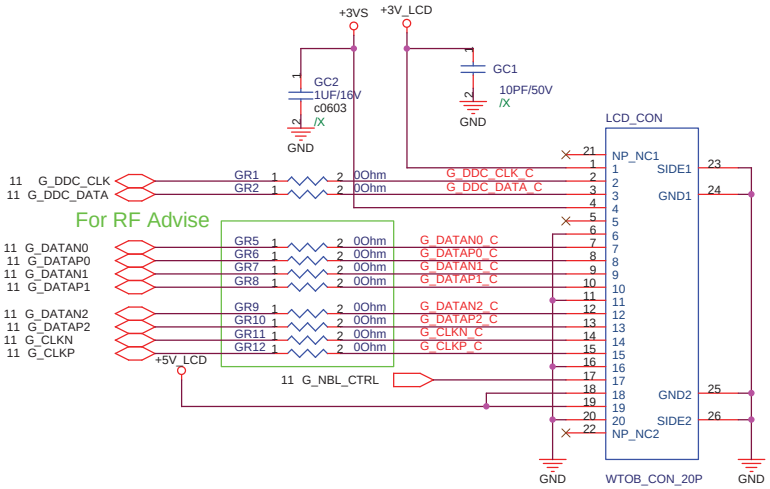
Title : Onboard VGA

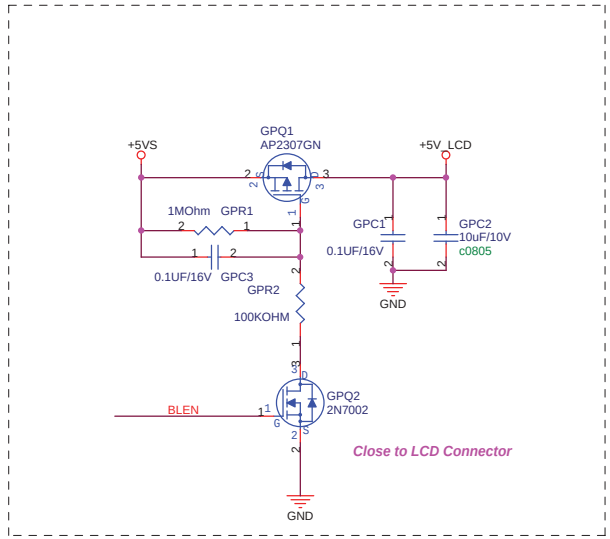
Engineer: Kell_Huang

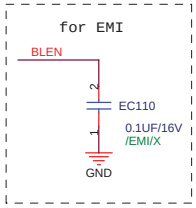
Size	Project Name	Rev
A3	900SD_MB	R1.0G

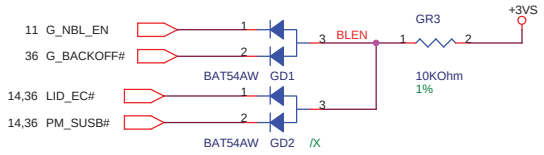
Date: Monday, November 10, 2008 Sheet 22 of 51

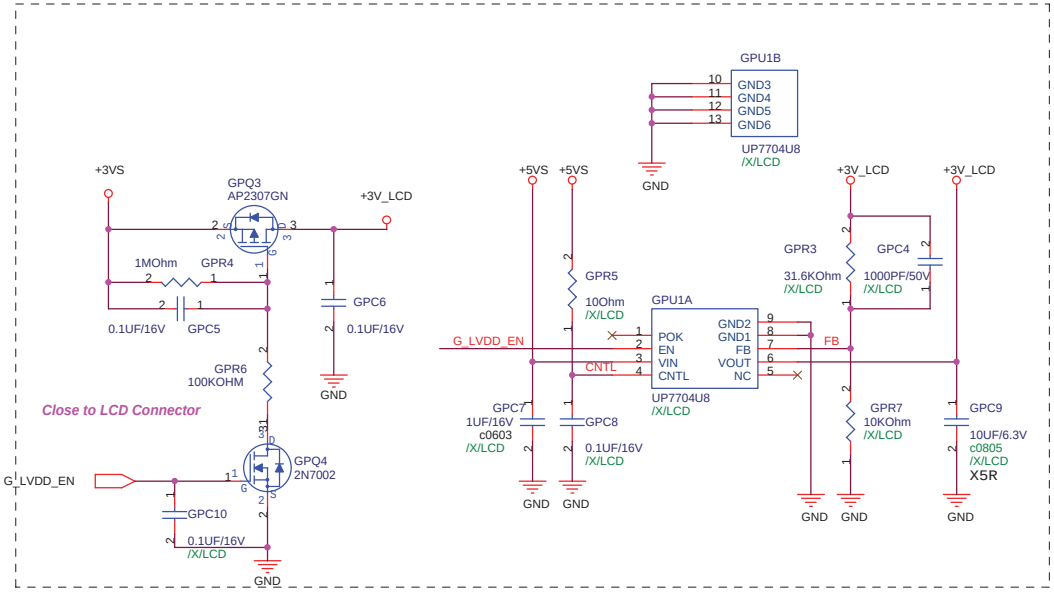
0.1 B Beta

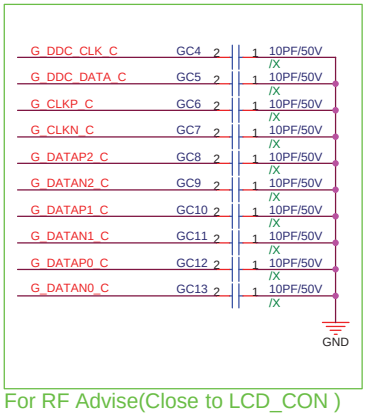


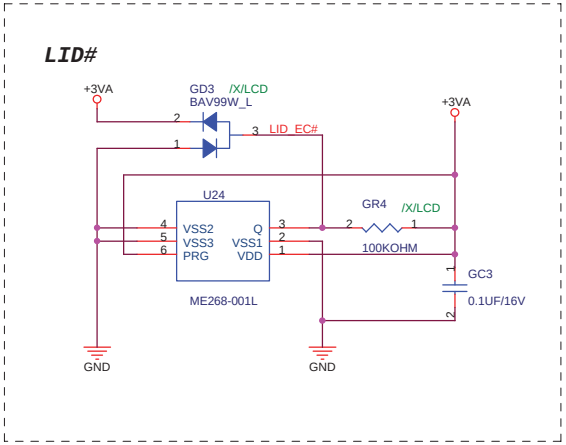






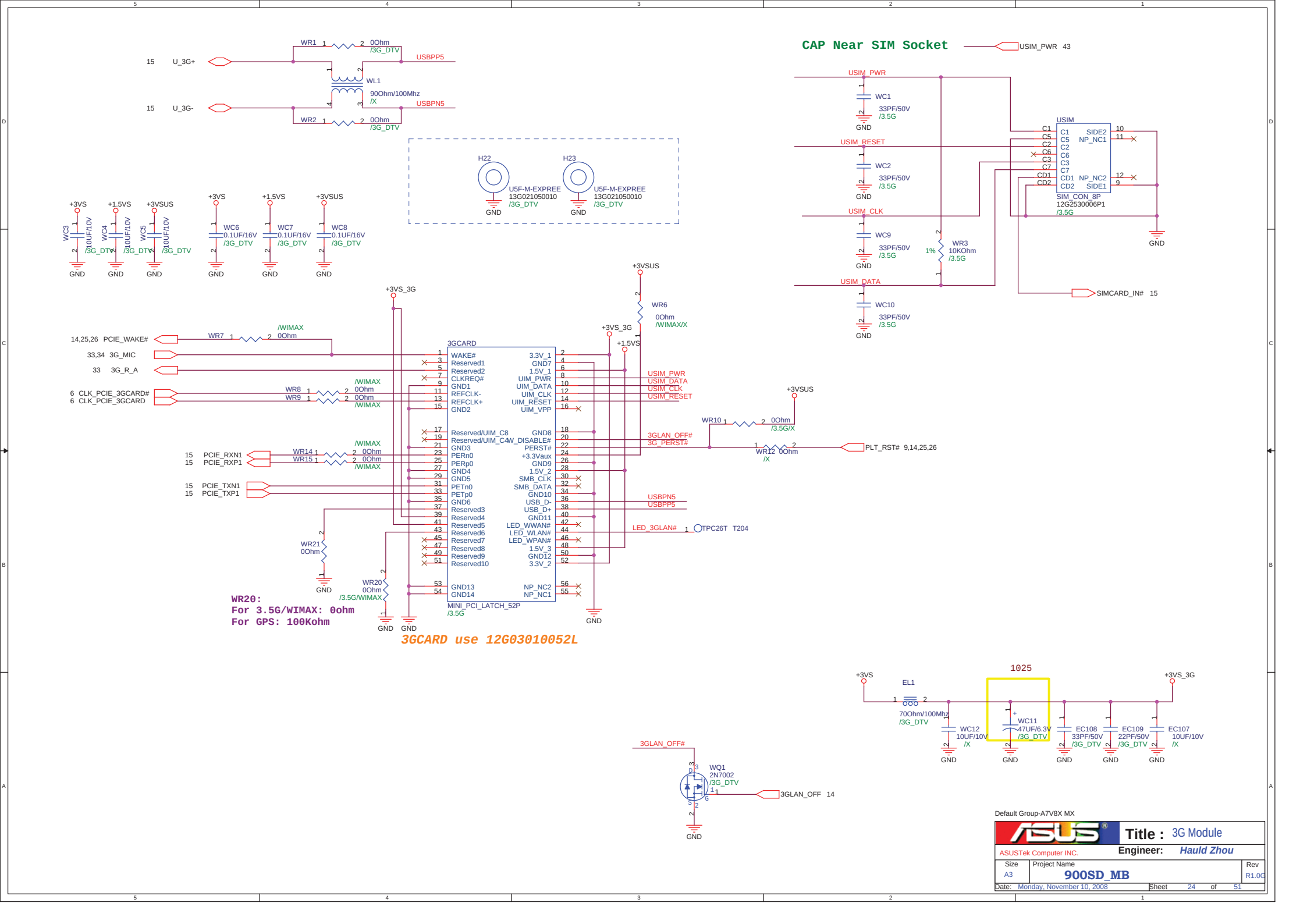


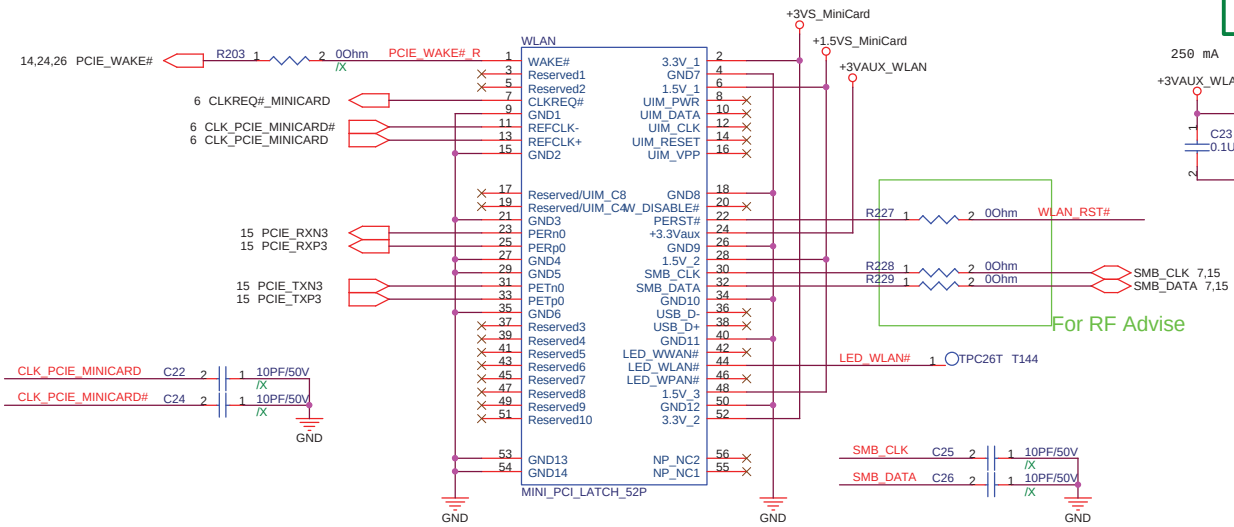




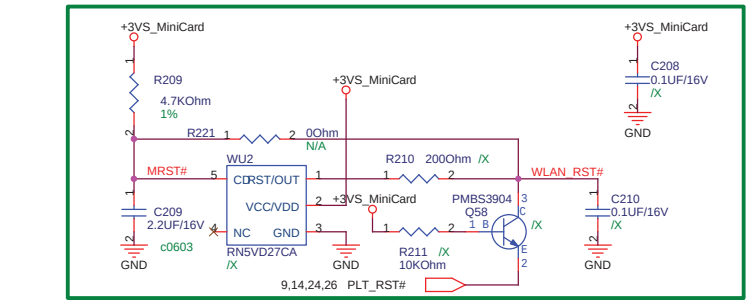
Default Group-A7V8X MX

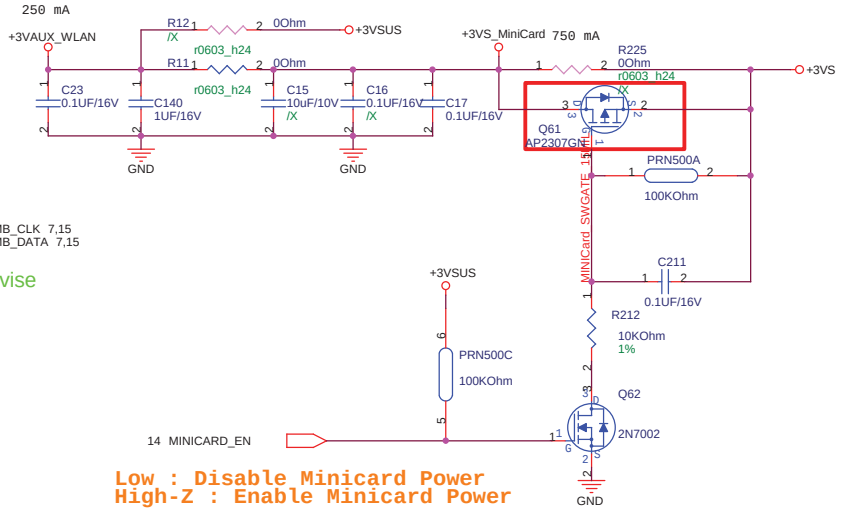
ASUSTek Computer Inc.	Title : LCD-CON for 10inch	
	Engineer: SUSAN_SHI	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 23 of 51	


CAP Near SIM Socket
USIM_PWR 43
WR1 0Ohm /3G_DTV
15 U_3G+
USBPP5
WL1
90Ohm/100Mhz /X
15 U_3G-
USBPN5
WR2 0Ohm /3G_DTV
H22 U5F-M-EXPREE 13G021050010 /3G_DTV
H23 U5F-M-EXPREE 13G021050010 /3G_DTV
GND
+3VS
+1.5VS
+3VSUS
WC3 10UF/10V /3G_DTV
WC4 10UF/10V /3G_DTV
WC5 10UF/10V /3G_DTV
WC6 0.1UF/16V /3G_DTV
WC7 0.1UF/16V /3G_DTV
WC8 0.1UF/16V /3G_DTV
USIM_PWR
WC1 33PF/50V /3.5G
USIM_RESET
WC2 33PF/50V /3.5G
USIM_CLK
WC9 33PF/50V /3.5G
WR3 10KOhm /3.5G 1%
USIM_DATA
WC10 33PF/50V /3.5G
USIM
C1 C5 C2 C6 C3 C7 CD1 CD2
SIDE2 NP_NC1 NP_NC2 SIDE1
SIM_CON_8P 12G2530006P1 /3.5G
SIMCARD_IN# 15
+3VS_3G
WR6 0Ohm /WIMAX/X
14,25,26 PCIE_WAKE#
WR7 /WIMAX 0Ohm
33,34 3G_MIC
33 3G_R_A
6 CLK_PCIE_3GCARD#
6 CLK_PCIE_3GCARD
WR8 /WIMAX 0Ohm
WR9 /WIMAX 0Ohm
3GCARD
WAKE# Reserved1 Reserved2 CLKREQ# GND1 REFCLK- REFCLK+ GND2
3.3V_1 GND7 1.5V_1 UIM_PWR UIM_DATA UIM_CLK UIM_RESET UIM_VPP
Reserved/UIM_C8 Reserved/UIM_C4 GND3 PERn0 PERp0 GND4 GND5 PETn0 PETp0 GND6 Reserved3 Reserved4 Reserved5 Reserved6 Reserved7 Reserved8 Reserved9 Reserved10
W_DISABLE# PERST# +3.3Vaux GND9 1.5V_2 SMB_CLK SMB_DATA GND10 USB_D- USB_D+ GND11 LED_WWAN# LED_WLAN# LED_WPAN# 1.5V_3 GND12 3.3V_2
GND13 GND14
NP_NC2 NP_NC1
MINI_PCI_LATCH_52P /3.5G
USIM_PWR
USIM_DATA
USIM_CLK
USIM_RESET
3GLAN_OFF#
3G_PERST#
USBPN5
USBPP5
LED_3GLAN#
TPC26T T204
15 PCIE_RXN1
15 PCIE_RXP1
WR14 /WIMAX 0Ohm
WR15 /WIMAX 0Ohm
15 PCIE_TXN1
15 PCIE_TXP1
WR10 0Ohm /3.5G/X
WR12 0Ohm /X
PLT_RST# 9,14,25,26
WR21 0Ohm
WR20 0Ohm /3.5G/WIMAX
WR20:
For 3.5G/WIMAX: 0ohm
For GPS: 100Kohm
3GCARD use 12G03010052L
1025
EL1 70Ohm/100Mhz /3G_DTV
WC12 10UF/10V /X
WC11 47UF/6.3V /3G_DTV
EC108 33PF/50V /3G_DTV
EC109 22PF/50V /3G_DTV
EC107 10UF/10V /X
3GLAN_OFF#
WQ1 2N7002 /3G_DTV
3GLAN_OFF 14
Default Group-A7V8X MX
ASUSTek Computer INC.
Title : 3G Module
Engineer: Hauld Zhou
Size A3
Project Name 900SD_MB
Rev R1.0G
Date: Monday, November 10, 2008
Sheet 24 of 51

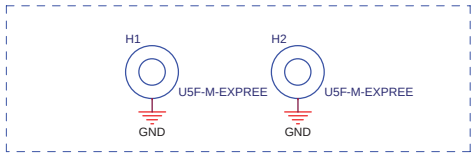


For RF Advise

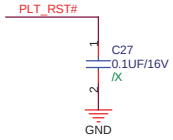


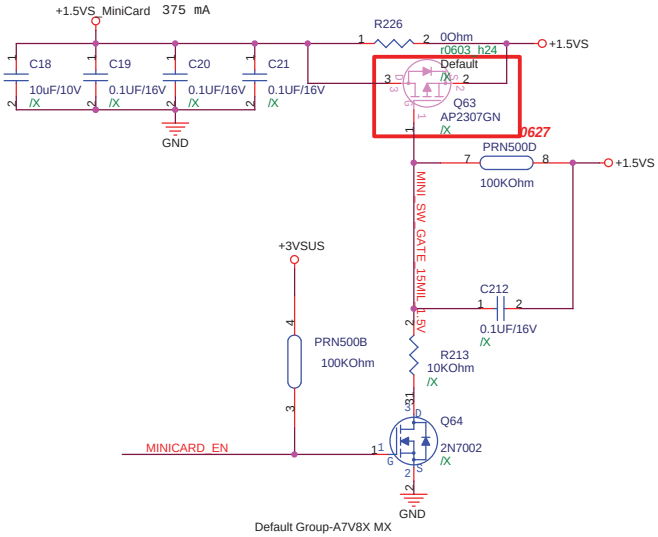


Low : Disable Minicard Power
High-Z : Enable Minicard Power



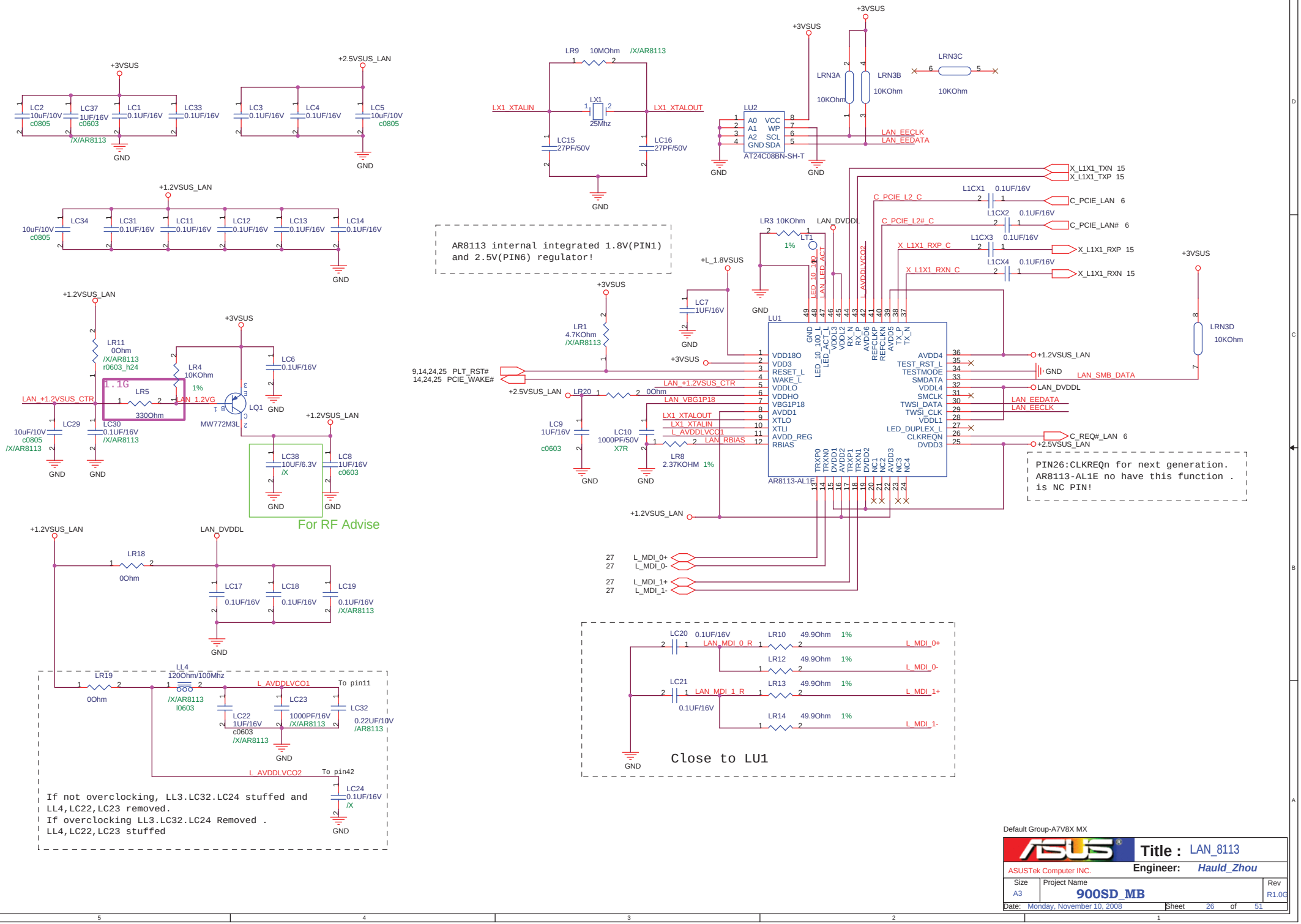
MINI CARD NUT(1.6mm) *2





Default Group-A7V8X MX

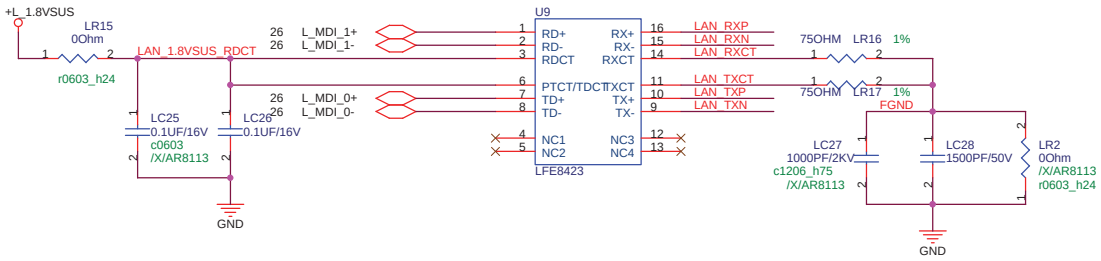
ASUSTek Computer INC.	Title : WLAN	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 25 of 51	

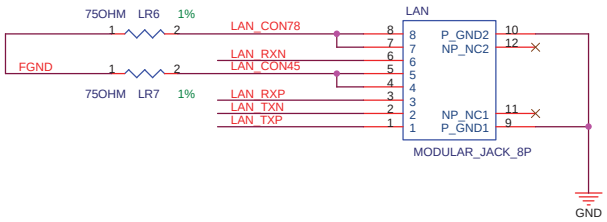


Default Group-A7V8X MX

ASUSTek Computer INC.	Title : LAN_8113	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 26 of 51	

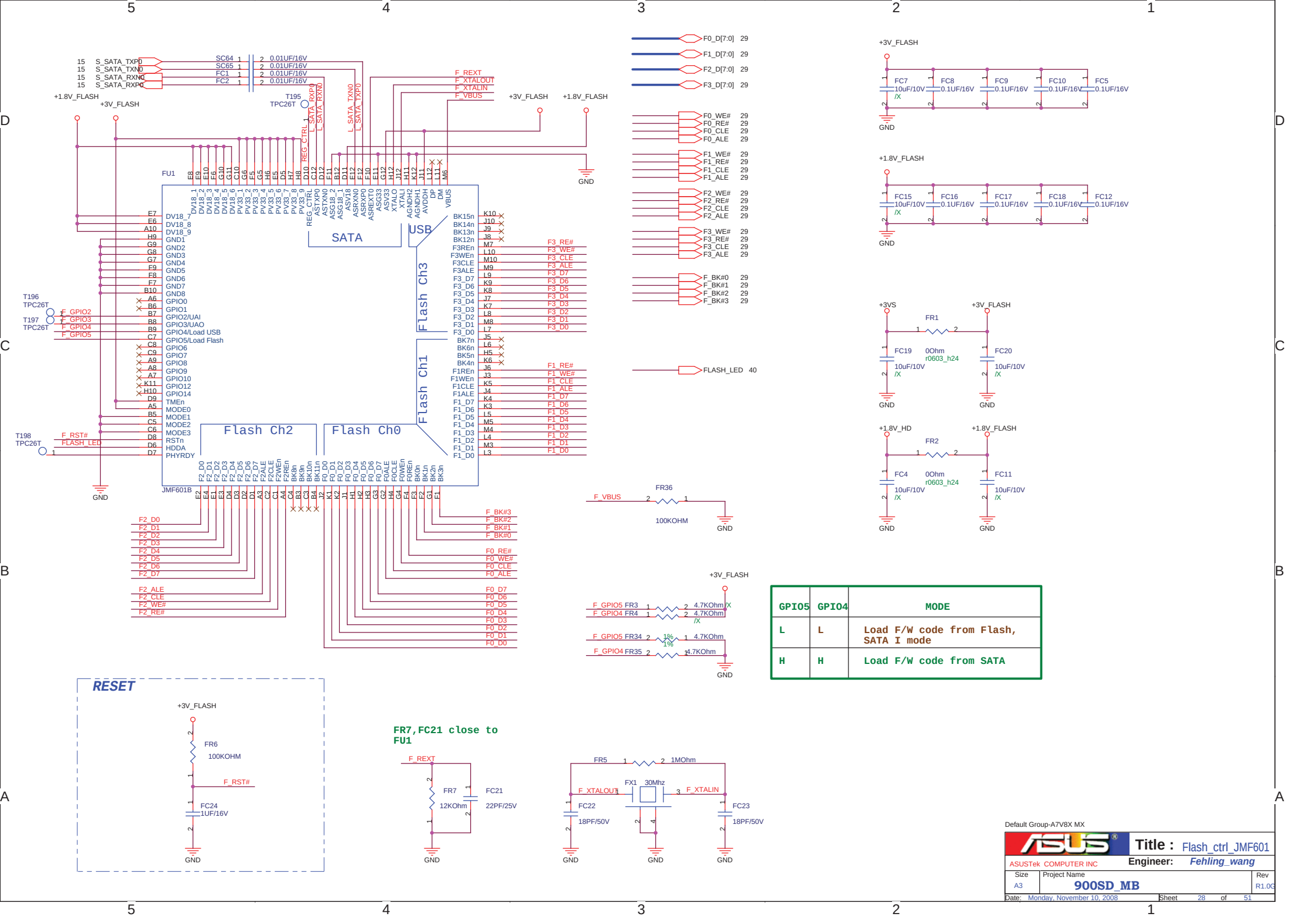
DELETE MODEM





Default Group-A7V8X MX

ASUSTek Computer INC.	Title : RJ45	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 27 of 51	



GPIO5	GPIO4	MODE
L	L	Load F/W code from Flash, SATA I mode
H	H	Load F/W code from SATA

Default Group-A7V8X MX

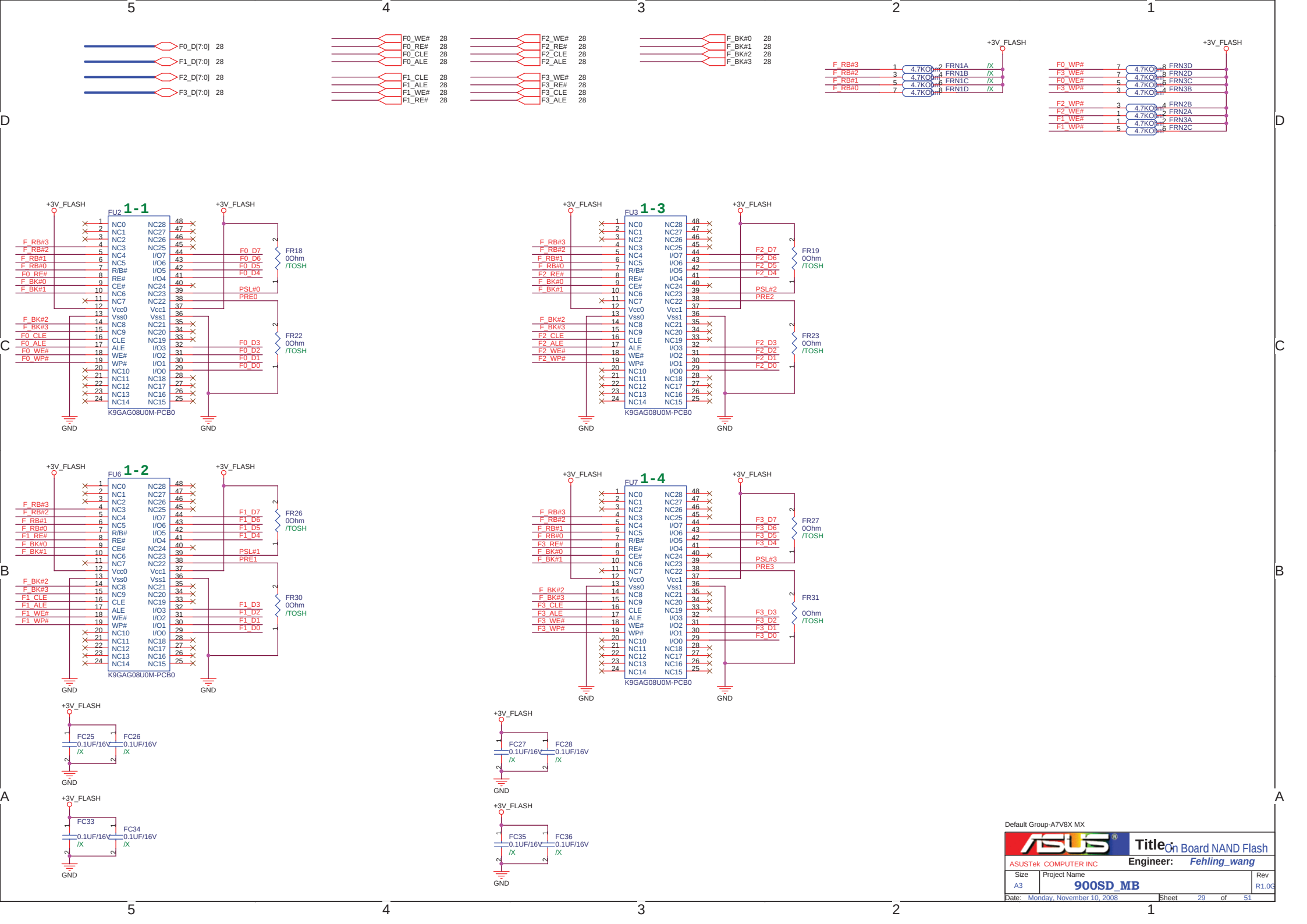
ASUSTek COMPUTER INC

Title : Flash_ctrl_JMF601

Engineer: Fehling_wang

Size	Project Name	Rev
A3	900SD_MB	R1.0G

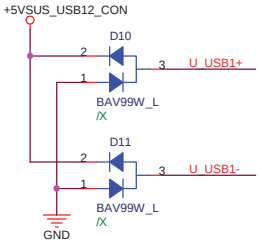
Date: Monday, November 10, 2008 Sheet 28 of 51

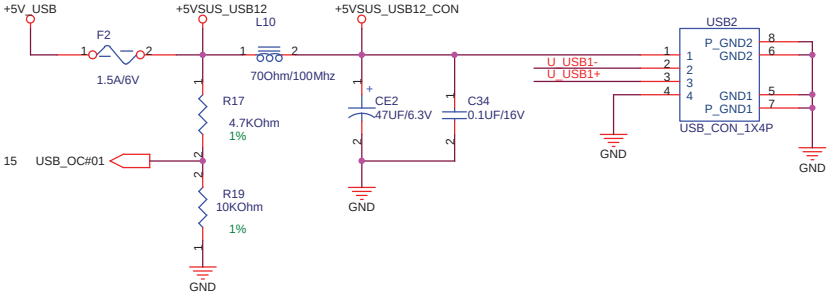


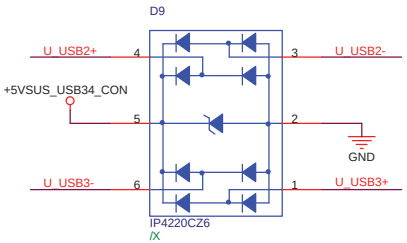
Default Group-A7V8X MX

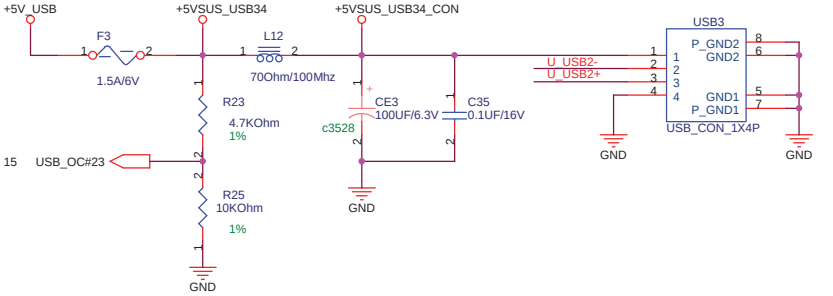
ASUSTek COMPUTER INC	Title: On Board NAND Flash	
	Engineer: Fehling_wang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 29 of 51	

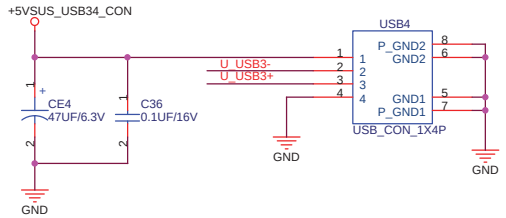






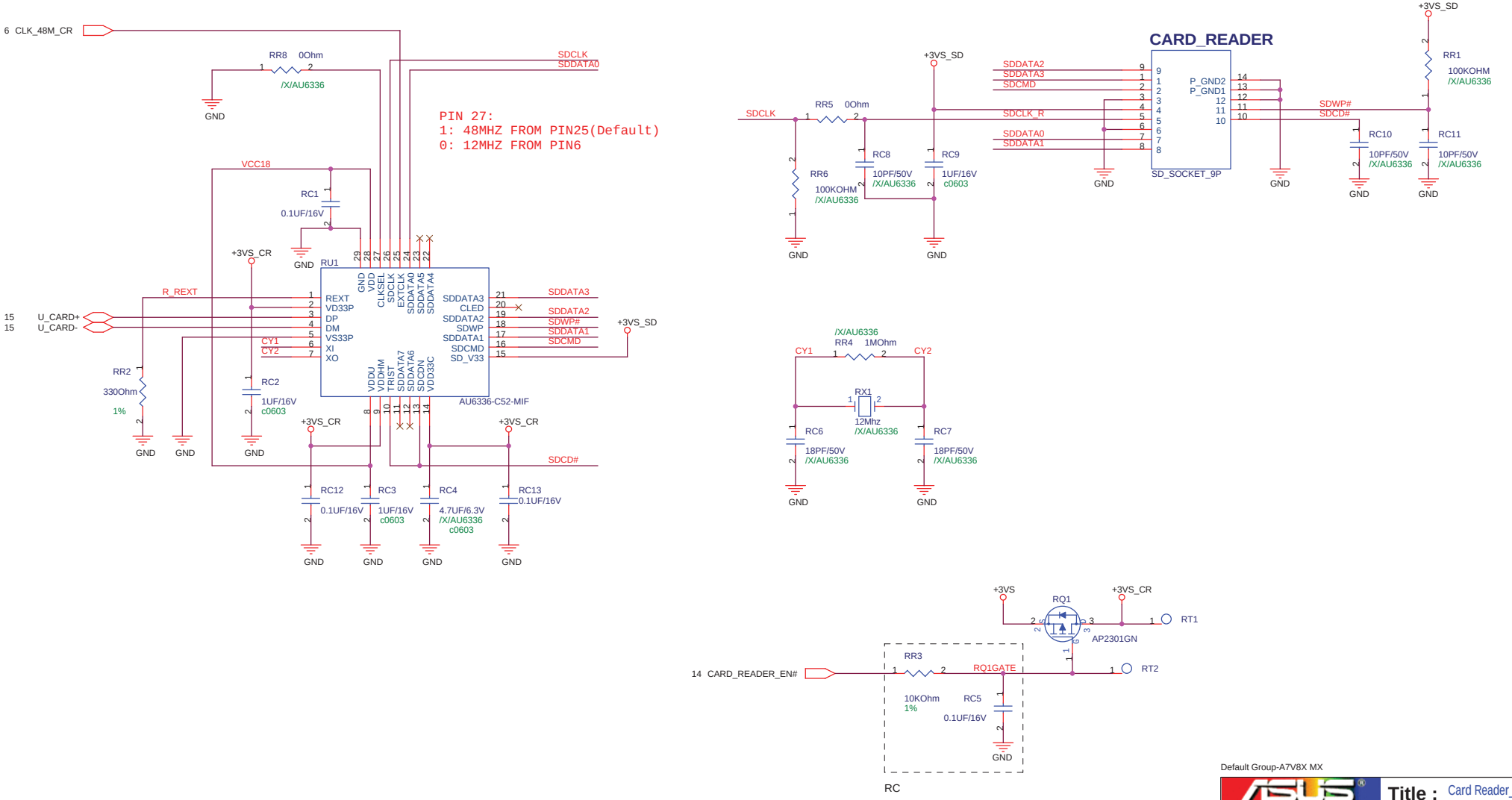






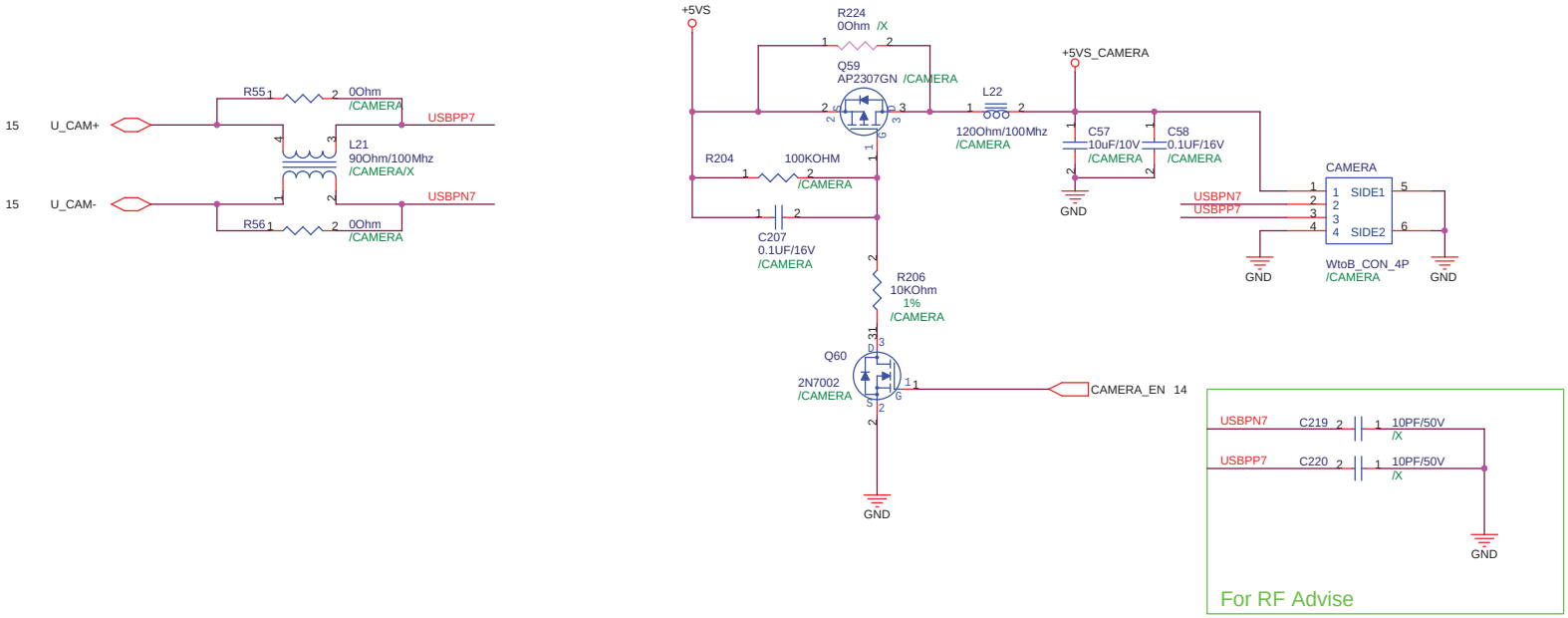
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : USB Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 30 of 51	



Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Card Reader_AU6336	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 31 of 51	



Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Camera Conn	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 32 of 51	

Vout=0.8*(1+(49.9K/10.2K))

+5VS
APU1
SHDN#
GND
IN
SET
OUT
APL5315BI-TRL
P_5VASET
APC1
1000PF/50V
/X/ALC269
X7R
APC10
10UF/16V
/X/ALC269
c0805
900SD R1.0G
APR2
10.2KOHM
1%
r0603
APR1
49.9KOHM
1%
APC11
1UF/16V
c0603
/X/ALC269
GND
+5V_A
APT1
TPC26T
APC6
10uF/10V
c0805
APC7
0.1UF/16V
/X/ALC269
APC8
10UF/16V
/X/ALC269
X5R
c0805
APC9
0.1UF/16V
AC5
0.1UF/16V
AC6
10UF/16V
c0805
X5R
/X/ALC269
A_GND
Place next to pin 38
Place next to pin 25

+5VS_PVDD
P_GND
A_SPK_R+_R 34
A_SPK_R-_R 34
A_SPK_L-_R 34
A_SPK_L+_R 34
+5VS_PVDD
+5V_A
A_GND
+3VS_DVDD
AU1A
GND
SPDIFO
EAPD/SPDIFO2
PVDD2
SPK_OUT_R-
SPK_OUT_R+
PVSS2
SPK_OUT_L-
SPK_OUT_L+
PVDD1
AVDD2
AVSS2
DVDD
GPIO0/DMIC_DATA
GPIO1/DMIC_CLK
PD#
SDATA_OUT
BCLK
DVSS
SDATA_IN
DVDD_IO
SYNC
RESET#
PCBEEP
CBP
CBN
CPVEE
HPOUT_R
HPOUT_L
CPVREF
MIC1_VREFO_R
MIC2_VREFO
MIC1_VREFO_L
VREF
AVSS1
AVDD1
A_CBP
AC1
2.2UF/16V
c0805
X7R
A_CBN
A_CPVEE
A_HP_R 34
A_HP_L 34
A_BIAS_MIC1_R 34
A_BIAS_MIC2 35
A_BIAS_MIC1_L 34
A_VREF
AC2
2.2UF/16V
c0805
X7R
AC3
0.1UF/16V
AC4
10UF/16V
c0805
X5R
/X/ALC269
+5V_A
A_GND
Place next to pin 27
A_PD#
14 A_Z_SDOUT
14 A_Z_BITCLK
14 A_Z_SDIN0
14 A_Z_SYNC
14 A_Z_RST#
33Ohm AR1
A_Z_SDIN0_R
/ALC269
A_PCBEEP
APT2
TPC26T
EC167
0.1UF/16V
AC33
22PF/25V
/X/ALC269
GND
ALC269Q-GR
SenseA
LINE2_L
LINE2_R
MIC2_L
MIC2_R
SenseB
MONO_OUT
MIC1_R
MIC1_L
LINE1_L
LINE1_R
JDREF
A_SENSE
A_MIC1_R 34
A_MIC1_L 34
AR5
20KOHM
1%
AR7 39.2KOhm 1%
AR8 20KOHM 1%
34 A_JD_HP
34 A_JD_MIC1
AC106 1UF/16V /3.5G/X
AC107 1UF/16V /3.5G/X
3G_R_A 24
R1.0G
AC108 1UF/16V /3.5G/X
3G_MIC 24,34
R1.0G
A_MIC2AMP_R 35
A_MIC2AMP_L 35

A_PD#	speaker AMP.
H	power down
L	power up

+5VS
AL2
120Ohm/100Mhz
l0603
+5VS_PVDD
APC12
0.1UF/16V
APC13
10uF/10V
c0805
APC14
0.1UF/16V
APC15
10UF/16V
/X/ALC269
c0805
X5R
ACE2
47UF/6.3V
c3528
/X
ACE1
100UF/6.3V
c7343d_h87
/X/ALC269
GND
Place next to pin 46
Place next to pin 39
P_GND

Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to uppress the surge.

36 A_OP_SD#
A_Z_RST#
A_PD#
AD1
BAT54AW
sot323

+3VS
AL1
120Ohm/100Mhz
l0603
+3VS_DVDD
APC2
0.1UF/16V
APC3
10uF/10V
c0805
/X/ALC269
APC4
0.1UF/16V
APC5
10UF/16V
/X/ALC269
c0805
X5R
Place next to pin 1
Place next to pin 9
GND

Digital plane
power plane
Analog plane

AU1B
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
ALC269Q-GR
P_GND

Default Group-A7V8X MX

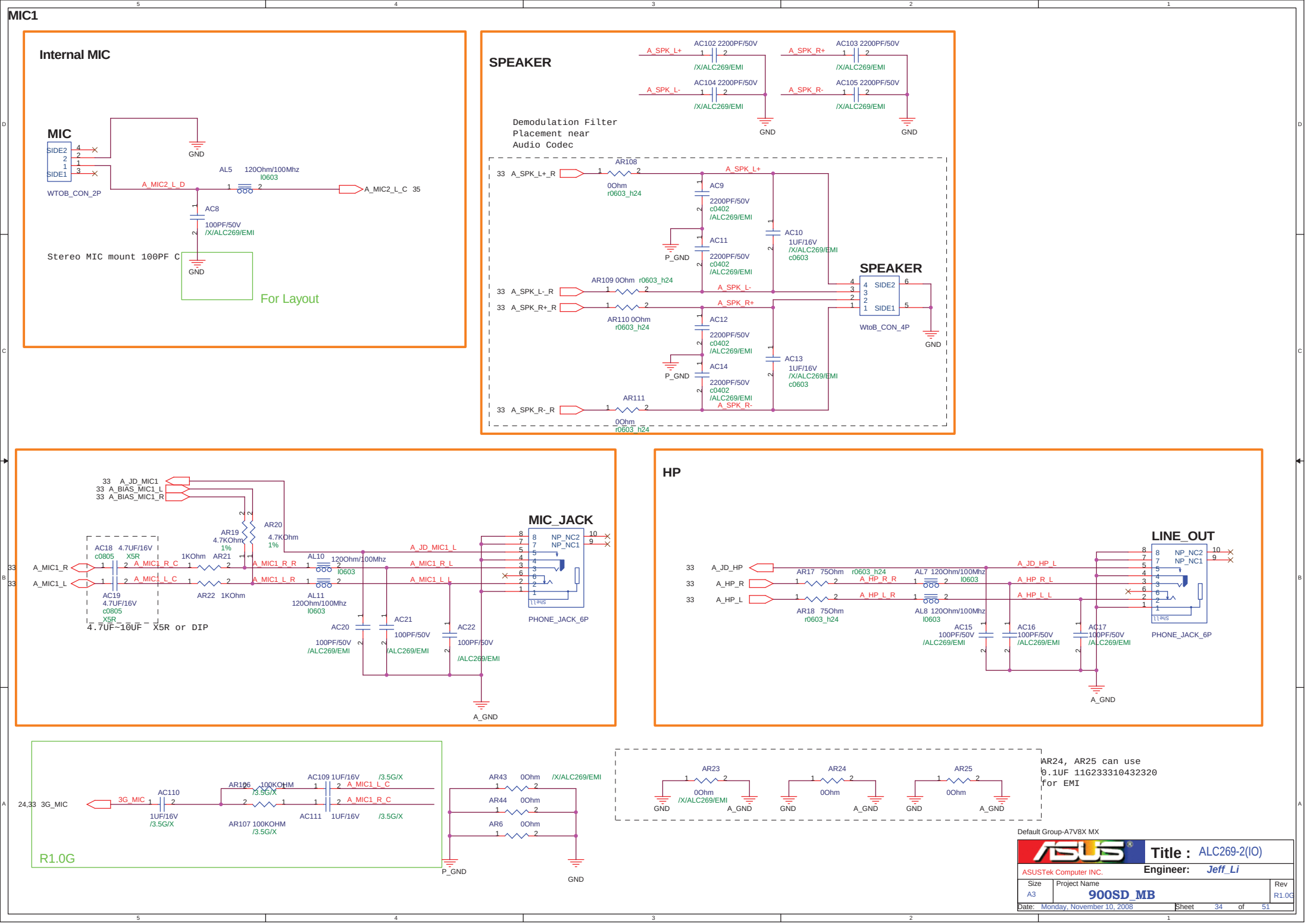
ASUSTek Computer INC.

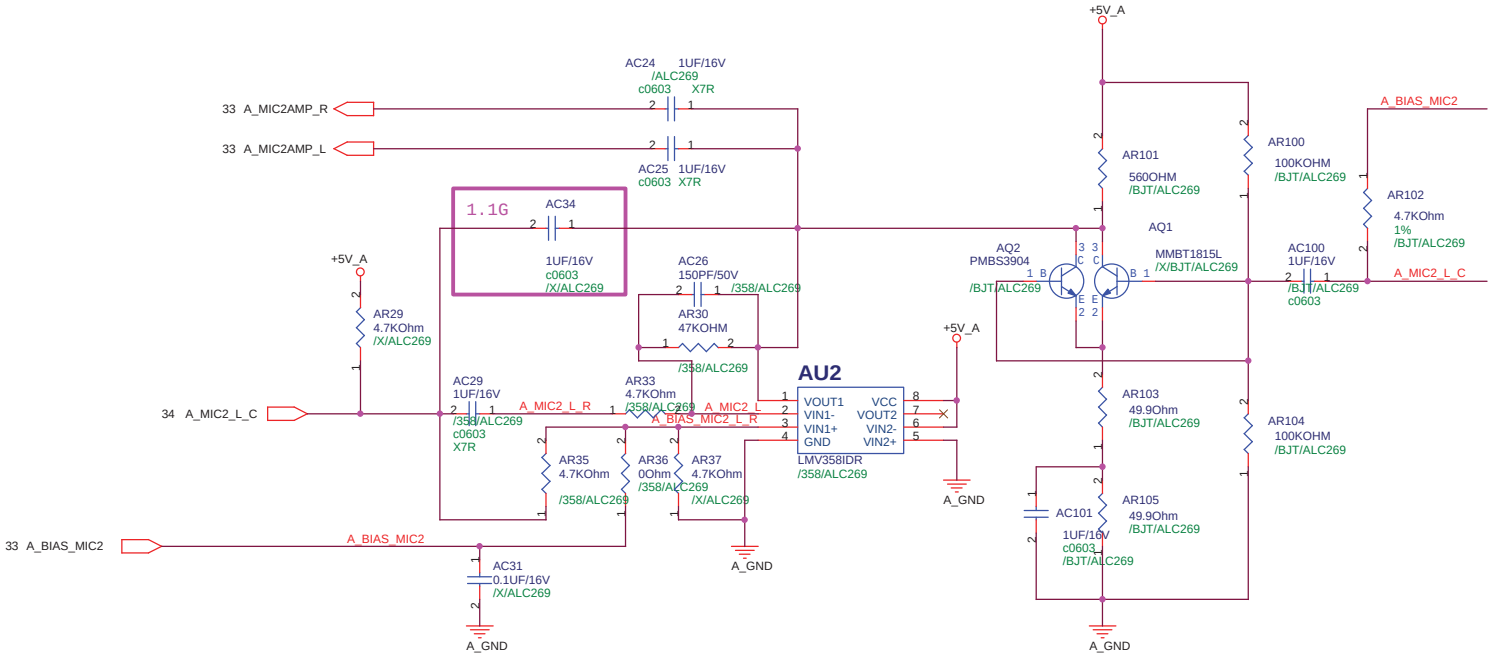
Title : ALC269-1

Engineer: Jeff_Li

Size	Project Name	Rev
A3	900SD_MB	R1.0G

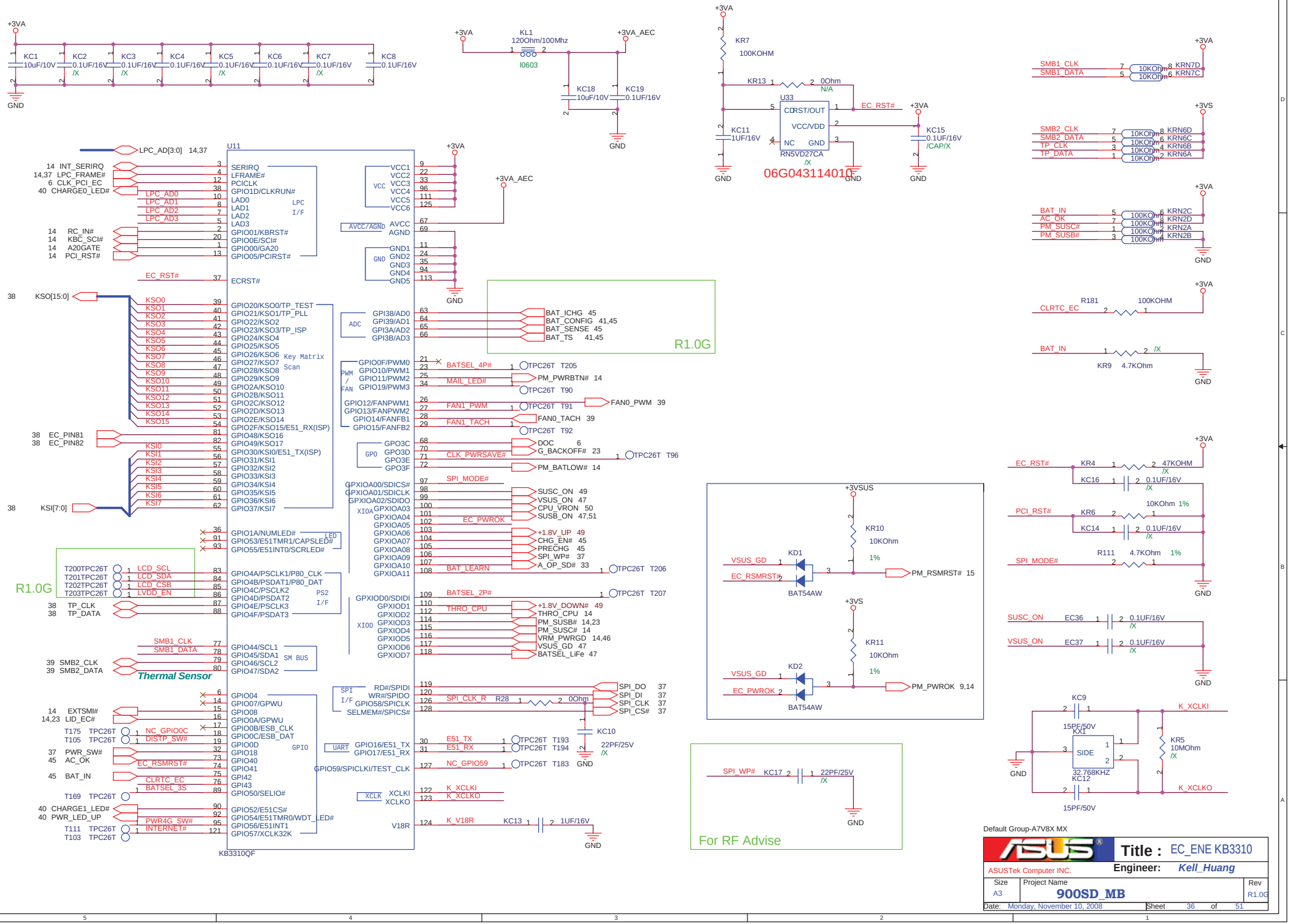
Date: Monday, November 10, 2008 Sheet 33 of 51

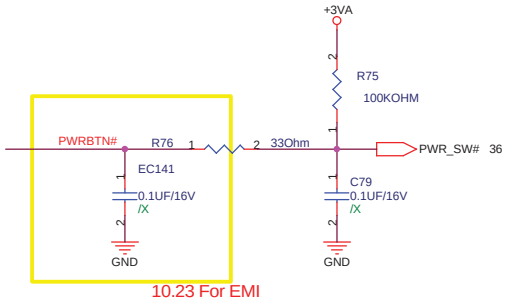

MIC1
Internal MIC
MIC
SIDE2
SIDE1
WTOB_CON_2P
GND
AL5 120Ohm/100Mhz
l0603
A_MIC2_L_D
A_MIC2_L_C 35
AC8
100PF/50V
/X/ALC269/EMI
Stereo MIC mount 100PF C
For Layout
SPEAKER
A_SPK_L+
AC102 2200PF/50V
/X/ALC269/EMI
A_SPK_R+
AC103 2200PF/50V
A_SPK_L-
AC104 2200PF/50V
A_SPK_R-
AC105 2200PF/50V
Demodulation Filter
Placement near
Audio Codec
33 A_SPK_L+_R
AR108
0Ohm
r0603_h24
AC9
2200PF/50V
c0402
/ALC269/EMI
AC10
1UF/16V
/X/ALC269/EMI
c0603
AC11
P_GND
AR109 0Ohm r0603_h24
33 A_SPK_L-_R
33 A_SPK_R+_R
AR110 0Ohm
r0603_h24
AC12
AC13
1UF/16V
/X/ALC269/EMI
c0603
AC14
33 A_SPK_R-_R
AR111
0Ohm
r0603_h24
SPEAKER
SIDE2
SIDE1
WtoB_CON_4P
33 A_JD_MIC1
33 A_BIAS_MIC1_L
33 A_BIAS_MIC1_R
AR19
4.7KOhm
1%
AR20
4.7KOhm
1%
AC18 4.7UF/16V
c0805 X5R
AC19
4.7UF/16V
c0805
X5R
4.7UF~10UF X5R or DIP
1KOhm AR21
AR22 1KOhm
A_MIC1_R
A_MIC1_L
A_MIC1_R_C
A_MIC1_L_C
A_MIC1_R_R
A_MIC1_L_R
AL10 120Ohm/100Mhz
l0603
AL11
120Ohm/100Mhz
l0603
A_JD_MIC1_L
A_MIC1_R_L
A_MIC1_L_L
MIC_JACK
NP_NC2
NP_NC1
PHONE_JACK_6P
AC20
100PF/50V
/ALC269/EMI
AC21
100PF/50V
/ALC269/EMI
AC22
100PF/50V
/ALC269/EMI
A_GND
HP
33 A_JD_HP
33 A_HP_R
33 A_HP_L
AR17 75Ohm r0603_h24
AR18 75Ohm
r0603_h24
A_HP_R_R
A_HP_L_R
AL7 120Ohm/100Mhz
l0603
AL8 120Ohm/100Mhz
l0603
A_JD_HP_L
A_HP_R_L
A_HP_L_L
LINE_OUT
NP_NC2
NP_NC1
PHONE_JACK_6P
AC15
100PF/50V
/ALC269/EMI
AC16
100PF/50V
/ALC269/EMI
AC17
100PF/50V
/ALC269/EMI
A_GND
24,33 3G_MIC
3G_MIC
AC110
1UF/16V
/3.5G/X
AR106 100KOHM
/3.5G/X
AR107 100KOHM
/3.5G/X
AC109 1UF/16V
/3.5G/X
AC111 1UF/16V
/3.5G/X
A_MIC1_L_C
A_MIC1_R_C
R1.0G
AR43 0Ohm /X/ALC269/EMI
AR44 0Ohm
AR6 0Ohm
P_GND
GND
AR23
0Ohm
/X/ALC269/EMI
AR24
0Ohm
AR25
0Ohm
AR24, AR25 can use
0.1UF 11G233310432320
for EMI
Default Group-A7V8X MX
Title : ALC269-2(IO)
ASUSTek Computer INC.
Engineer: Jeff_Li
Size A3
Project Name 900SD_MB
Rev R1.0G
Date: Monday, November 10, 2008
Sheet 34 of 51



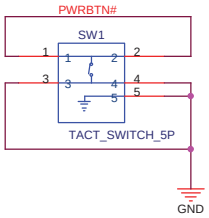
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : ALC269-3(MIC AMP)	
	Engineer: Jeff_Li	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 35 of 51	

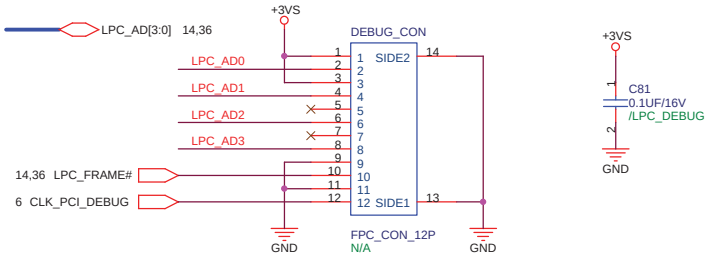

+3VA
KC1 10uF/10V
KC2 0.1UF/16V /X
KC3 0.1UF/16V /X
KC4 0.1UF/16V
KC5 0.1UF/16V /X
KC6 0.1UF/16V
KC7 0.1UF/16V /X
KC8 0.1UF/16V
GND
KL1 120Ohm/100Mhz 0603
+3VA_AEC
KC18 10uF/10V
KC19 0.1UF/16V
KR7 100KOHM
KR13 0Ohm N/A
U33 CRST/OUT VCC/VDD NC GND RN5VD27CA /X
EC_RST#
KC11 1UF/16V
KC15 0.1UF/16V /CAP/X
06G043114010
SMB1_CLK
SMB1_DATA
SMB2_CLK
SMB2_DATA
TP_CLK
TP_DATA
BAT_IN
AC_OK
PM_SUSC#
PM_SUSB#
10KOhm
100KOhm
KRN7D
KRN7C
KRN6D
KRN6C
KRN6B
KRN6A
KRN2C
KRN2D
KRN2A
KRN2B
R181 100KOHM
CLRTC_EC
KR9 4.7KOhm
U11
KB3310QF
LPC_AD[3:0] 14,37
SERIRQ
LFRAME#
PCICLK
GPIO1D/CLKRUN#
LAD0
LAD1
LAD2
LAD3
GPIO01/KBRST#
GPIO0E/SCI#
GPIO00/GA20
GPIO05/PCIRST#
LPC I/F
ECRST#
KSO[15:0]
KSI[7:0]
Key Matrix Scan
GPIO20/KSO0/TP_TEST
GPIO21/KSO1/TP_PLL
GPIO22/KSO2
GPIO23/KSO3/TP_ISP
GPIO24/KSO4
GPIO25/KSO5
GPIO26/KSO6
GPIO27/KSO7
GPIO28/KSO8
GPIO29/KSO9
GPIO2A/KSO10
GPIO2B/KSO11
GPIO2C/KSO12
GPIO2D/KSO13
GPIO2E/KSO14
GPIO2F/KSO15/E51_RX(ISP)
GPIO48/KSO16
GPIO49/KSO17
GPIO30/KSI0/E51_TX(ISP)
GPIO31/KSI1
GPIO32/KSI2
GPIO33/KSI3
GPIO34/KSI4
GPIO35/KSI5
GPIO36/KSI6
GPIO37/KSI7
EC_PIN81
EC_PIN82
VCC1 VCC2 VCC3 VCC4 VCC5 VCC6
AVCC/AGND AVCC AGND
GND1 GND2 GND3 GND4 GND5
ADC GPI38/AD0 GPI39/AD1 GPI3A/AD2 GPI3B/AD3
BAT_ICHG 45
BAT_CONFIG 41,45
BAT_SENSE 45
BAT_TS 41,45
R1.0G
PWM / FAN GPIO0F/PWM0 GPIO10/PWM1 GPIO11/PWM2 GPIO19/PWM3
GPIO12/FANPWM1
GPIO13/FANPWM2
GPIO14/FANFB1
GPIO15/FANFB2
BATSEL_4P#
MAIL_LED#
FAN1_PWM
FAN1_TACH
PM_PWRBTN# 14
TPC26T T205
TPC26T T90
TPC26T T91
TPC26T T92
FAN0_PWM 39
FAN0_TACH 39
GPO GPO3C GPO3D GPO3E GPO3F
CLK_PWRSAVE#
DOC 6
G_BACKOFF# 23
PM_BATLOW# 14
TPC26T T96
SPI_MODE#
XIOA GPXIOA00/SDICS# GPXIOA01/SDICLK GPXIOA02/SDIDO GPXIOA03 GPXIOA04 GPXIOA05 GPXIOA06 GPXIOA07 GPXIOA08 GPXIOA09 GPXIOA10 GPXIOA11
EC_PWROK
SUSC_ON 49
VSUS_ON 47
CPU_VRON 50
SUSB_ON 47,51
+1.8V_UP 49
CHG_EN# 45
PRECHG 45
SPI_WP# 37
A_OP_SD# 33
BAT_LEARN
TPC26T T206
XIOD GPXIOD0/SDIDI GPXIOD1 GPXIOD2 GPXIOD3 GPXIOD4 GPXIOD5 GPXIOD6 GPXIOD7
BATSEL_2P#
THRO_CPU
+1.8V_DOWN# 49
THRO_CPU 14
PM_SUSB# 14,23
PM_SUSC# 14
VRM_PWRGD 14,46
VSUS_GD 47
BATSEL_LiFe 47
TPC26T T207
LED
GPIO1A/NUMLED#
GPIO53/E51TMR1/CAPSLED#
GPIO55/E51INT0/SCRLED#
PS2 I/F
GPIO4A/PSCLK1/P80_CLK
GPIO4B/PSDAT1/P80_DAT
GPIO4C/PSCLK2
GPIO4D/PSDAT2
GPIO4E/PSCLK3
GPIO4F/PSDAT3
T200TPC26T LCD_SCL
T201TPC26T LCD_SDA
T202TPC26T LCD_CSB
T203TPC26T LVDD_EN
TP_CLK
TP_DATA
R1.0G
SM BUS
GPIO44/SCL1
GPIO45/SDA1
GPIO46/SCL2
GPIO47/SDA2
SMB1_CLK
SMB1_DATA
SMB2_CLK
SMB2_DATA
Thermal Sensor
SPI I/F RD#/SPIDI WR#/SPIDO GPIO58/SPICLK SELMEM#/SPICS#
SPI_CLK_R R28 0Ohm
SPI_DO 37
SPI_DI 37
SPI_CLK 37
SPI_CS# 37
KC10 22PF/25V /X
UART GPIO16/E51_TX GPIO17/E51_RX
E51_TX
E51_RX
TPC26T T193
TPC26T T194
GPIO59/SPICLKI/TEST_CLK
NC_GPIO59
TPC26T T183
XCLK XCLKI XCLKO
K_XCLKI
K_XCLKO
V18R
K_V18R
KC13 1UF/16V
GPIO
NC_GPIO0C
DISTP_SW#
PWR_SW#
AC_OK
EC_RSMRST#
BAT_IN
CLRTC_EC
BATSEL_3S
TPC26T T175
TPC26T T105
TPC26T T169
EXTSMI#
LID_EC#
CHARGE1_LED#
PWR_LED_UP
PWR4G_SW#
INTERNET#
TPC26T T111
TPC26T T103
+3VSUS
KR10 10KOhm 1%
KD1 BAT54AW
VSUS_GD
EC_RSMRST#
PM_RSMRST# 15
+3VS
KR11 10KOhm 1%
KD2 BAT54AW
EC_PWROK
PM_PWROK 9,14
SPI_WP#
KC17 22PF/25V /X
For RF Advise
EC_RST#
KR4 47KOHM /X
KC16 0.1UF/16V /X
PCI_RST#
KR6 10KOhm 1%
KC14 0.1UF/16V /X
R111 4.7KOhm 1%
SUSC_ON
EC36 0.1UF/16V /X
VSUS_ON
EC37 0.1UF/16V /X
KC9 15PF/50V
KX1 SIDE 32.768KHZ
KC12 15PF/50V
KR5 10MOhm /X
K_XCLKI
K_XCLKO
Default Group-A7V8X MX
ASUSTek Computer INC.
Title : EC_ENE KB3310
Engineer: Kell_Huang
Size A3
Project Name 900SD_MB
Rev R1.0G
Date: Monday, November 10, 2008
Sheet 36 of 51

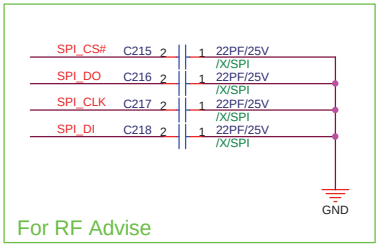


10.23 For EMI

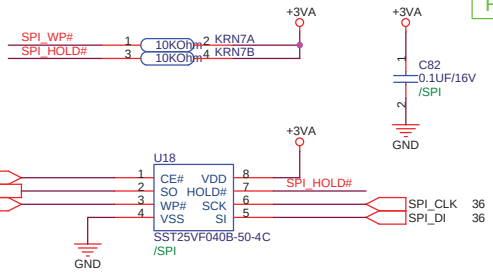


For Debug





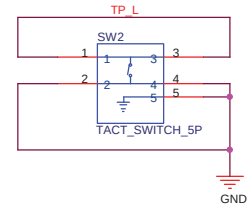
For RF Advise

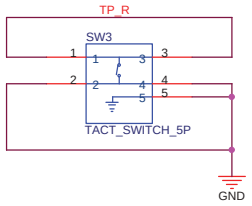


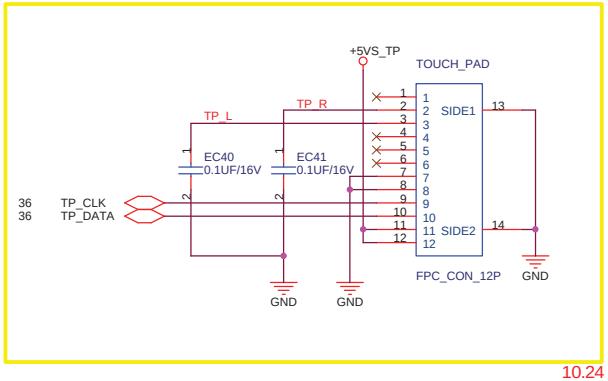
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Switch_SPI ROM	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 37 of 51	

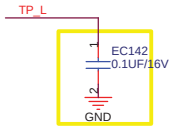
For Touch-Pad





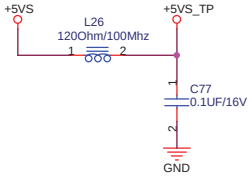


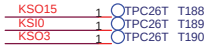
10.24

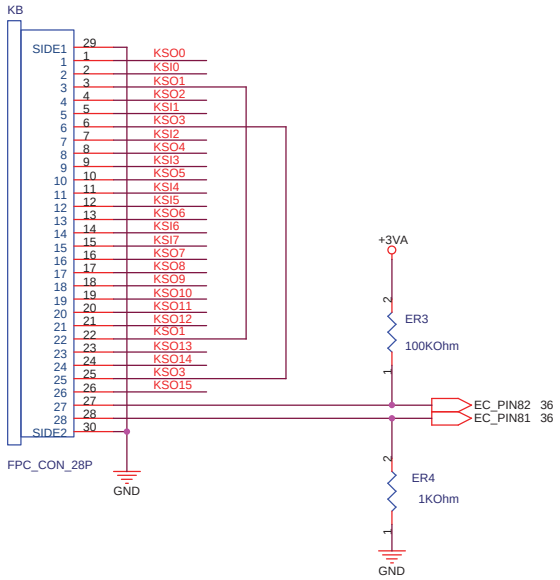


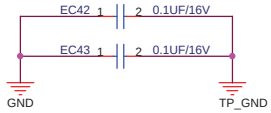
10.23 For EMI

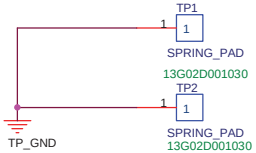
For Keyboard



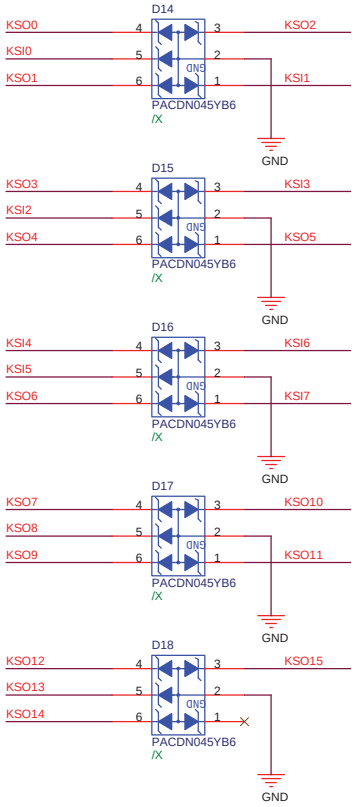


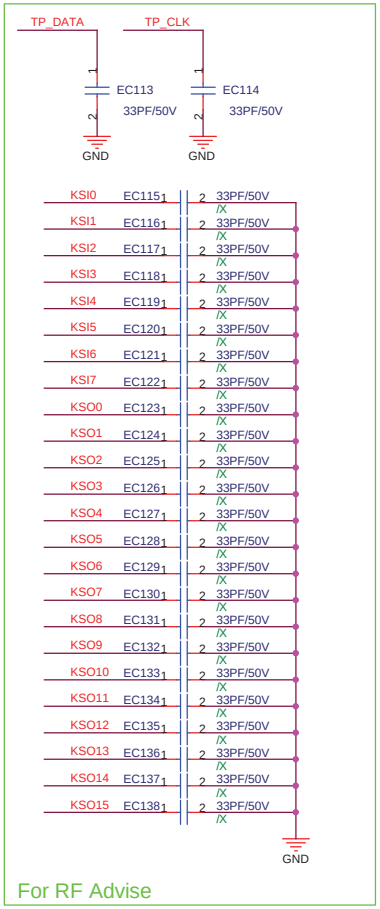








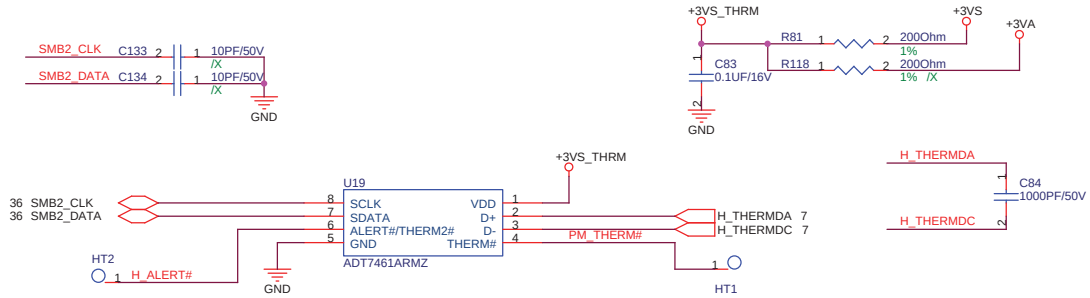




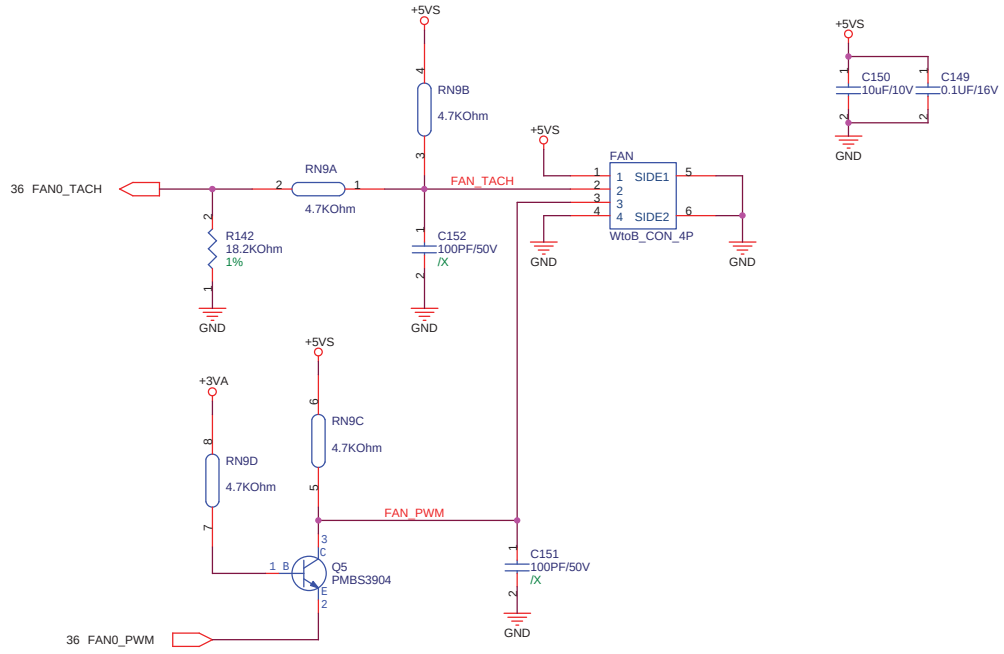
For RF Advise

Default Group-A7V8X MX

ASUSTek Computer INC.	Title : KB_Touch Pad	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 38 of 51	



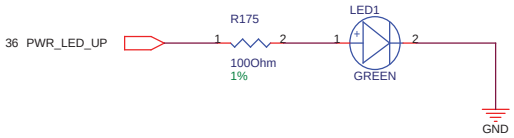
U19 use 06G023048021



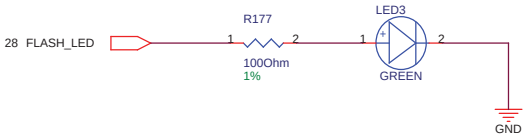
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Thermal Sensor_FAN	
	Engineer: *Kell_Huang*	
Size: A3	Project Name: **900SD_MB**	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 39 of 51	

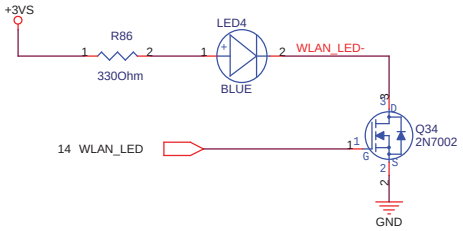
for POWER LED



for FLASH LED

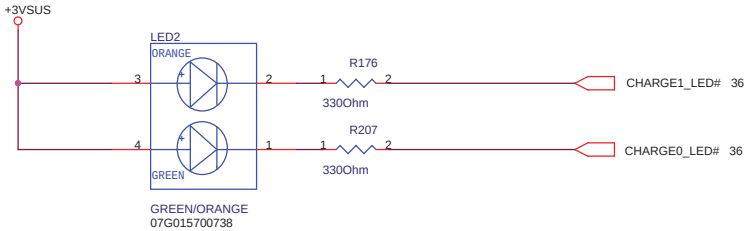


for WLAN LED



R1.0G

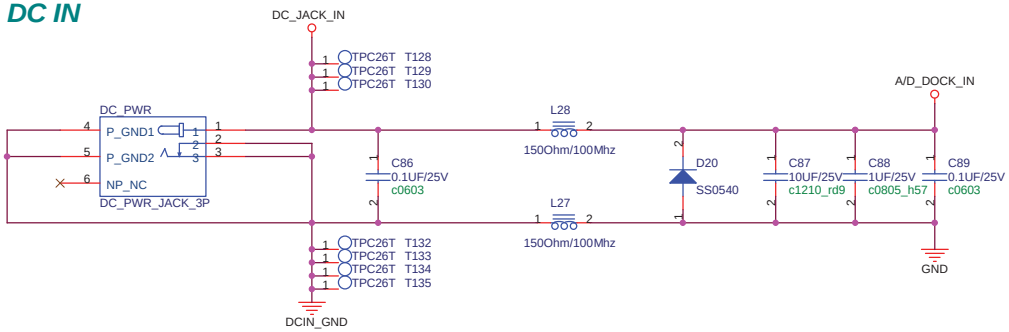
for CHARGE LED



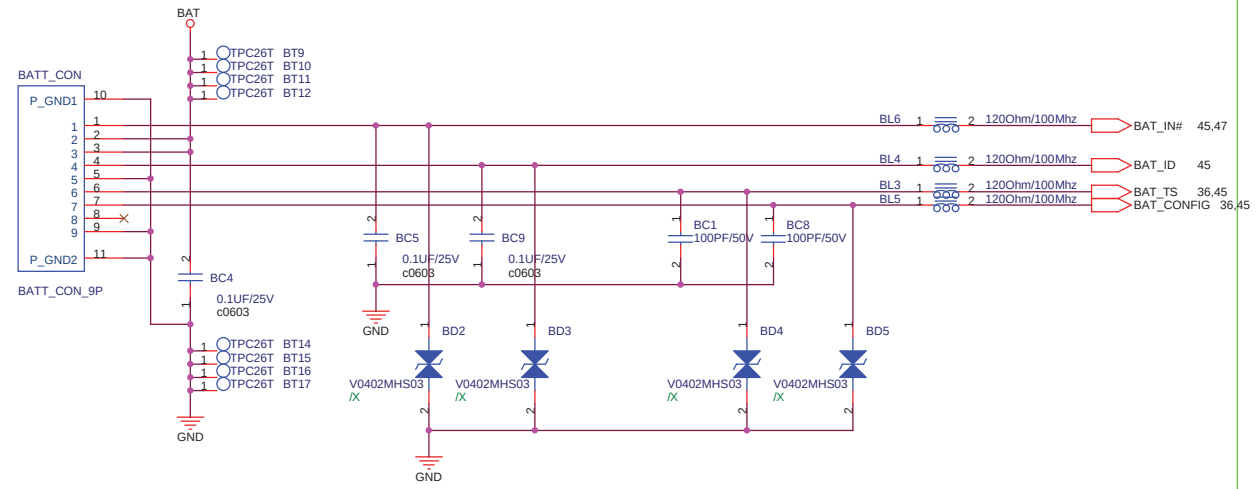
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : LED	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 40 of 51	

DC IN

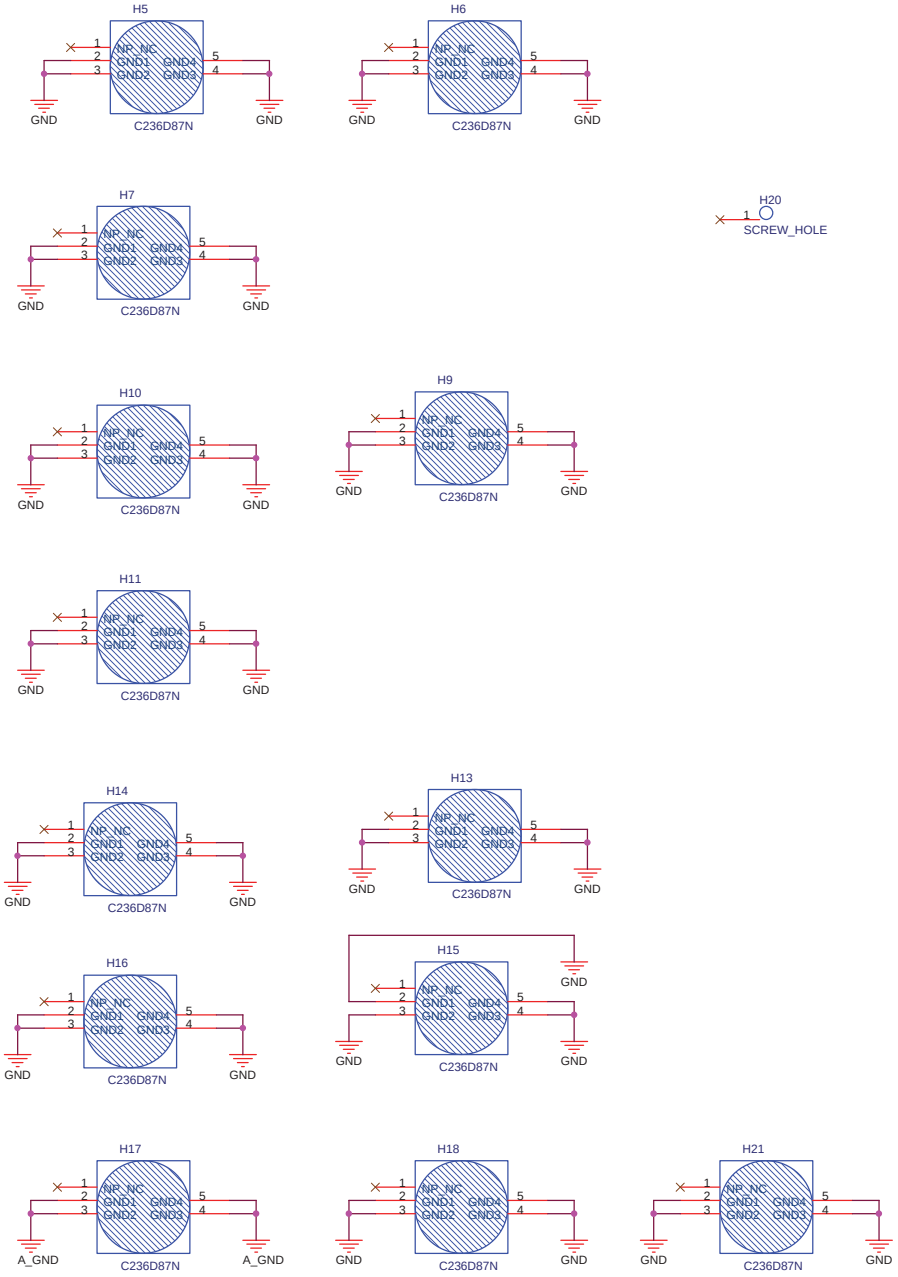


BAT IN



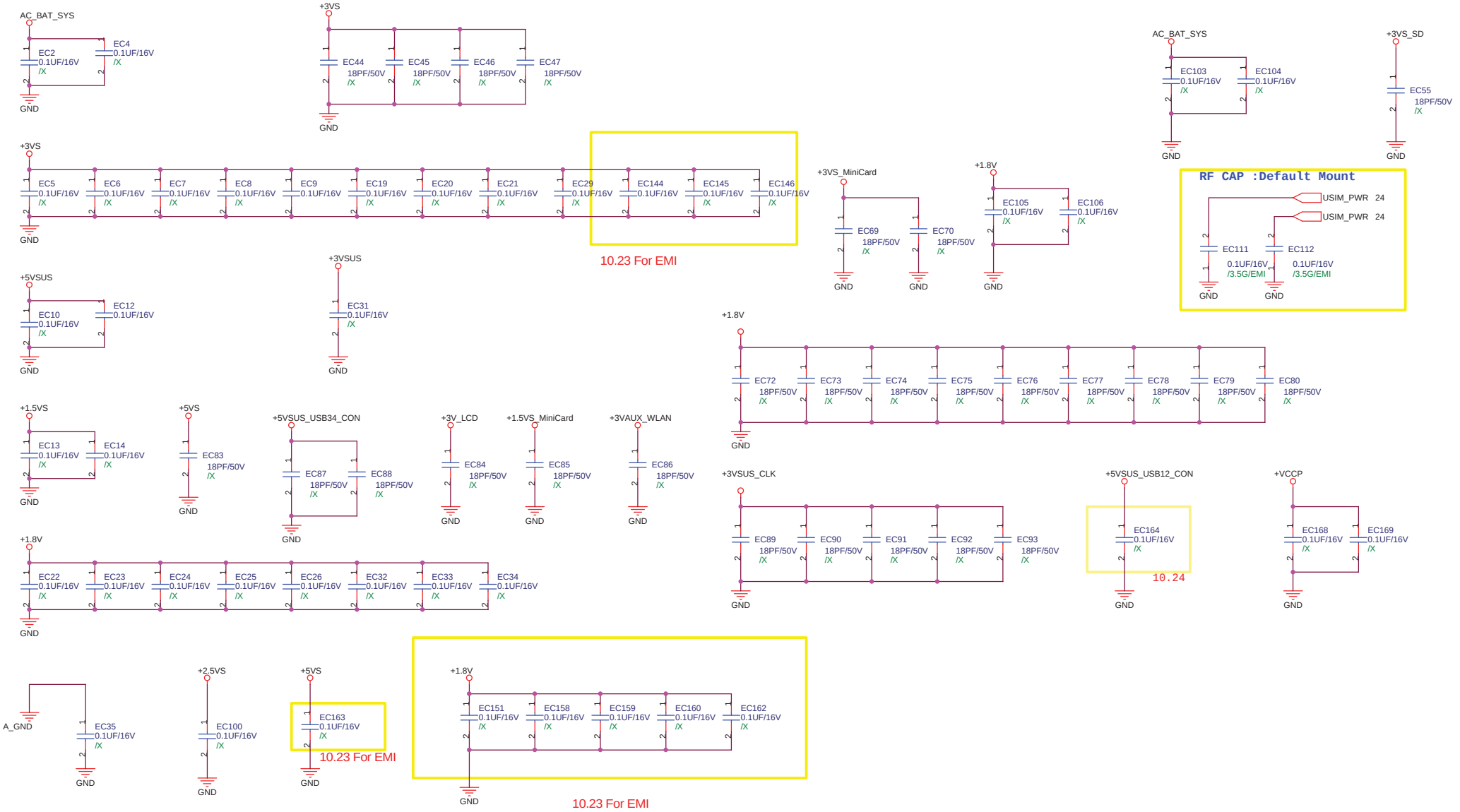
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 41 of 51	



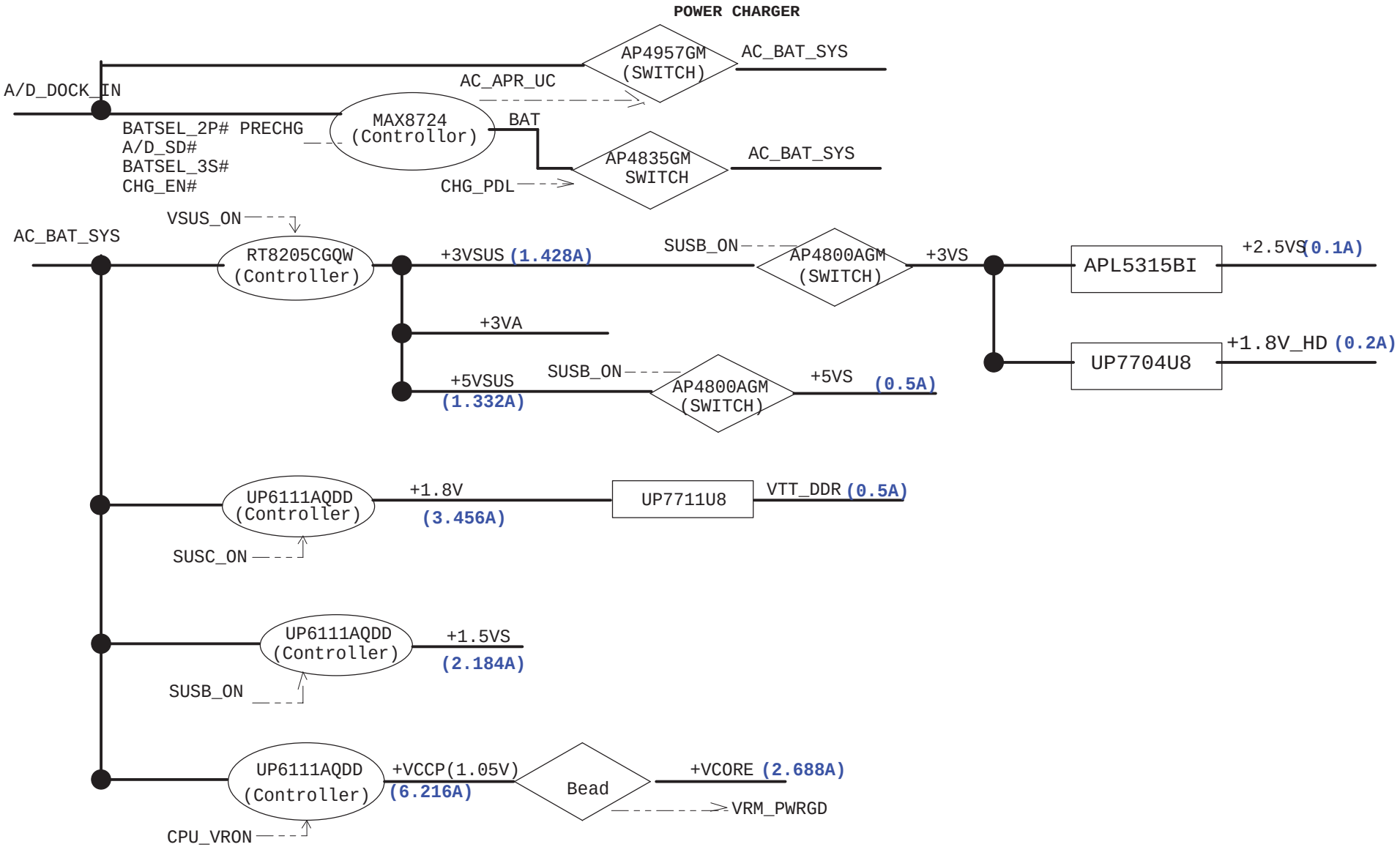
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Srew Hole	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 42 of 51	



Default Group-A7V8X MX

ASUSTek Computer INC.	Title : EMI	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 43 of 51	



Default Group-A7V8X MX

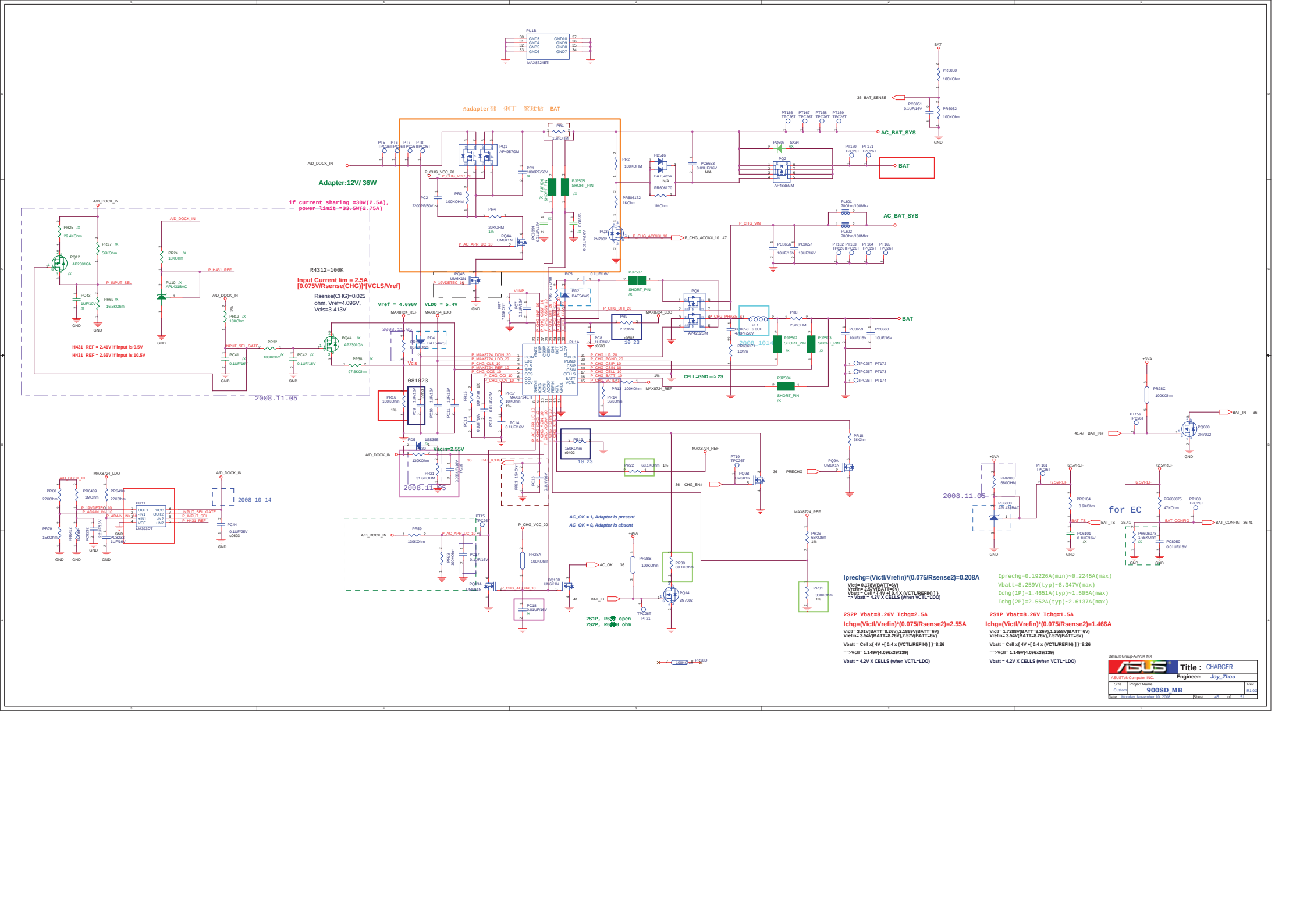
ASUSTek Computer INC.

Title : Power Flow

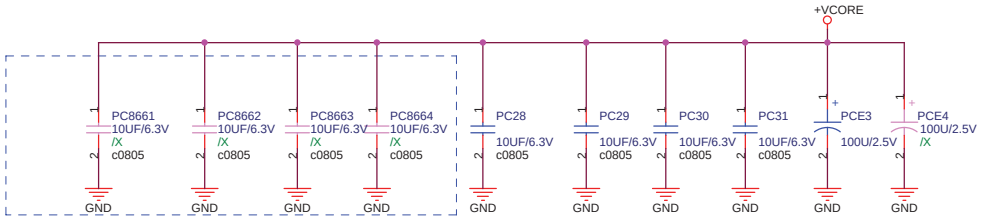
Engineer: Joy_Zhou

Size	Project Name	Rev
A3	900SD_MB	R1.0G

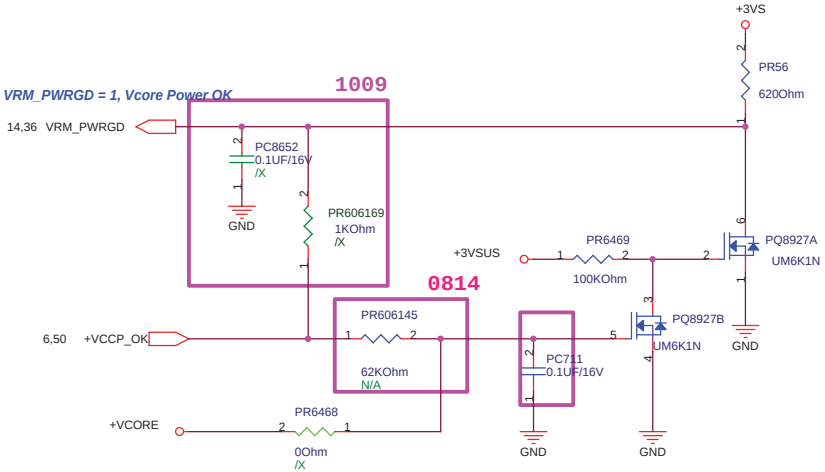
Date: Monday, November 10, 2008 Sheet 44 of 51


adapter砸 俐丁 篆球拈 BAT
Adapter:12V/ 36W
if current sharing =30W(2.5A), power limit =33.5W(2.75A)
R4312=100K
Input Current lim = 2.5A
[0.075V/Rsense(CHG)]*[VCLS/Vref]
Rsense(CHG)=0.025 ohm, Vref=4.096V, Vcls=3.413V
Vref = 4.096V
VL00 = 5.4V
H431_REF = 2.41V if input is 9.5V
H431_REF = 2.66V if input is 10.5V
CELL=GND ---> 2S
Vacin=2.55V
AC_OK = 1, Adaptor is present
AC_OK = 0, Adaptor is absent
2008.11.05
2008-10-14
for EC
AC_BAT_SYS
BAT
Iprechg=(Victl/Vrefin)*(0.075/Rsense2)=0.208A
Victl= 0.176V(BATT=6V)
Vrefin= 2.57V(BATT=6V)
Vbatt = Cell * [4V +[0.4 x (VCTLREFIN)]]
=> Vbatt = 4.2V X CELLS (when VCTL=LDO)
Iprechg=0.19226A(min)~0.2245A(max)
Vbatt=8.259V(typ)~8.347V(max)
Ichg(1P)=1.4651A(typ)~1.505A(max)
Ichg(2P)=2.552A(typ)~2.6137A(max)
2S2P Vbat=8.26V Ichg=2.5A
Ichg=(Victl/Vrefin)*(0.075/Rsense2)=2.55A
Victl= 3.01V(BATT=8.26V),2.1869V(BATT=6V)
Vrefin= 3.54V(BATT=8.26V),2.57V(BATT=6V)
Vbatt = Cell x{ 4V +[0.4 x (VCTLREFIN)] }=8.26
==>Vctl= 1.149V(4.096x39/139)
Vbatt = 4.2V X CELLS (when VCTL=LDO)
2S1P, R6[illegible] open
2S2P, R6[illegible] 0 ohm
2S1P Vbat=8.26V Ichg=1.5A
Ichg=(Victl/Vrefin)*(0.075/Rsense2)=1.466A
Victl= 1.7288V(BATT=8.26V),1.2558V(BATT=6V)
Vrefin= 3.54V(BATT=8.26V),2.57V(BATT=6V)
Vbatt = Cell x{ 4V +[0.4 x (VCTLREFIN)] }=8.26
==>Vctl= 1.149V(4.096x39/139)
Vbatt = 4.2V X CELLS (when VCTL=LDO)
Default Group-A7V8X MX
Title : CHARGER
ASUSTek Computer INC.
Engineer: Joy_Zhou
Size: Custom
Project Name: 900SD_MB
Rev: R1.0C
Date: Monday, November 10, 2008
Sheet 45 of 53

+Vcore / 7A



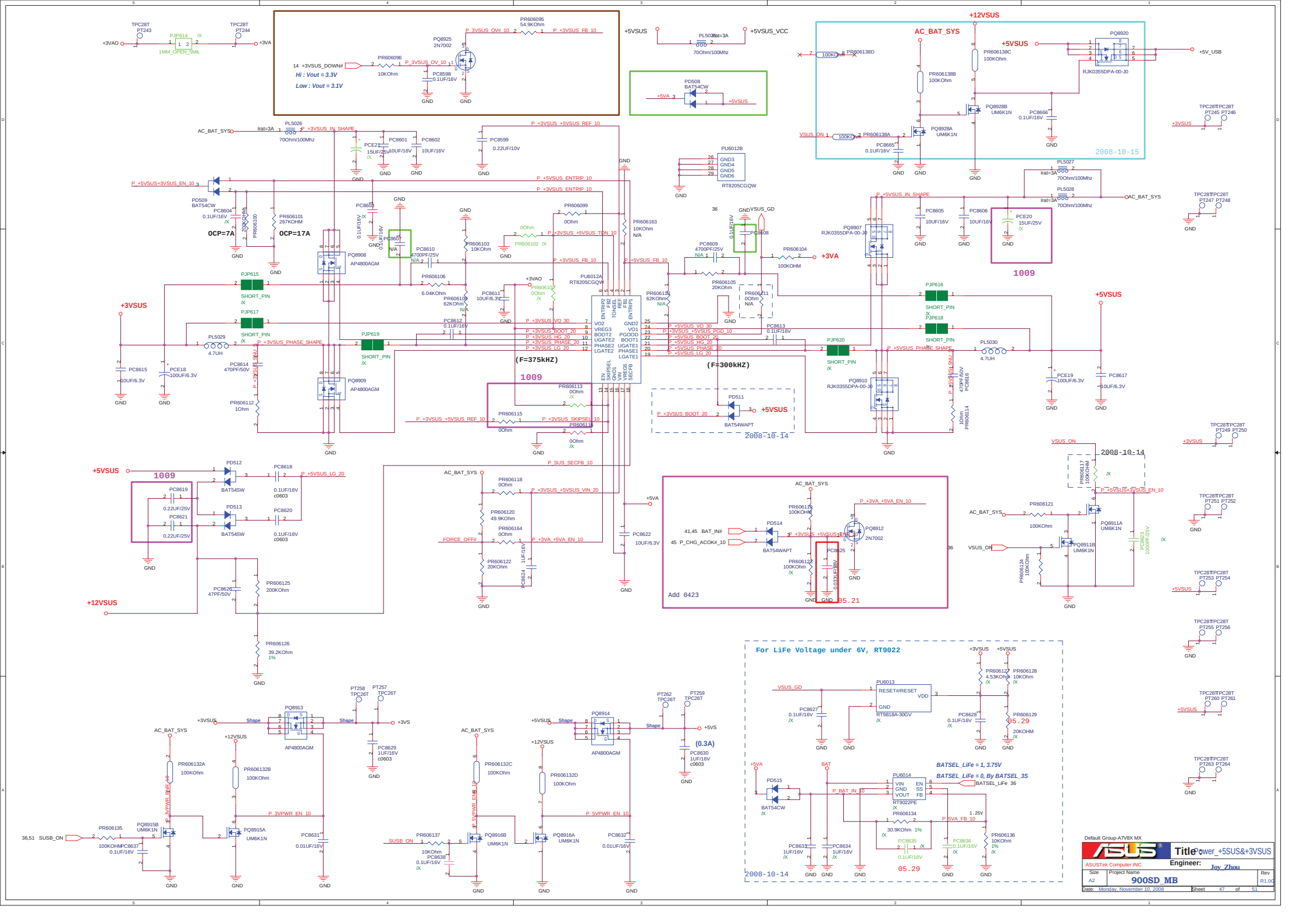
2008-10-15



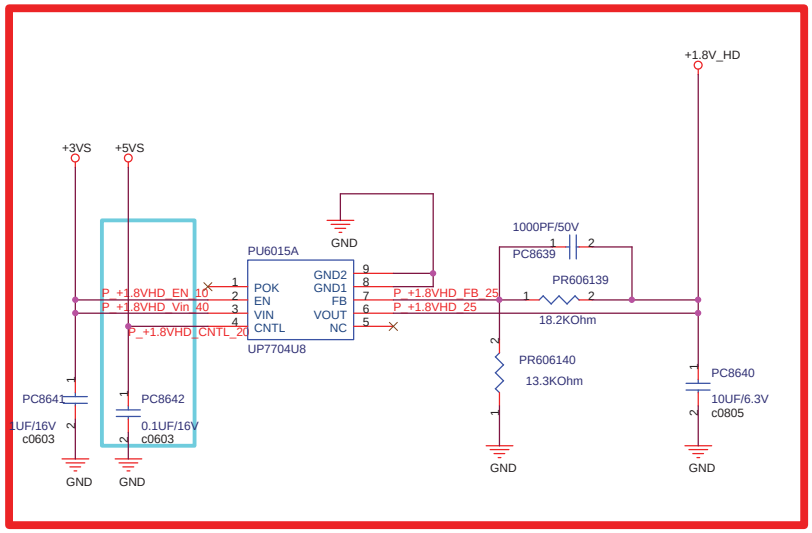


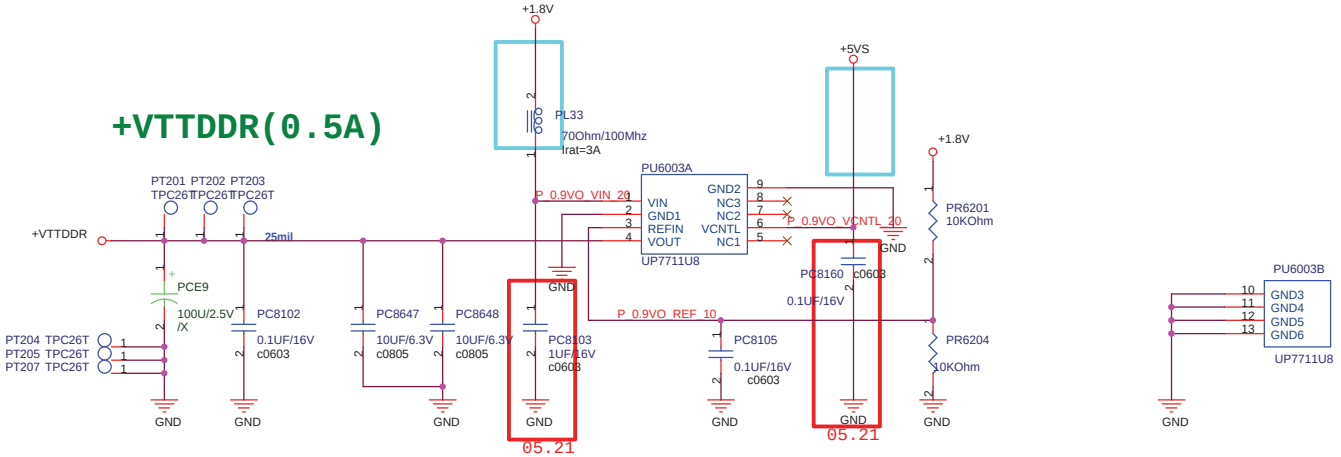
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Vcore	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 46 of 51	



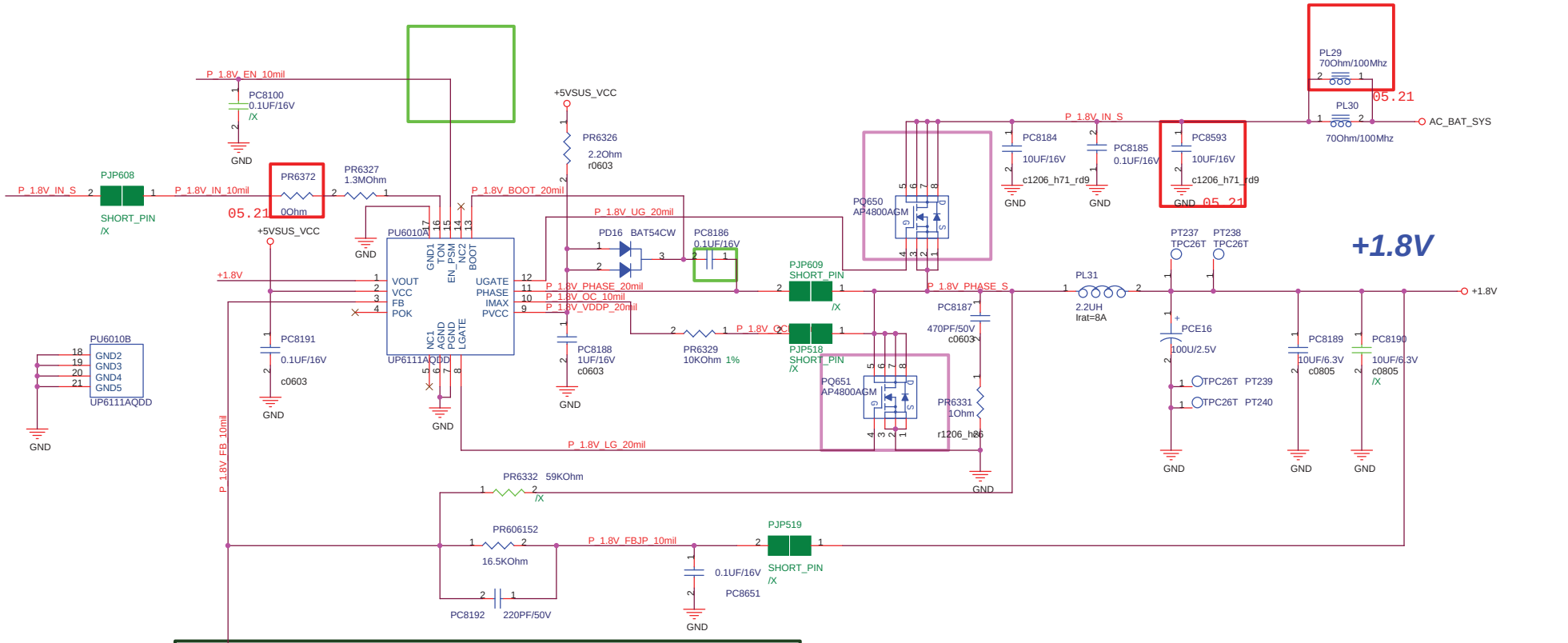
Hi : Vout = 3.3V
Low : Vout = 3.1V
OCP=7A
OCP=17A
(F=375kHZ)
(F=300kHZ)
1009
2008-10-15
2008-10-14
Add 0423
For LiFe Voltage under 6V, RT9022
BATSEL_LiFe = 1, 3.75V
BATSEL_LiFe = 0, By BATSEL_3S
(0.3A)
Default Group-A7V8X MX
ASUSTek Computer INC.
Title: Power_+5SUS&+3VSUS
Engineer: Joy Zhou
Size A2
Project Name 900SD_MB
Rev R1.0G
Date: Monday, November 10, 2008
Sheet 47 of 51





Default Group-A7V8X MX

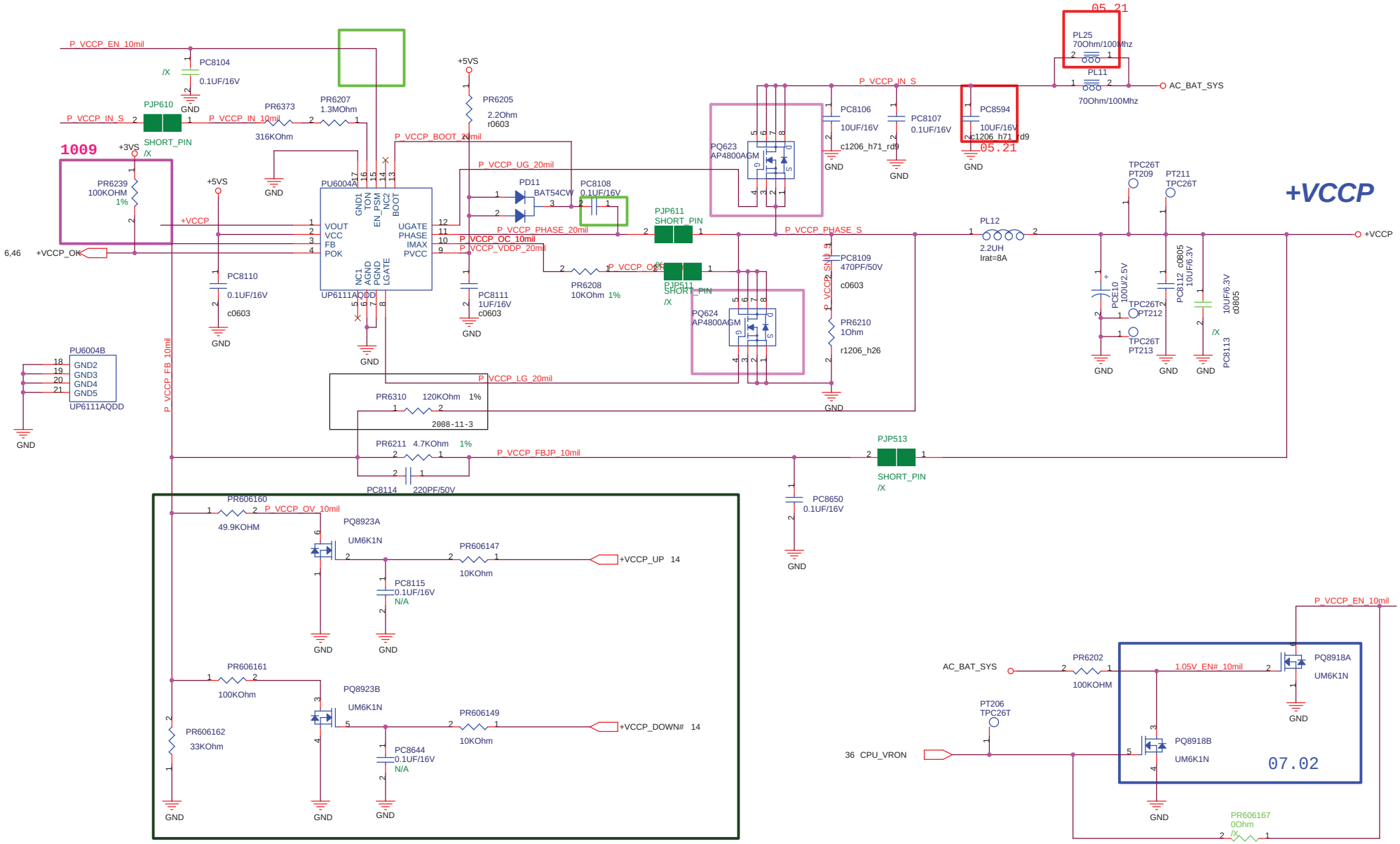
ASUSTek Computer INC.	Title : 1.8VHD_VTT_DDR	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 48 of 51	



+1.8V_UP	+1.8V_DOWN#	+1.8V
H	H	1.8V
L	H	1.7V
H	L	NO CARE
L	L	1.65V

Default Group-A7V8X MX

ASUSTek Computer INC.	Title : +1.8V	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 49 of 51	



+VCCP_UP	+VCCP_DOWN#	+VCCP
H	H	0.96V
L	H	0.89V
H	L	NO CARE
L	L	0.85V

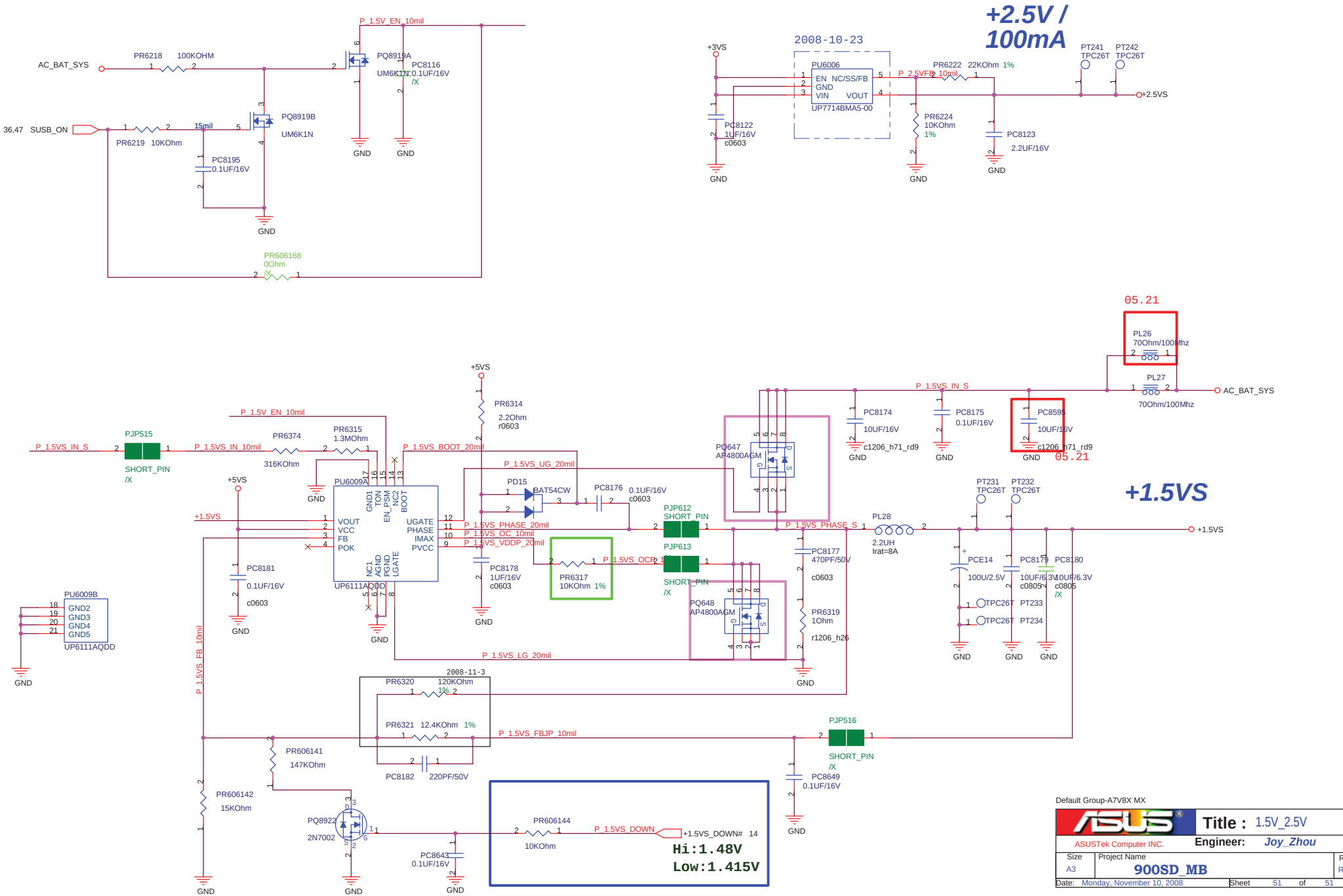
2008-11-3

0.955V
0.886V

0.852V

Default Group-A7V8X MX

ASUSTek Computer INC.	Title : VCCP	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0C
Date: Monday, November 10, 2008	Sheet 50 of 51	



Default Group-A7V8X MX

ASUSTek Computer INC.	Title : 1.5V_2.5V	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 51 of 51	

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