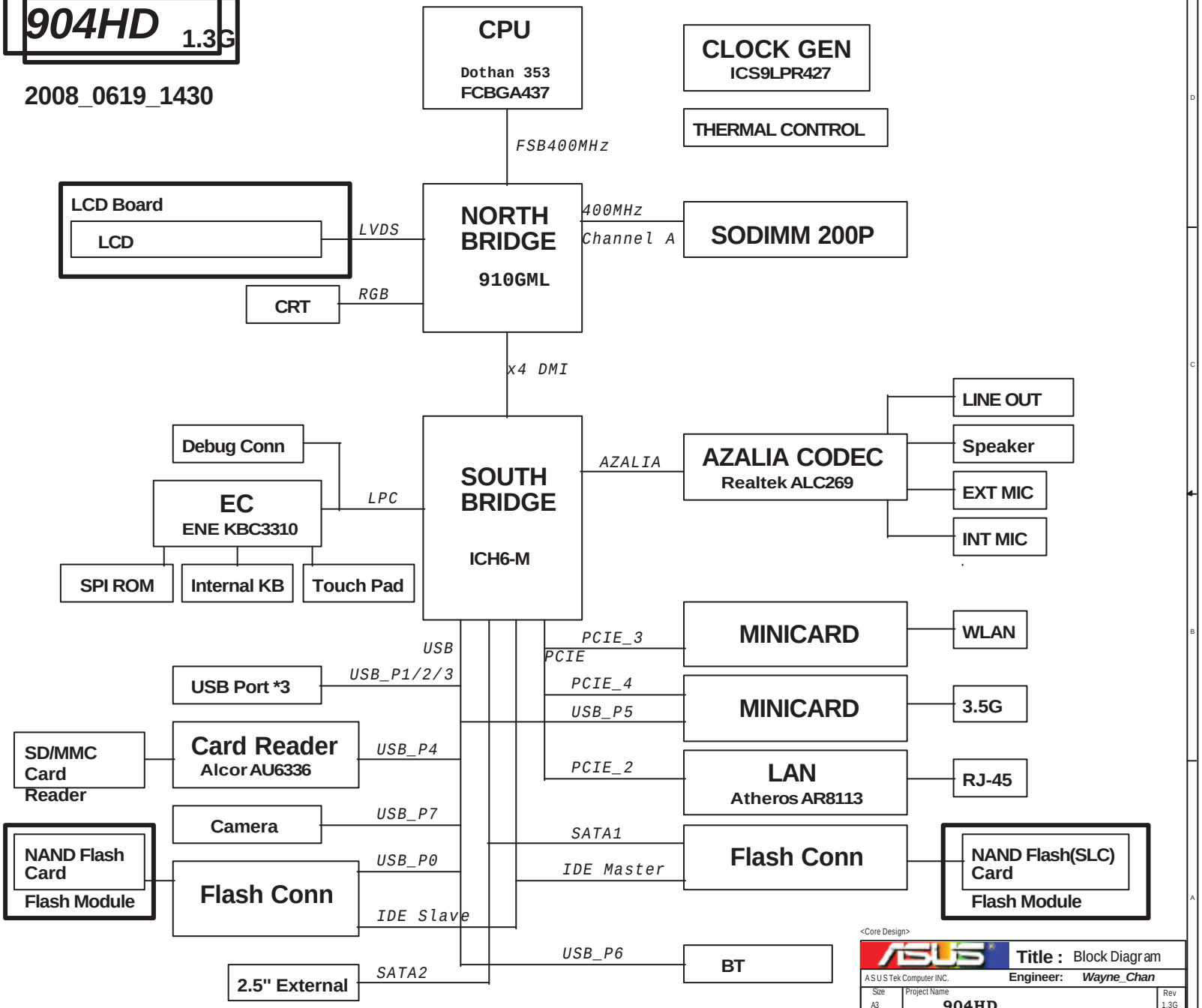
01_Block Diagram
02_System Setting
03_Power Sequence
04_EC Pin Define
05_History
06_*
07_Clock Gen_ICS9LPR427
08_Dothan_HOST
09_Dothan_PWR_GND
10_NB-910GML_HOST_DMI
11_NB-910GML_DRAM
12_NB-910GML_VGA_LVDS_TV
13_NB-910GML_PWR
14_NB-910GML_GND
15_SB-ICH6-M_Azalia_GPIO_PCI_LAN
16_SB-ICH6-M_USB_PCIE_DMI_IDE_SATA
17_SB-ICH6-M_PWR_GND
18_DDR2 SODIMM
19_DDR2_Termination
20_Onboard VGA
21_LCD Conn_LID
22_PCIEx 3.5G & Ext. Antenna
23_Mini WIFI+ BT
24_LAN_Atheros AR8113
25_MDC_RJ45
26_Flash Conn
27_SATA HDD
28_USB Port
29_Camera Power
30_Card Reader_AU6336C52
31_Codec_ALC269
32_Audio_AMP_Jack
33_EC_ENE KB3310
34_EC_UART controller
35_Switch_SPI ROM_Debug Conn
36_Thermal Sensor_FAN
37_KB_Touch Pad
38_LED
39_Discharge
40_PWR Jack
41_Srew Hole
42_EMI
43_POWER FLOW
44_Vcore
45_Power System
46_Power_+1.8V & VTTDDR
47_Power_VCCP
48_Power_+1.5VS & +2.5VS
49_Power_Charger

904HD 1.3G

2008_0619_1430



<Core Design>

ASUS Title : Block Diagram

ASUS Tek Computer INC. Engineer: Wayne_Chan

Size	Project Name	Rev
A3	904HD	1.3G

Date: Tuesday, July 01, 2008 Sheet 1 of 49

EEE PC 1000HD PCB version

GPI29	GPI31	PCB version
0	0	1.0G
0	1	
1	0	
1	1	

USB

USB 0	Flash Conn
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	BT
USB 7	Camera

PCIE

PCIE1	NC
PCIE2	LAN
PCIE3	Minicard
PCIE4	Minicard

Azalia

ACZ_SDIN0	CODEC
ACZ_SDIN1	NC
ACZ_SDIN2	NC

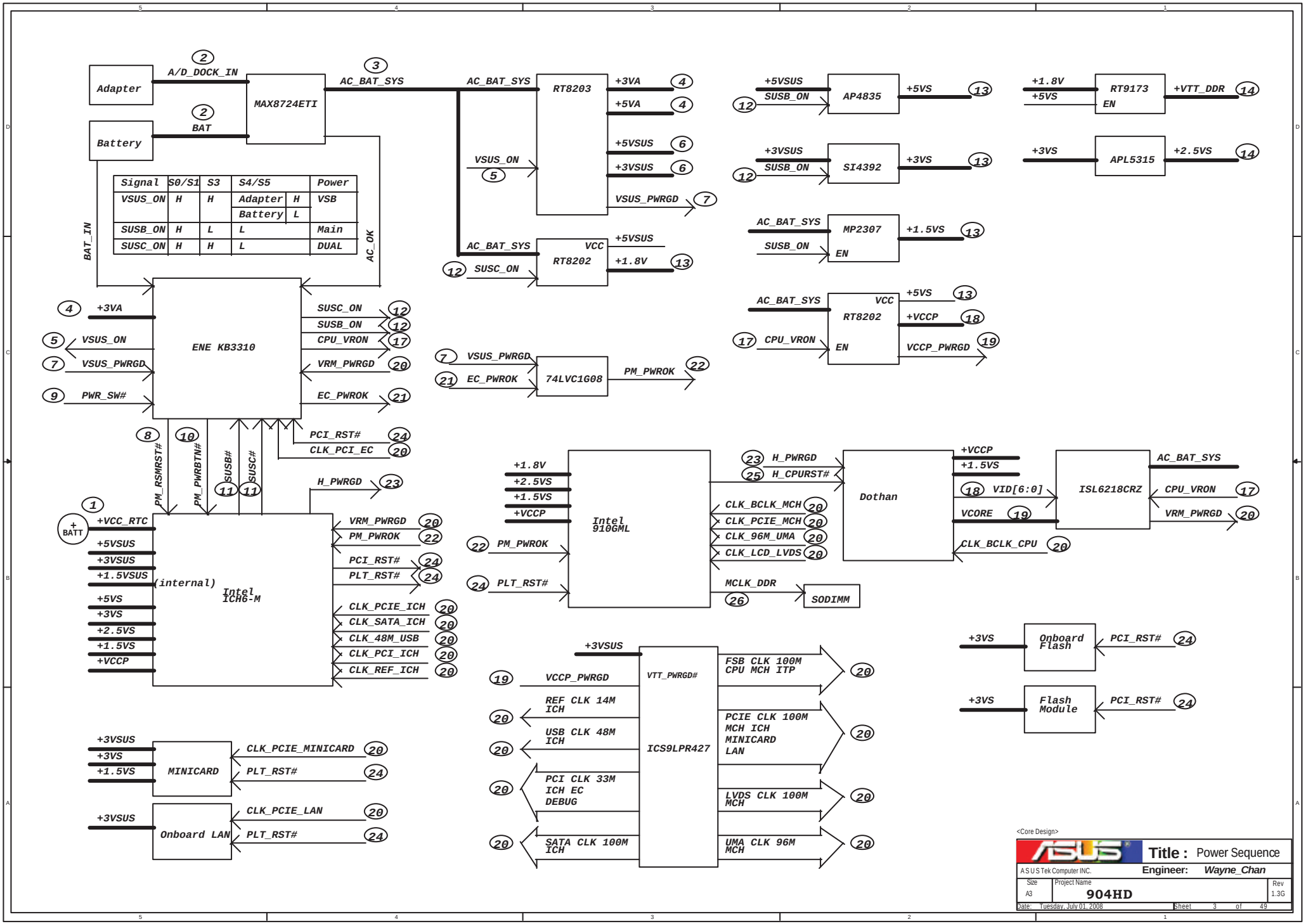
<Core Design>

Title : System Setting

A S U S Tek Computer INC. Engineer: Wayne_Chan

Size	Project Name	Rev
A3	904HD	1.3G

Date: Tuesday, July 01, 2008 Sheet 2 of 49


Adapter
A/D_DOCK_IN
MAX8724ETI
AC_BAT_SYS
Battery
BAT
BAT_IN
AC_OK
Signal | S0/S1 | S3 | S4/S5 | Power
VSUS_ON | H | H | Adapter H | VSB
Battery L
SUSB_ON | H | L | L | Main
SUSC_ON | H | H | L | DUAL
RT8203
+3VA
+5VA
+5VSUS
+3VSUS
VSUS_ON
VSUS_PWRGD
RT8202
VCC
+1.8V
SUSC_ON
+5VSUS
AP4835
+5VS
SUSB_ON
SI4392
+3VS
MP2307
EN
RT9173
+VTT_DDR
APL5315
+2.5VS
+VCCP
VCCP_PWRGD
CPU_VRON
ENE KB3310
SUSB_ON
VRM_PWRGD
PWR_SW#
EC_PWROK
PCI_RST#
CLK_PCI_EC
H_PWRGD
PM_RSMRST#
PM_PWRBTN#
SUSB#
SUSC#
74LVC1G08
PM_PWROK
EC_PWROK
+VCC_RTC
BATT
Intel
ICH6-M
(internal)
+5VSUS
+3VSUS
+1.5VSUS
+5VS
+3VS
+2.5VS
+1.5VS
+VCCP
CLK_PCIE_ICH
CLK_SATA_ICH
CLK_48M_USB
CLK_PCI_ICH
CLK_REF_ICH
Intel
910GML
+1.8V
+2.5VS
+1.5VS
+VCCP
PM_PWROK
PLT_RST#
H_PWRGD
H_CPURST#
CLK_BCLK_MCH
CLK_PCIE_MCH
CLK_96M_UMA
CLK_LCD_LVDS
MCLK_DDR
SODIMM
Dothan
+VCCP
+1.5VS
VID[6:0]
VCORE
CLK_BCLK_CPU
ISL6218CRZ
AC_BAT_SYS
CPU_VRON
VRM_PWRGD
+3VSUS
VTT_PWRGD#
ICS9LPR427
VCCP_PWRGD
REF CLK 14M
ICH
USB CLK 48M
ICH
PCI CLK 33M
ICH EC
DEBUG
SATA CLK 100M
ICH
FSB CLK 100M
CPU MCH ITP
PCIE CLK 100M
MCH ICH
MINICARD
LAN
LVDS CLK 100M
MCH
UMA CLK 96M
MCH
MINICARD
CLK_PCIE_MINICARD
PLT_RST#
Onboard LAN
CLK_PCIE_LAN
Onboard
Flash
Flash
Module
<Core Design>
ASUS
Title : Power Sequence
A S U S Tek Computer INC.
Engineer: Wayne_Chan
Size
A3
Project Name
904HD
Rev
1.3G
Date: Tuesday, July 01, 2008
Sheet 3 of 49

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	HOTKEY_SW0#	I	Internal pullhigh
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	HOTKEY_SW1#	I	Internal pullhigh
15	GPIO08	EXTSMI#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	0-LidOff, 1-LidOn. Internal Pull Up
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	HOTKEY_SW2#	I	Internal pullhigh
20	GPIO0E/SCI#	EXT_SCI#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL_4P#	I	battery charging current setting
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	power button, internel pull-up
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	CHG_LED_GREEN#	O	Green LED for charging
39	GPIO20/KSO0/ITP_TEST	KSO0	O	
40	GPIO21/KSO1/ITP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pullhigh
56	GPIO31/KSI1	KSI1	I	Internal pullhigh
57	GPIO32/KSI2	KSI2	I	Internal pullhigh
58	GPIO33/KSI3	KSI3	I	Internal pullhigh
59	GPIO34/KSI4	KSI4	I	Internal pullhigh
60	GPIO35/KSI5	KSI5	I	Internal pullhigh
61	GPIO36/KSI6	KSI6	I	Internal pullhigh
62	GPIO37/KSI7	KSI7	I	Internal pullhigh
63	GPI38/AD0	BAT_ICHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configureation
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSAVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery LowLow
73	GPIO40	AC_OK	I	AC Adaptor Plugin
74	GPIO41	EC_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	NC	I	for KB type detection
82	GPIO49/KSO17	NC	I	for KB type detection
83	GPIO4A/PSCLK1	NC	O	LCD_SCL
84	GPIO4B/PSDAT1	NC	O	LCD_SDA
85	GPIO4C/PSCLK2	NC	O	LCD_CSB
86	GPIO4D/PSDAT2	NC	O	LCD_VSYNC
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRL_LED#	O	
95	GPIO56	HOTKEY_SW3#	I	Internal pullhigh
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	EC_PWROK	O	
103	GPXOA06	PM_LEVELDOWN#	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	CPU_LEVELDOWN#	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	PM_SUSB#	I	100K pull down to GND
115	GPXID4	PM_SUSC#	I	100K pull down to GND
116	GPXID5	VRM_PWRGD	I	Pull high to +3V
117	GPXID6	VSUS_PWRGD	I	
118	GPXID7	BATSEL_LiFe	O	
121	GPIO57	INTERNET#	I	Internal pullhigh
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	Internal pullhigh

EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

<Core Design>

ASUS

Title : EC Pin Define

ASUS Tek Computer INC. Engineer: Wayne_Chan

Size	Project Name	Rev
A3	904HD	1.3G

Date: Tuesday, July 01, 2008 Sheet 4 of 49

1.0G From 1000H 2008.3.31.2030 circuit

1.Change CPU to Dothan

2.Change NB to 910GML

3.Change SB to ICH6-M

4.VCORE control change to ISL6218CRZ

1.1G

1.Change Project name to 1000D

2.Support LiFe Battery

3.Add speaker connect

1.2G

1.Change Project name to 1000HD
2.Modify page 45.
3.Add and reserved CE1 CE5 CE6 for USB port
4.Modify schematic of LED
5.Remove Capacitor of Microphone from clock and data signal
6.Add page33 Hotkey de-bounced related schematic
7.Add page23 PERST#pull down 1M ohm

1.3G

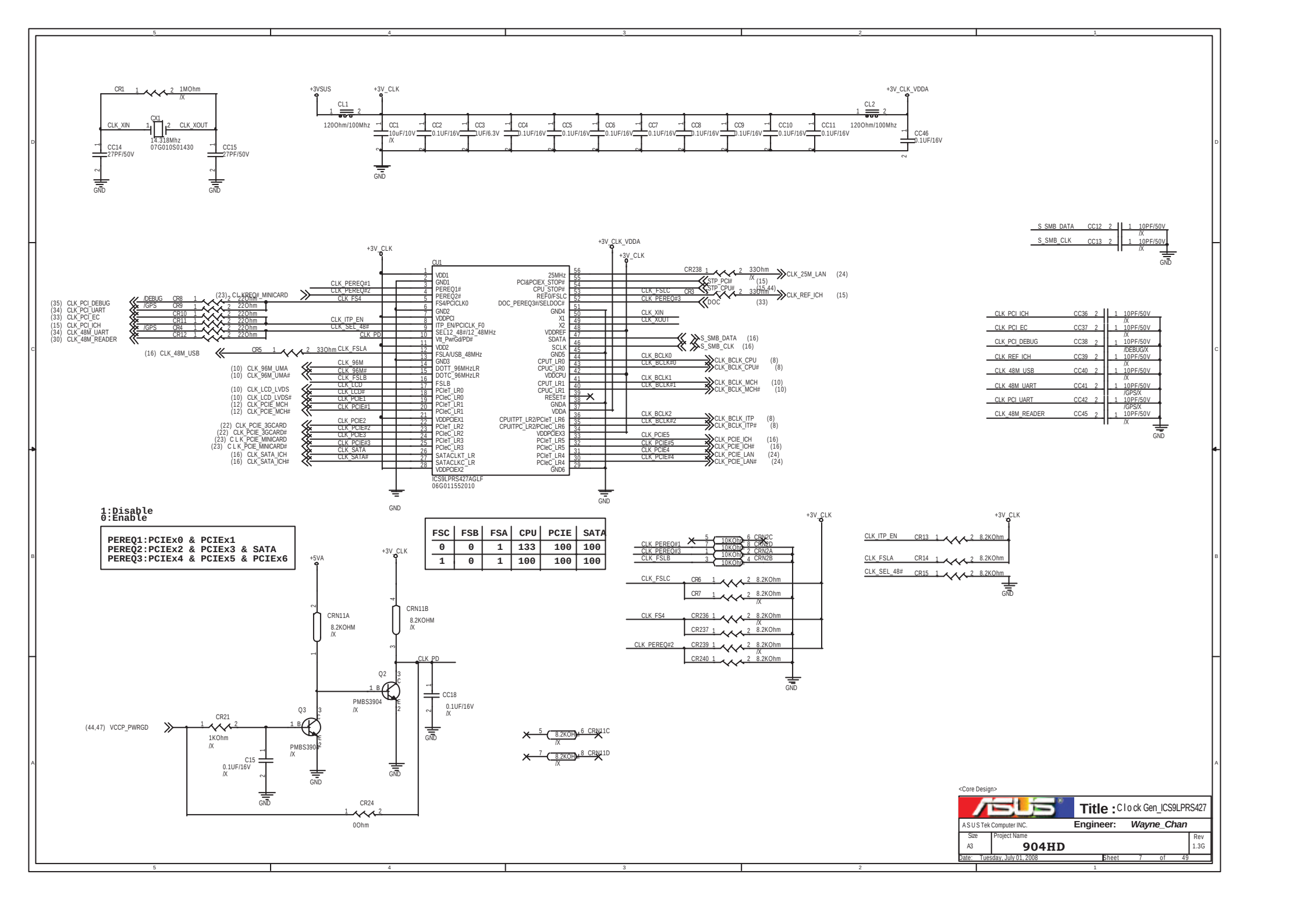
1.Change net BAT_TS pull up to +3VA_AEC
2.Change SD1.2 pull up to +3VA_AEC
3.Add and reserved R287,R288,R289,R290 for USB power
4.Add PR670,PR671
5.Add PR483,PR42, PR230, PR231,remove PJP400

<Core Design>

ASUS	Title : History	
A S U S Tek Computer INC.	Engineer: *Wayne_Chan*	
Size: A3	Project Name: 904HD	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 5 of 49	

<Core Design>

ASUS	Title : Blank	
A S U S Tek Computer INC.	Engineer: *Wayne_Chan*	
Size: A3	Project Name: 904HD	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 6 of 49	



<Core Design>

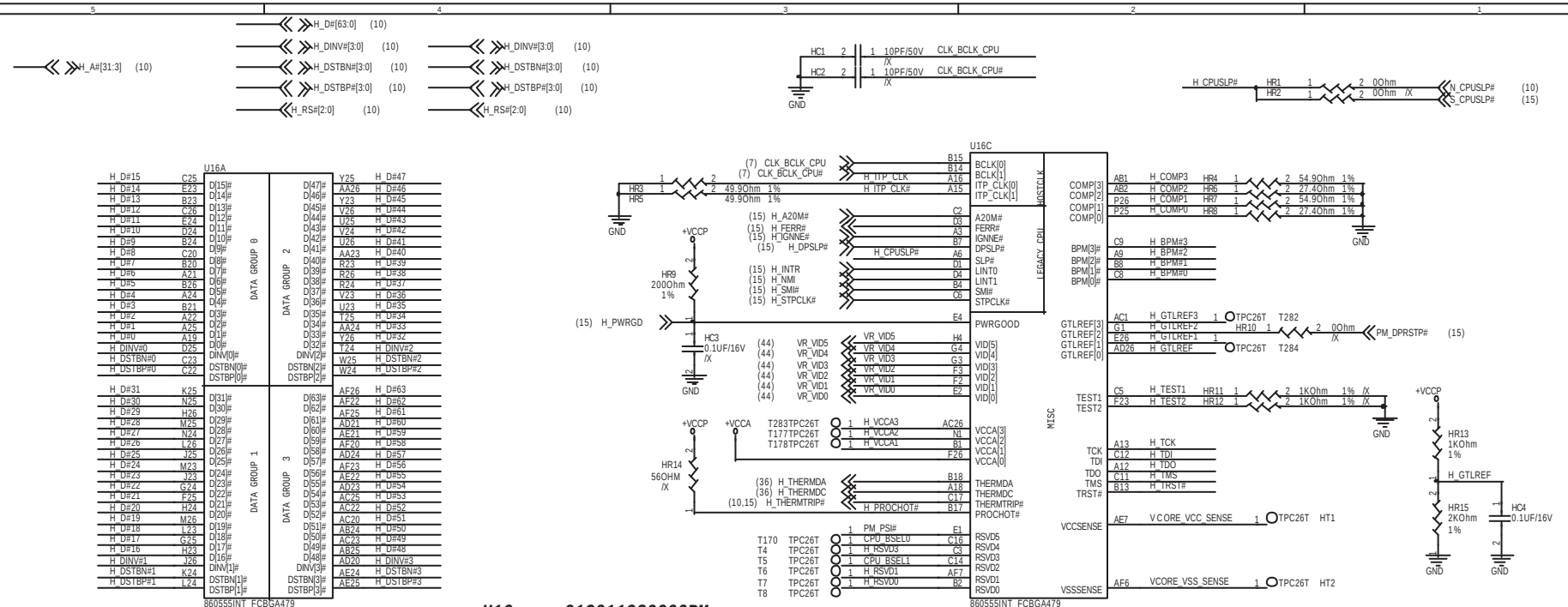
ASUS Tek Computer INC.

Title : Clock Gen_ICS9LPRS427

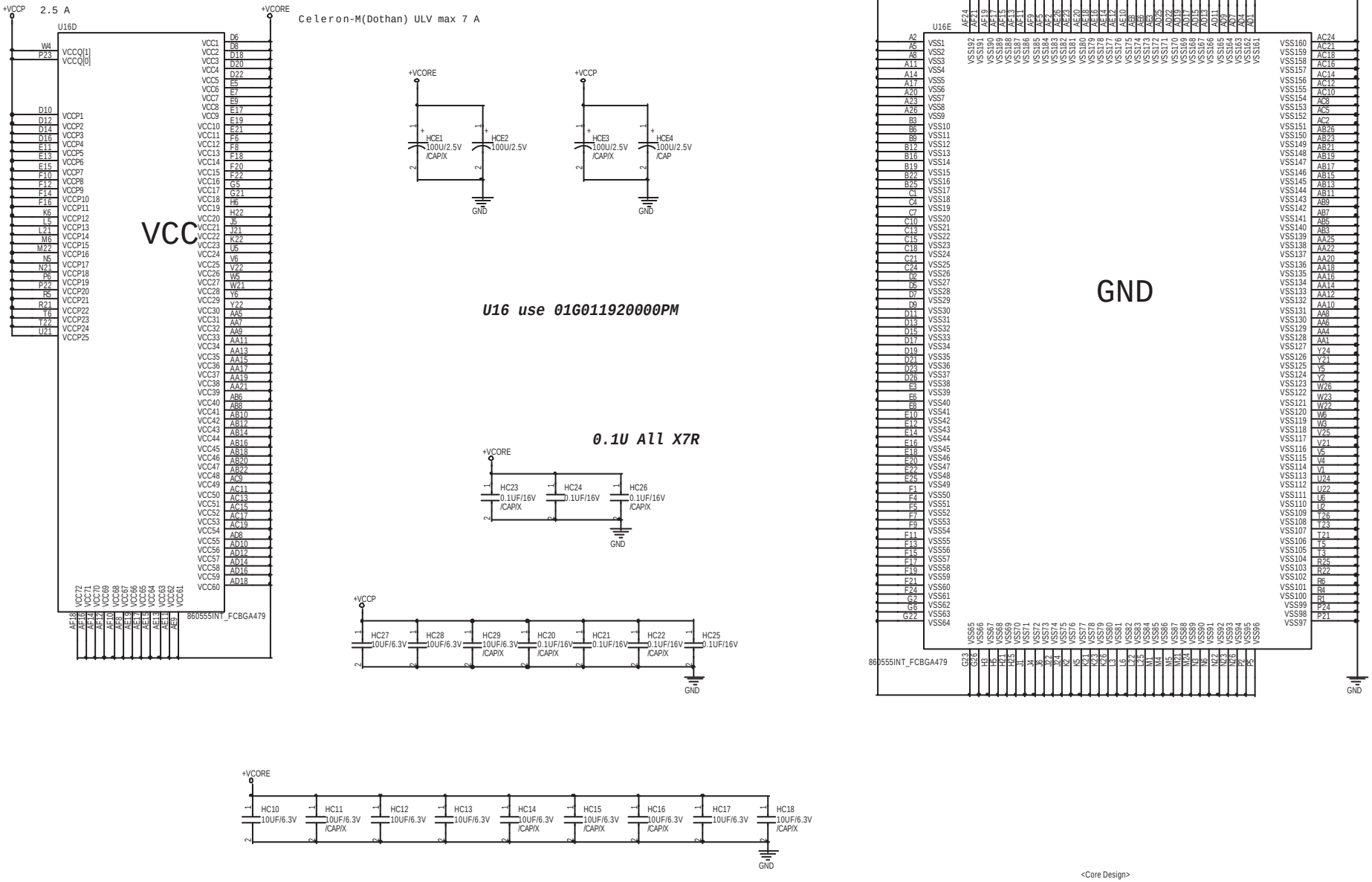
Engineer: Wayne_Chan

Size	Project Name	Rev
A3	904HD	1.3G

Date: Tuesday, July 01, 2008 Sheet 7 of 49



U16 use 01G011920000PM



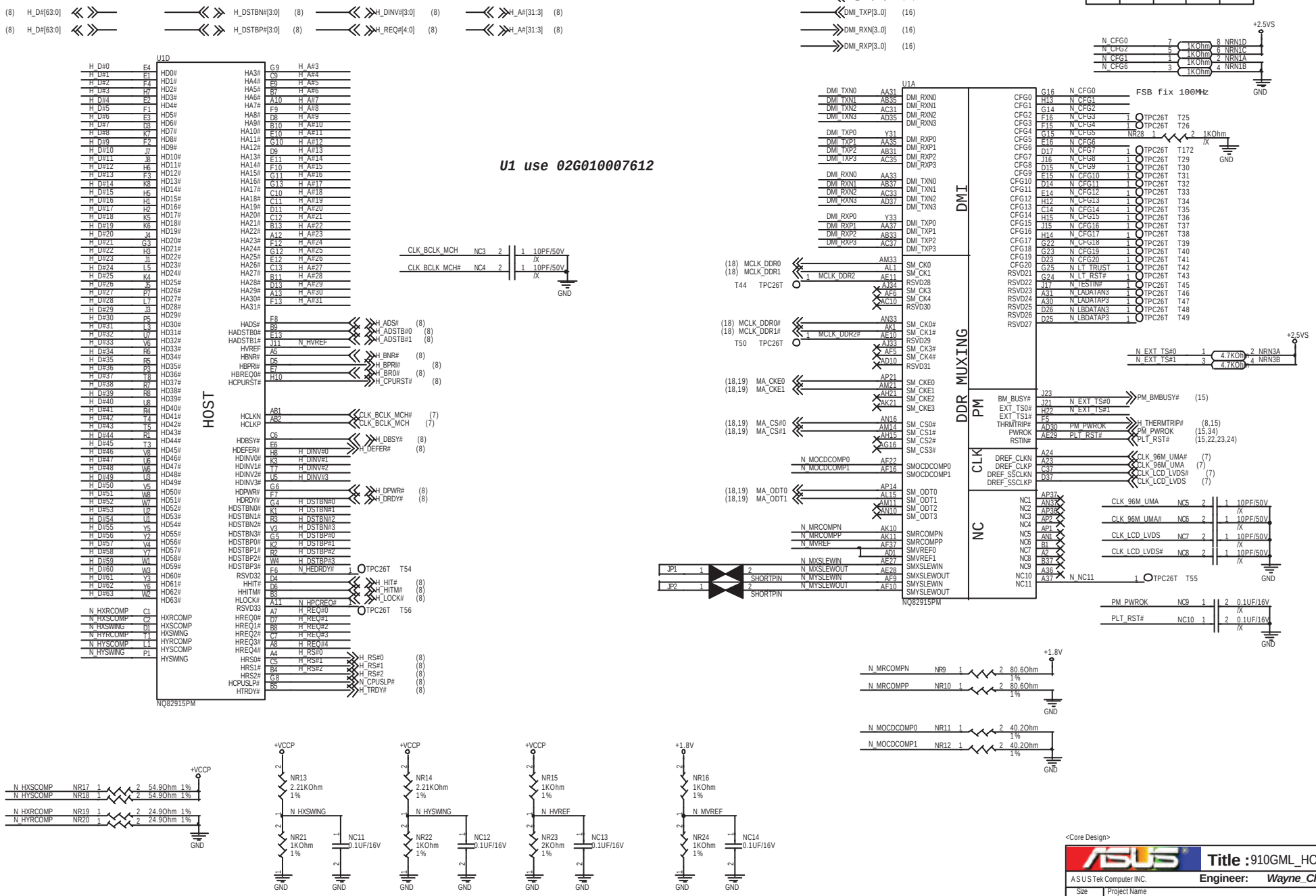
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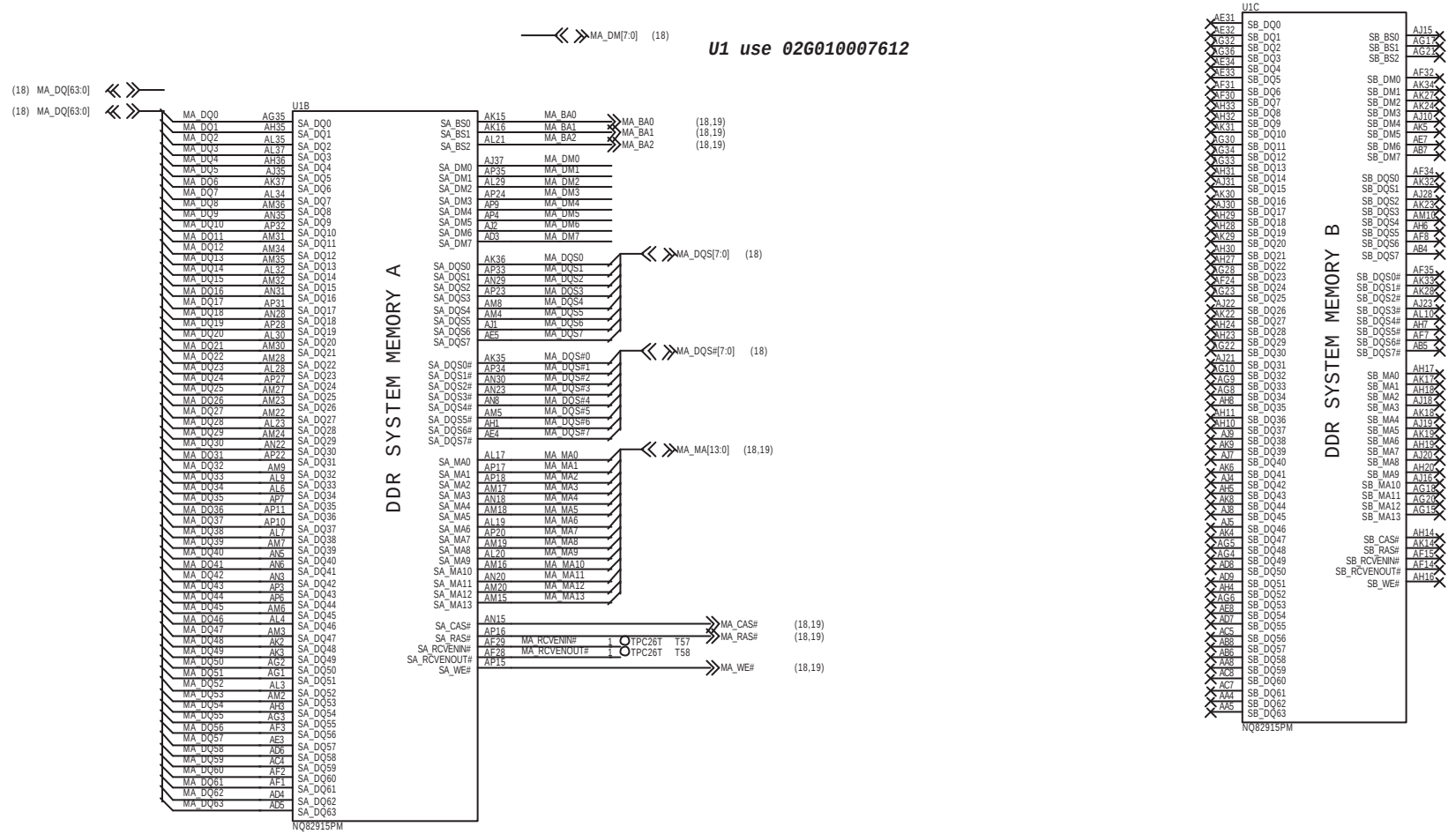
ASUS Tek Computer INC.	Title : Dothan_PWR_GND	
	Engineer: *Wayne_Chan*	
Size: A3	Project Name: **904HD**	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 9 of 49	

BCLK	FSB	BSEL2	BSEL1	BSEL0
100	400	H	L	H

U1 use 02G010007612

FSB fix 100MHz





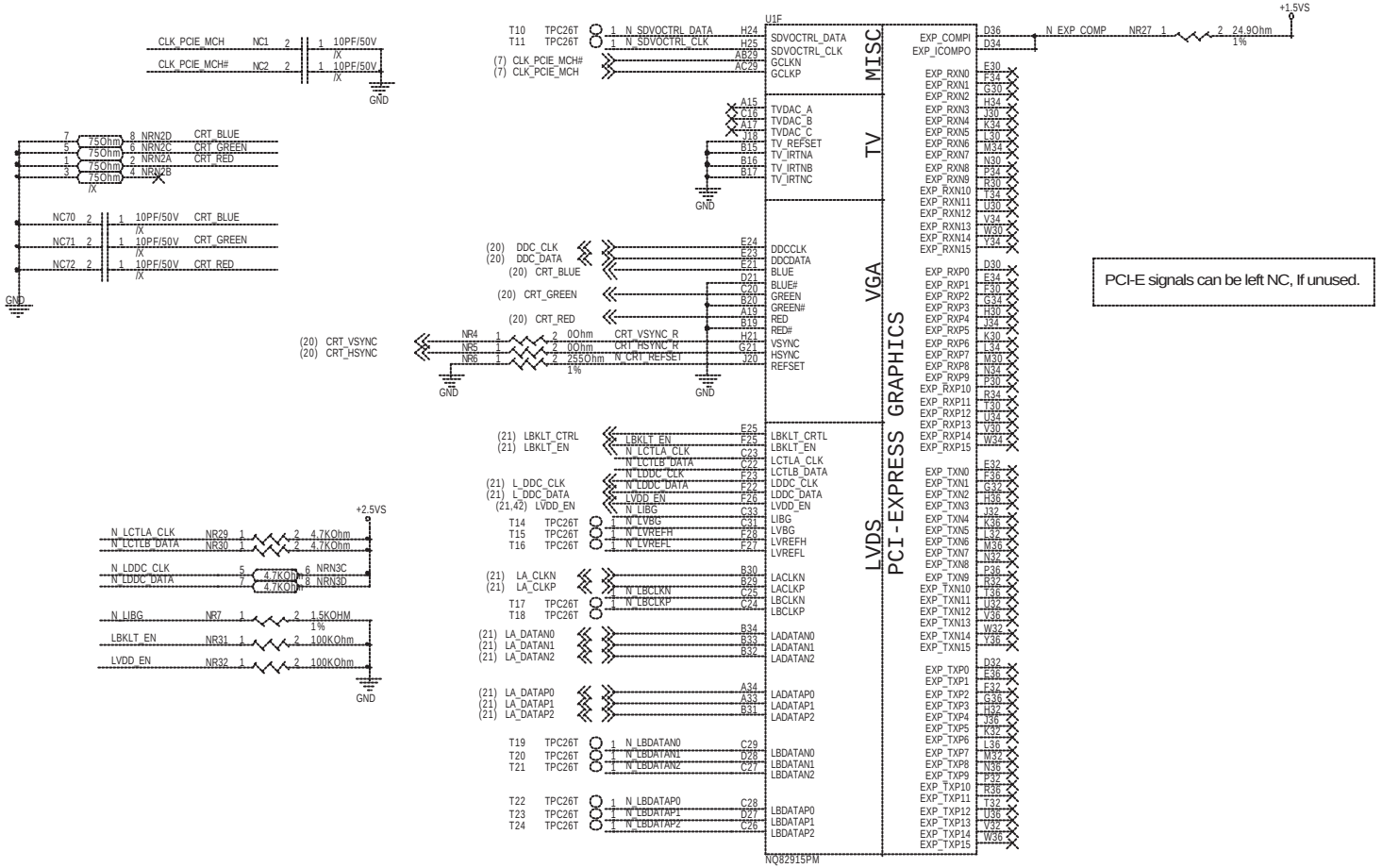
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ASUS	Title : 910GML_DRAM	
A S U S Tek Computer INC.	Engineer: *Wayne_Chan*	
Size: A3	Project Name: **904HD**	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 11 of 49	

SDVO SMbus have internal pull down

SDVOCRTL_DATA Int PD
0 : No SDVO device
1 : SDVO device present

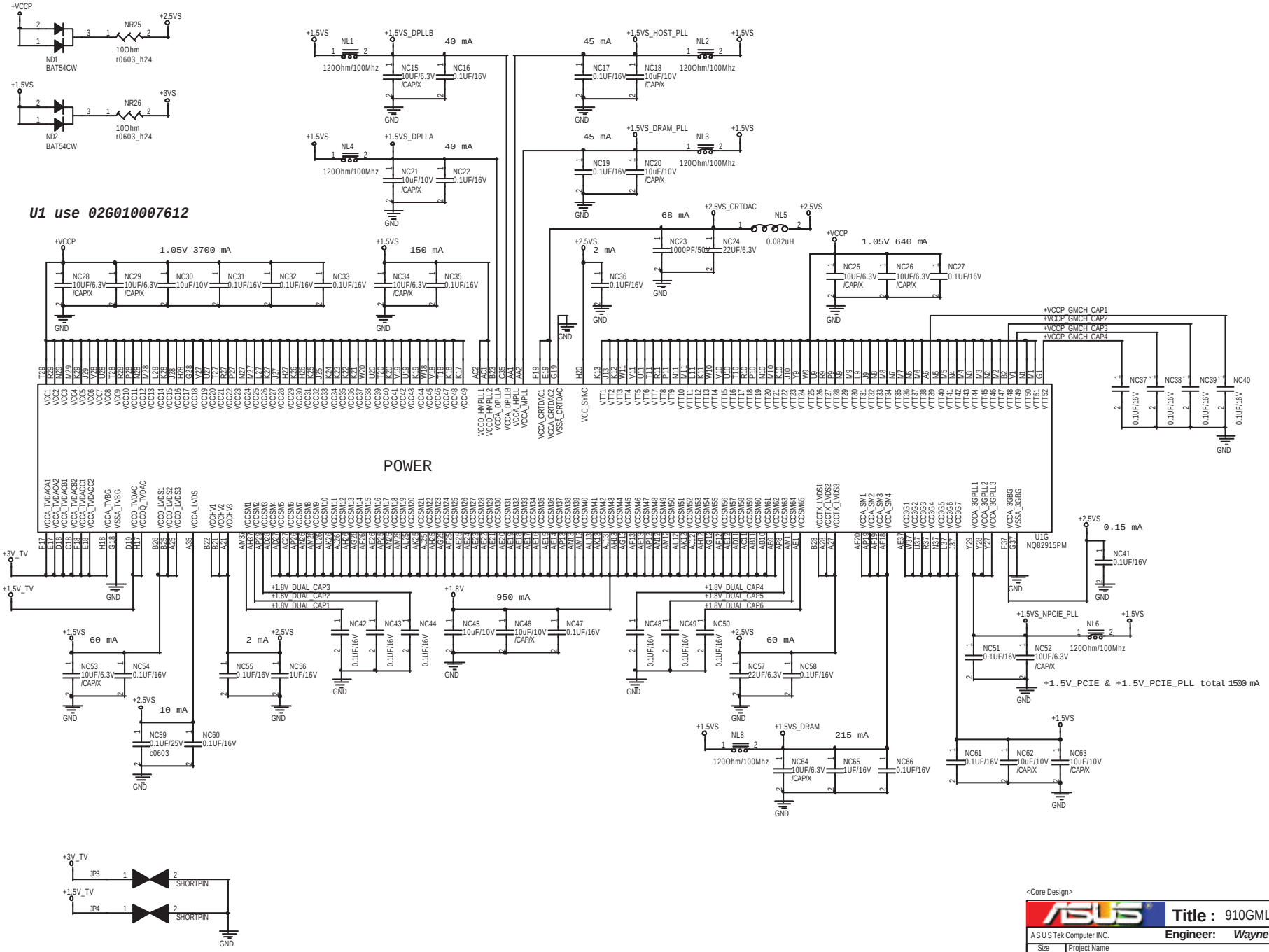
U1 use 02G010007612



PCI-E signals can be left NC, If unused.

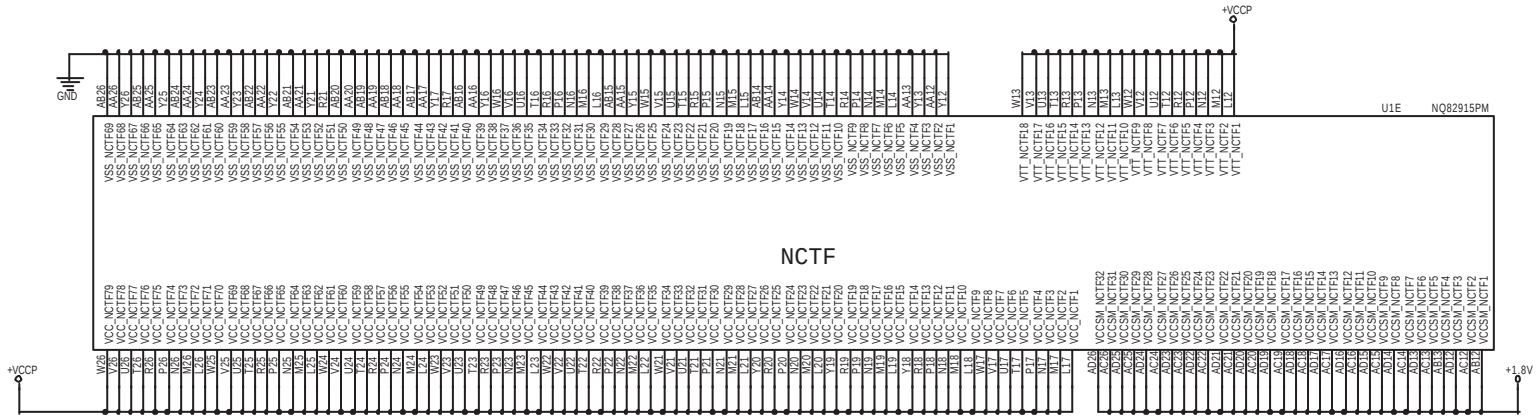
<Core Design>

ASUS Tek Computer INC.	Title : 910GML_VGA_LVDS	
	Engineer: *Wayne_Chan*	
Size: A3	Project Name: **904HD**	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 12 of 49	

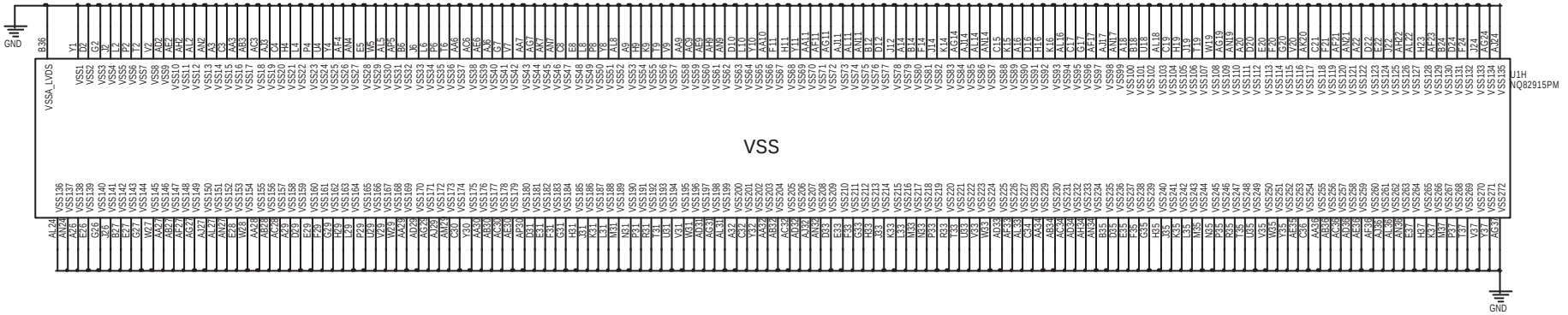


<Core Design>

ASUS	Title : 910GML_PWR	
A S U S Tek Computer INC.	Engineer: *Wayne_Chan*	
Size: A3	Project Name: **904HD**	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 13 of 49	

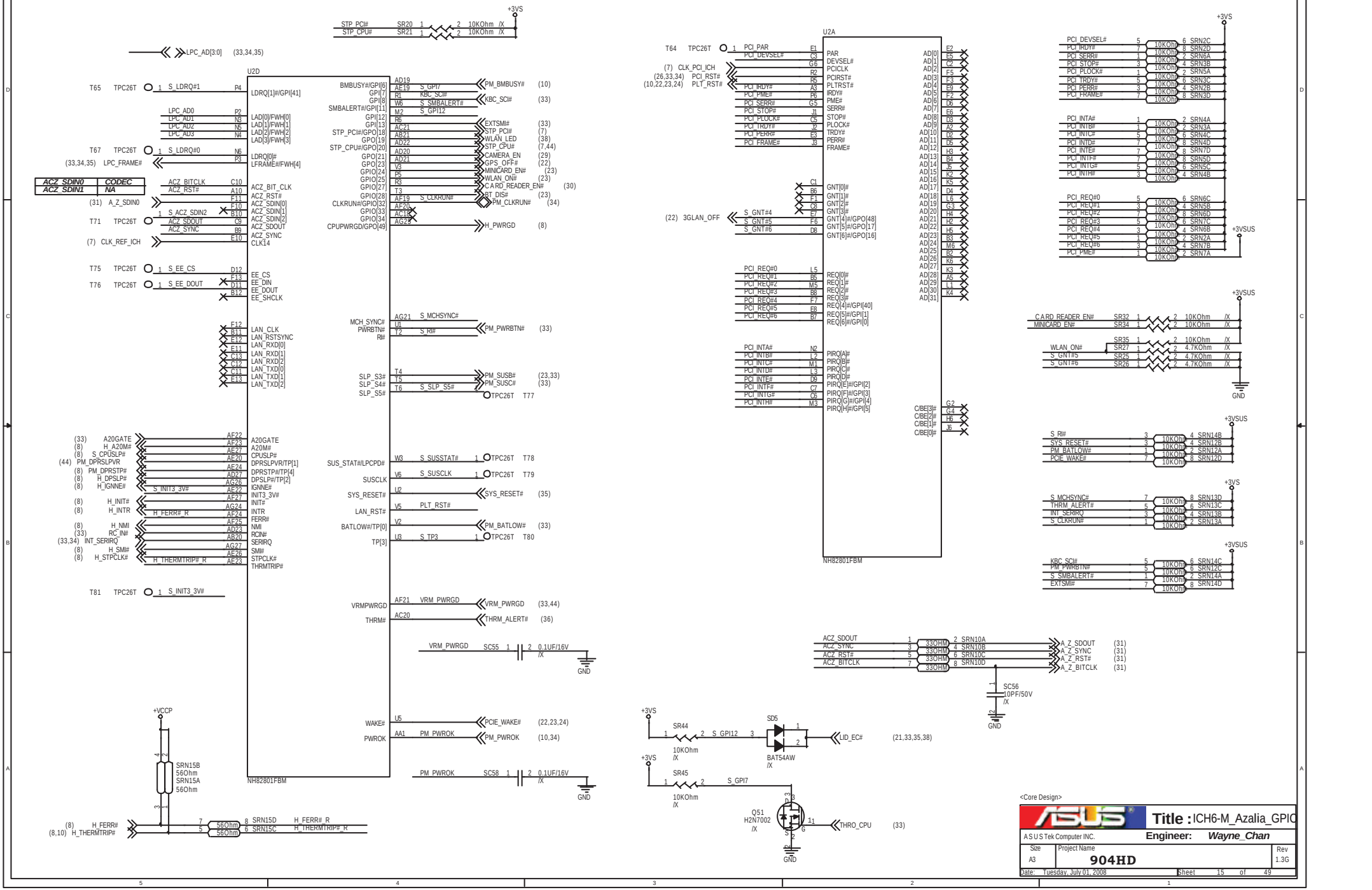


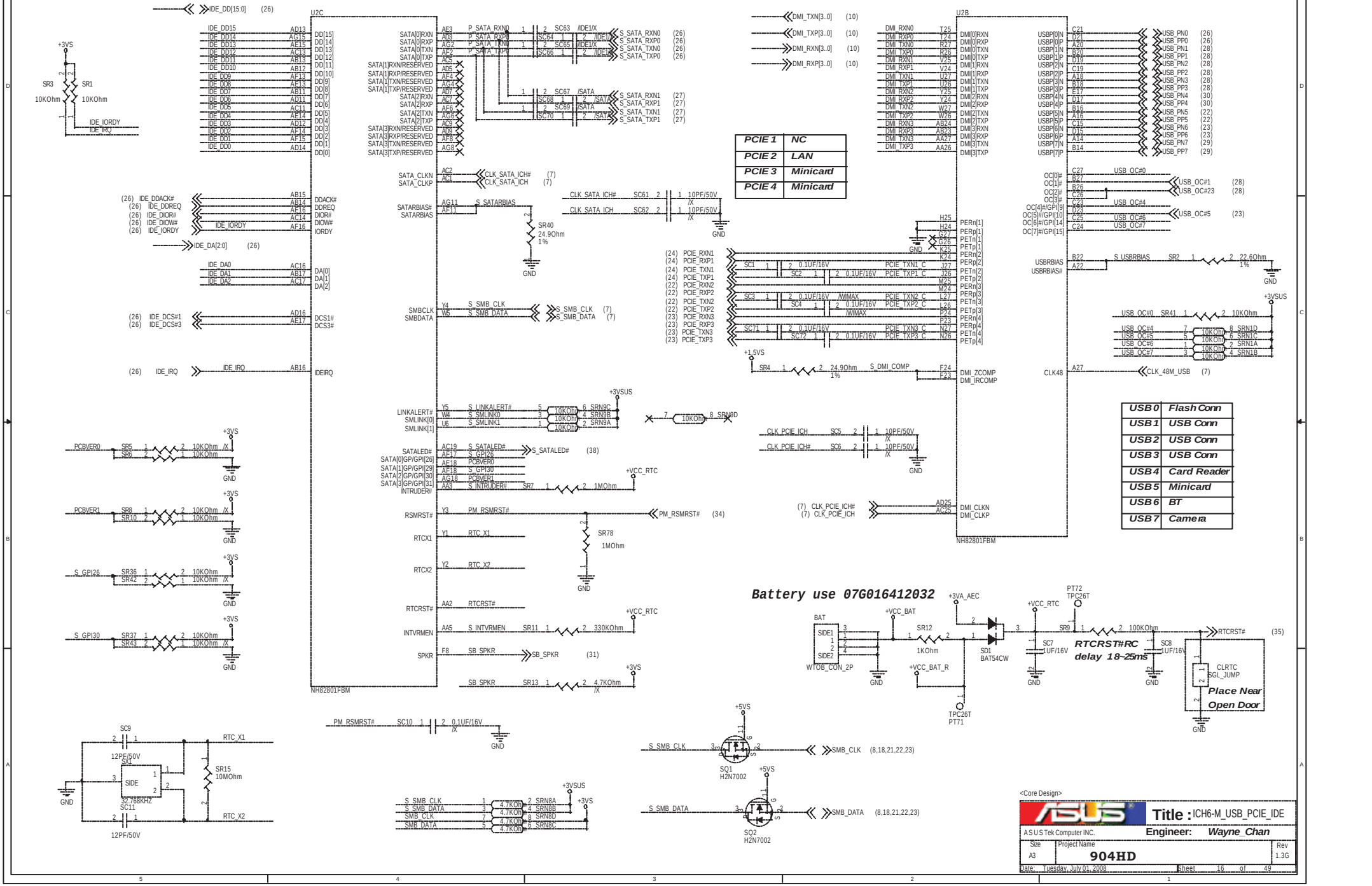
U1 use 02G010007612

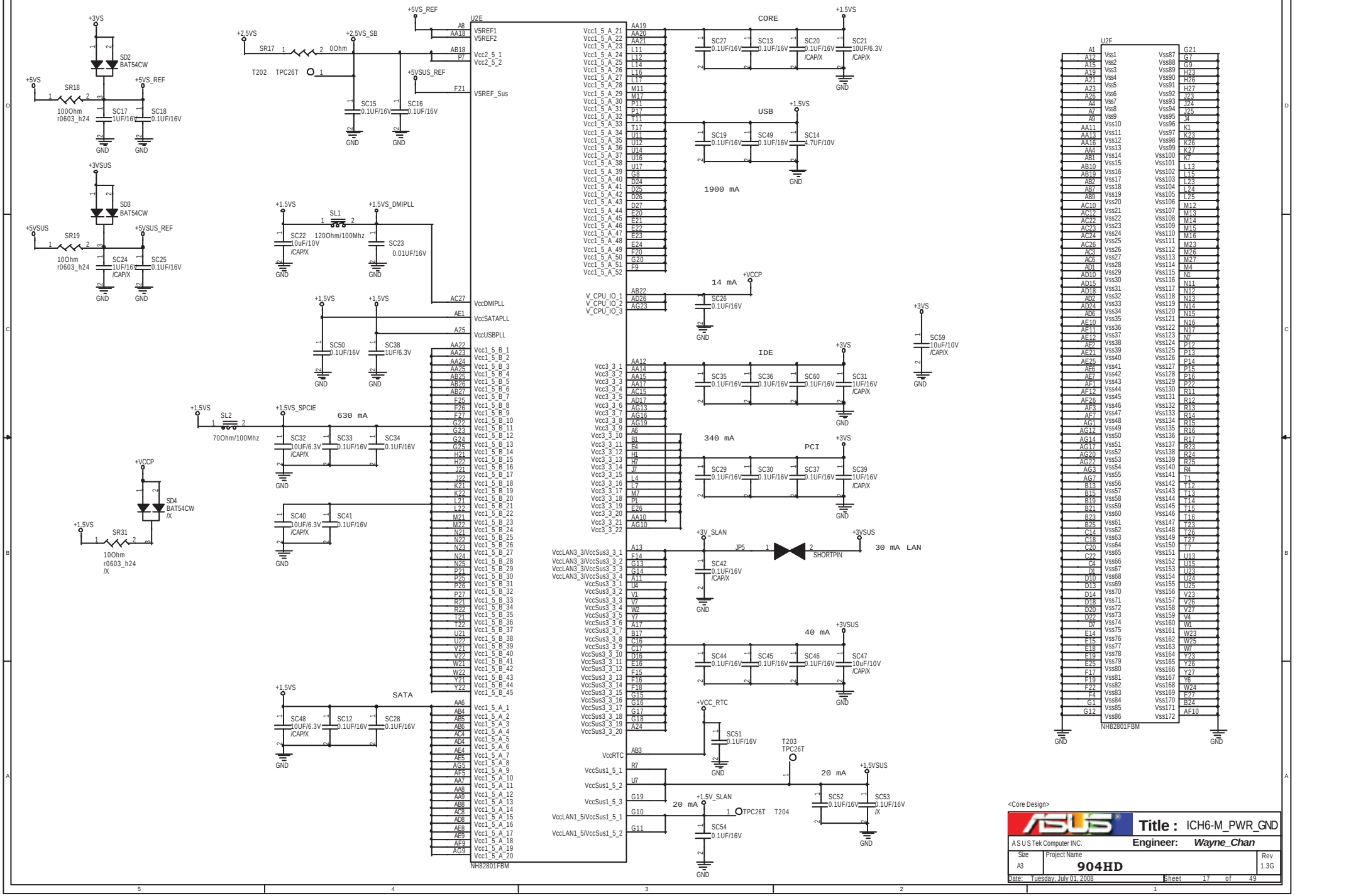


<Core Design>

ASUS Tek Computer INC.	Title : 910GML_GND	
	Engineer: *Wayne_Chan*	
Size: A3	Project Name: **904HD**	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 14 of 49	

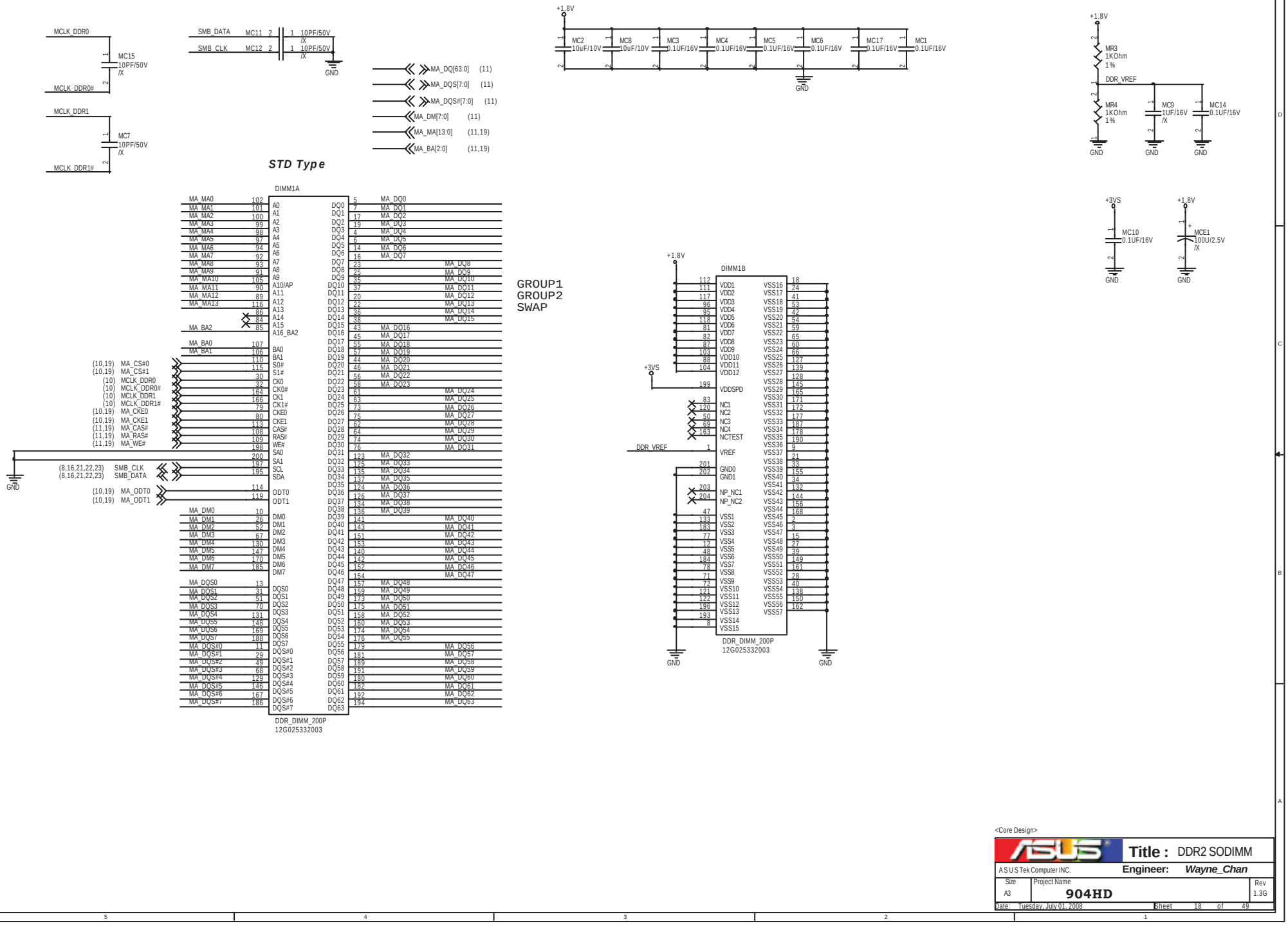

U2D
NH82801FBM
U2A
NH82801FBM
+3VS
+3VSUS
+VCCP
GND
LPC_AD[3:0] (33,34,35)
LPC_FRAME# (33,34,35)
A_Z_SDIN0 (31)
CLK_REF_ICH (7)
CLK_PCI_ICH (7)
PCI_RST# (26,33,34)
PLT_RST# (10,22,23,24)
3GLAN_OFF (22)
H_FERR# (8)
H_THERMTRIP# (8,10)
INT_SERIRQ (33,34)
ACZ_SDIN0 CODEC
ACZ_SDIN1 NA
SRN15B 56Ohm
SRN15A 56Ohm
SC55 0.1UF/16V /X
SC58 0.1UF/16V /X
SC56 10PF/50V /X
SR44 10KOhm /X
SR45 10KOhm /X
SD5 BAT54AW /X
Q51 H2N7002 /X
LID_EC# (21,33,35,38)
THRO_CPU (33)
<Core Design>
ASUS Tek Computer INC.
Title : ICH6-M_Azalia_GPIO
Engineer: Wayne_Chan
Size A3
Project Name 904HD
Rev 1.3G
Date: Tuesday, July 01, 2008
Sheet 15 of 49


U2C
NH82801FBM
U2B
NH82801FBM
PCIE 1 NC
PCIE 2 LAN
PCIE 3 Minicard
PCIE 4 Minicard
USB0 Flash Conn
USB1 USB Conn
USB2 USB Conn
USB3 USB Conn
USB4 Card Reader
USB5 Minicard
USB6 BT
USB7 Camera
Battery use 07G016412032
RTCRST#RC delay 18~25ms
Place Near Open Door
Title : ICH6-M_USB_PCIE_IDE
ASUS Tek Computer INC.
Engineer: Wayne_Chan
Project Name 904HD
Rev 1.3G
Date: Tuesday, July 01, 2008
Sheet 16 of 49



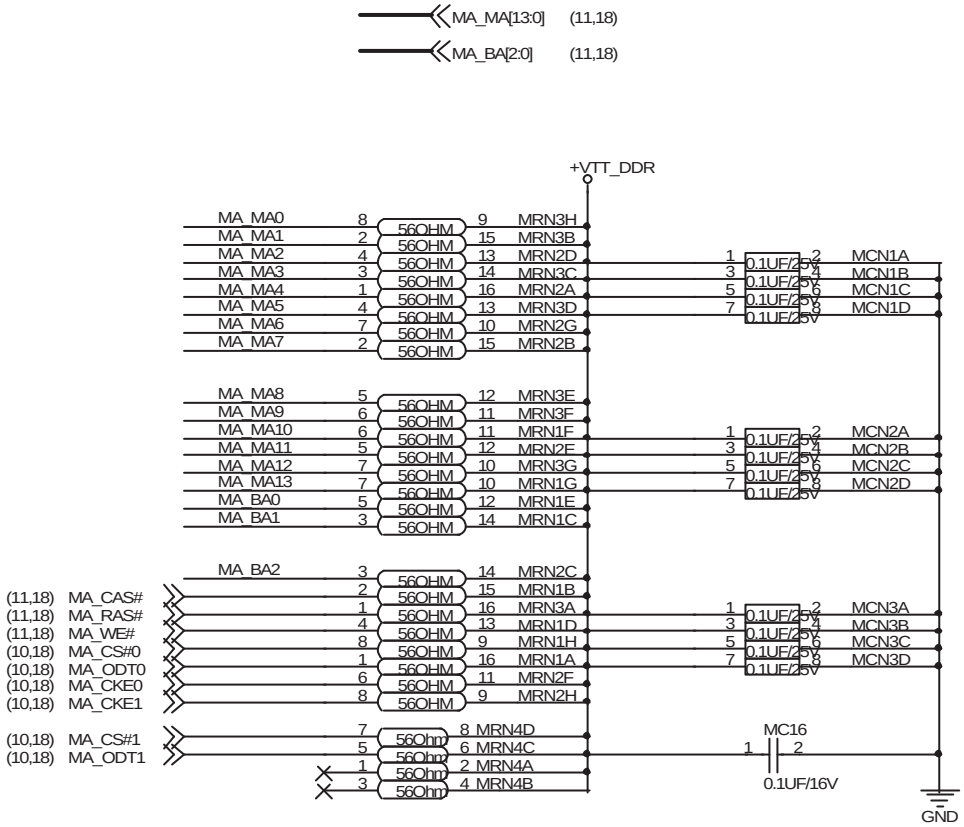
<Core Design>

ASUS Tek Computer INC.	Title :	ICH6-M_PWR_GND	
	Engineer:	*Wayne_Chan*	
Size: A3	Project Name: **904HD**		Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 17 of 49		



<Core Design>

ASUS	Title : DDR2 SODIMM	
A S U S Tek Computer INC.	Engineer: *Wayne_Chan*	
Size: A3	Project Name: **904HD**	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 18 of 49	



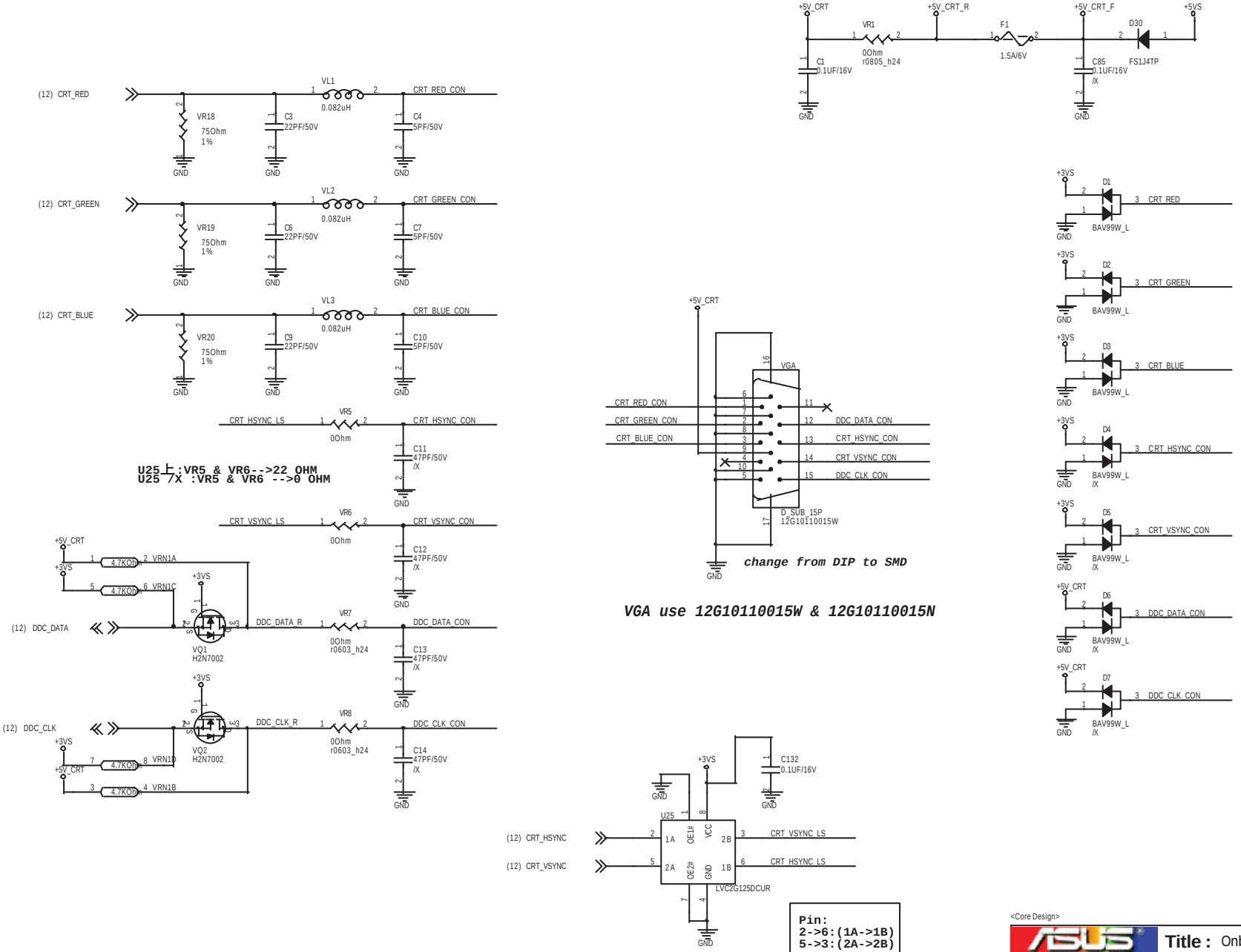
<Core Design>

Title : DDR2_Termination

ASUSTek Computer INC. **Engineer:** *Wayne_Chan*

Size	Project Name	Rev
A4	**904HD**	1.3G

Date: Tuesday, July 01, 2008 Sheet 19 of 49



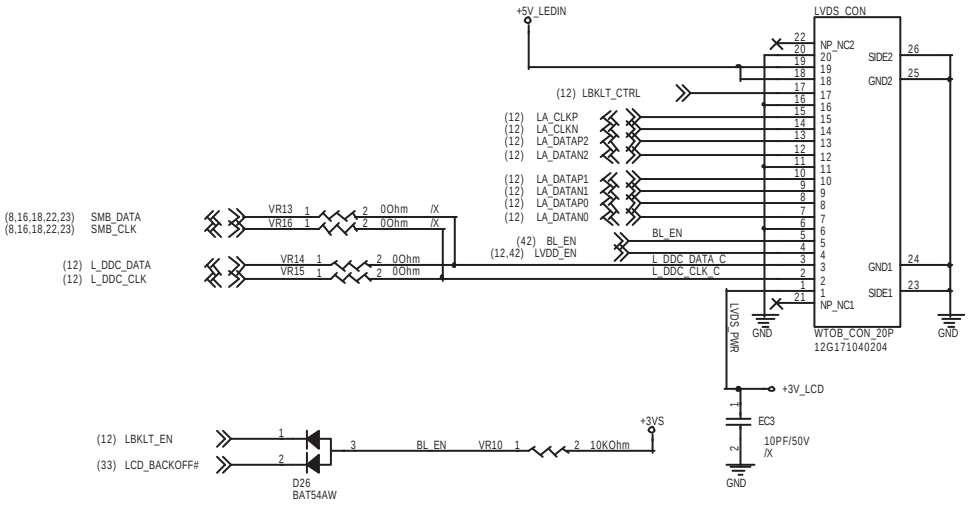
change from DIP to SMD

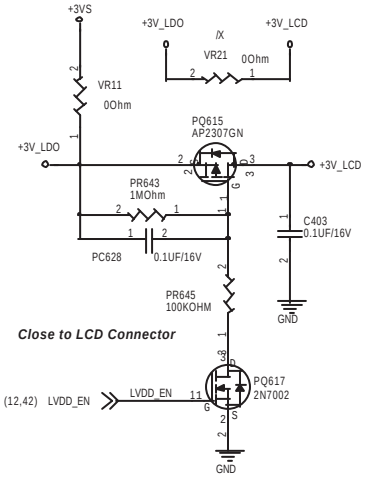
VGA use 12G10110015W & 12G10110015N

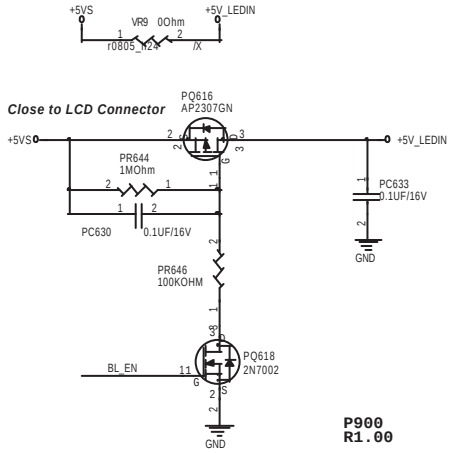
Pin:
2->6:(1A->1B)
5->3:(2A->2B)

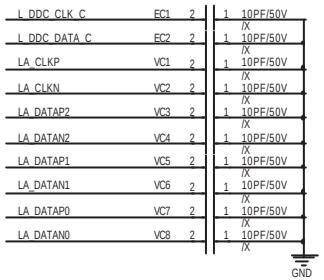
<Core Design>

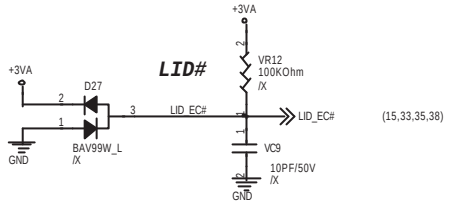
ASUS Tek Computer INC.	Title : Onboard VGA	
	Engineer: Wayne_Chan	
Size: A3	Project Name: 904HD	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 20 of 49	

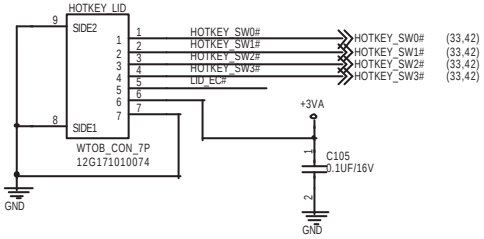

+5V_LEDIN
LVDS_CON
(12) LBKLT_CTRL
(12) LA_CLKP
(12) LA_CLKN
(12) LA_DATAP2
(12) LA_DATAN2
(12) LA_DATAP1
(12) LA_DATAN1
(12) LA_DATAP0
(12) LA_DATAN0
(42) BL_EN
(12,42) LVDD_EN
BL_EN
L_DDC_DATA_C
L_DDC_CLK_C
NP_NC2
SIDE2
GND2
GND1
SIDE1
NP_NC1
WTOB_CON_20P
12G171040204
LVDS PWR
+3V_LCD
EC3
10PF/50V
/X
GND
(8,16,18,22,23) SMB_DATA
(8,16,18,22,23) SMB_CLK
VR13
VR16
0Ohm
/X
(12) L_DDC_DATA
(12) L_DDC_CLK
VR14
VR15
(12) LBKLT_EN
(33) LCD_BACKOFF#
D26
BAT54AW
BL_EN
VR10
10KOhm
+3VS

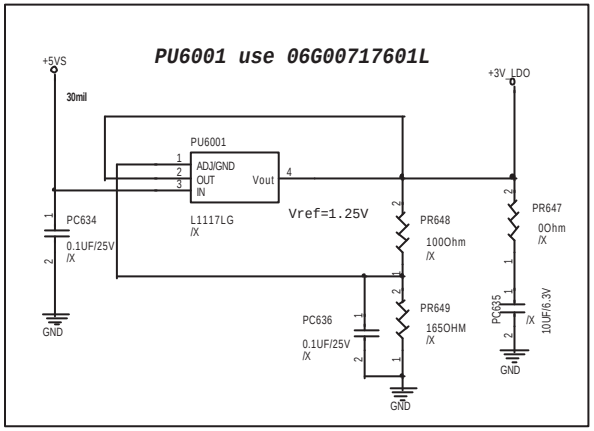

+3VS
+3V_LDO
/X
+3V_LCD
VR21
0Ohm
VR11
0Ohm
PQ615
AP2307GN
PR643
1MOhm
PC628
0.1UF/16V
C403
0.1UF/16V
PR645
100KOHM
Close to LCD Connector
(12,42) LVDD_EN
LVDD_EN
PQ617
2N7002
GND


+5VS
+5V_LEDIN
VR9
0Ohm
/X
Close to LCD Connector
PQ616
AP2307GN
PR644
1MOhm
PC630
0.1UF/16V
PC633
0.1UF/16V
PR646
100KOHM
BL_EN
PQ618
2N7002
GND
P900
R1.00

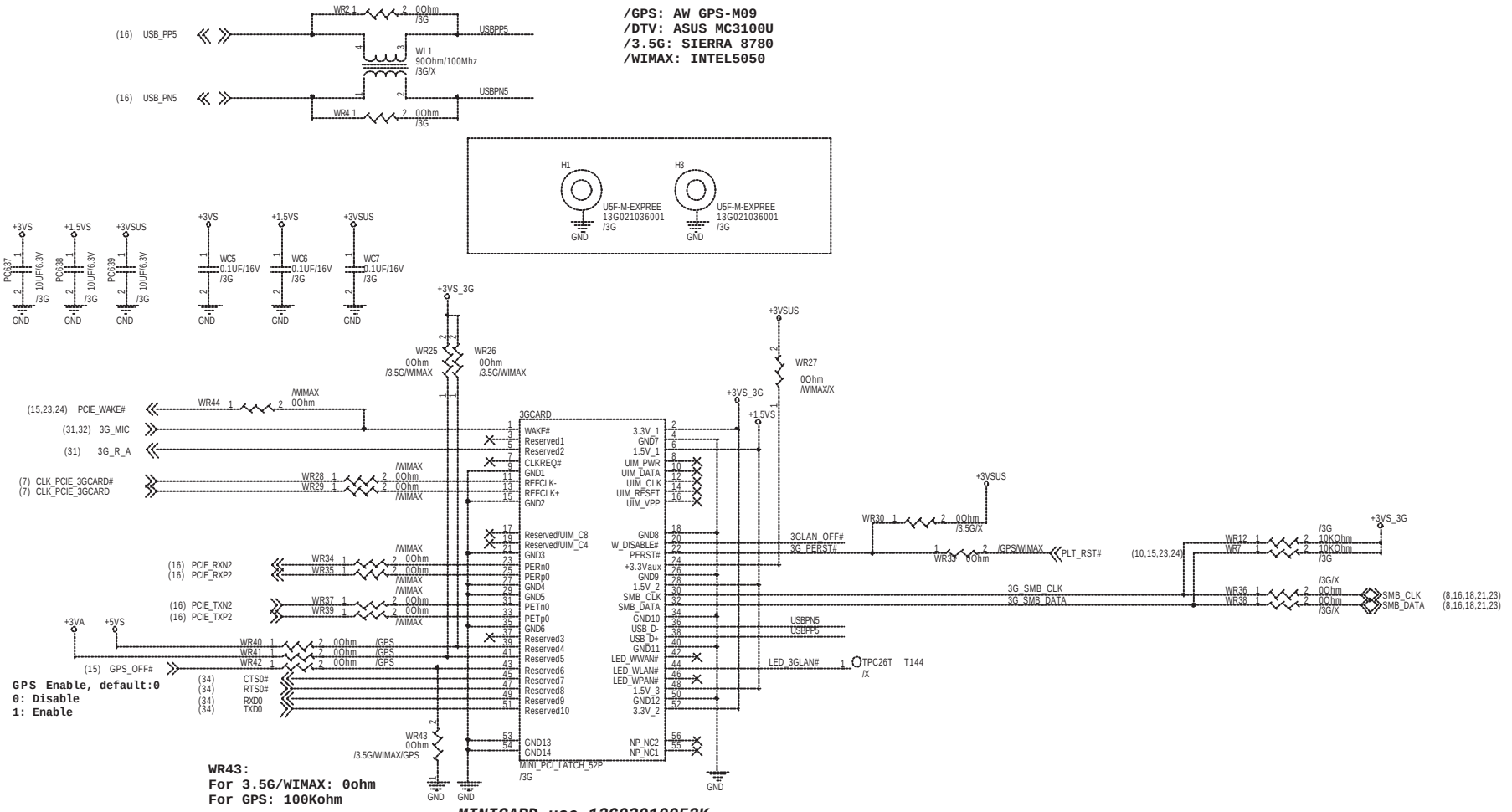

L_DDC_CLK_C
L_DDC_DATA_C
LA_CLKP
LA_CLKN
LA_DATAP2
LA_DATAN2
LA_DATAP1
LA_DATAN1
LA_DATAP0
LA_DATAN0
EC1
EC2
VC1
VC2
VC3
VC4
VC5
VC6
VC7
VC8
10PF/50V
/X
GND


+3VA
LID#
D27
BAV99W_L
/X
LID_EC#
VR12
100KOHM
/X
VC9
10PF/50V
/X
GND
(15,33,35,38)


HOTKEY_LID
SIDE2
SIDE1
WTOB_CON_7P
12G171010074
HOTKEY_SW0#
HOTKEY_SW1#
HOTKEY_SW2#
HOTKEY_SW3#
LID_EC#
(33,42)
+3VA
C105
0.1UF/16V
GND


PU6001 use 06G00717601L
+5VS
30mil
+3V_LDO
PU6001
ADJ/GND
OUT
Vout
IN
L1117LG
/X
Vref=1.25V
PC634
0.1UF/25V
/X
PR648
100Ohm
/X
PR647
0Ohm
/X
PC635
10UF/6.3V
/X
PC636
0.1UF/25V
/X
PR649
165OHM
/X
GND

/GPS: AW GPS-M09
/DTV: ASUS MC3100U
/3.5G: SIERRA 8780
/WIMAX: INTEL5050

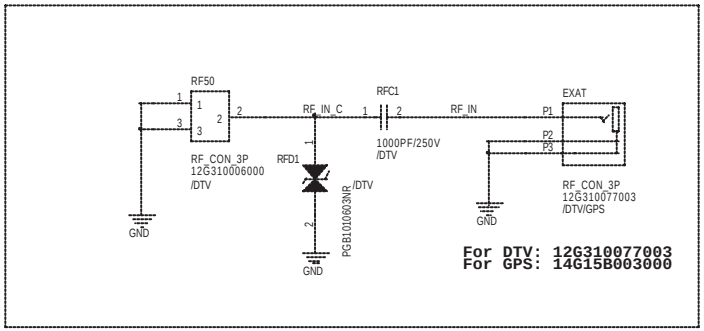


GPS Enable, default:0
0: Disable
1: Enable

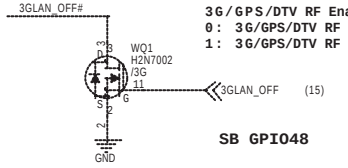
WR43:
For 3.5G/WIMAX: 0ohm
For GPS: 100Kohm

MINICARD use 12G03010052K

External Antenna

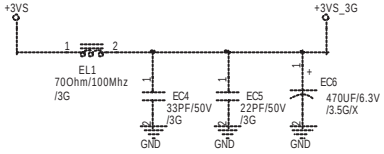


For DTV: 12G310077003
For GPS: 14G15B003000



3G/GPS/DTV RF Enable, default:1
0: 3G/GPS/DTV RF Enable
1: 3G/GPS/DTV RF Disable

SB GPIO48



<Core Design>

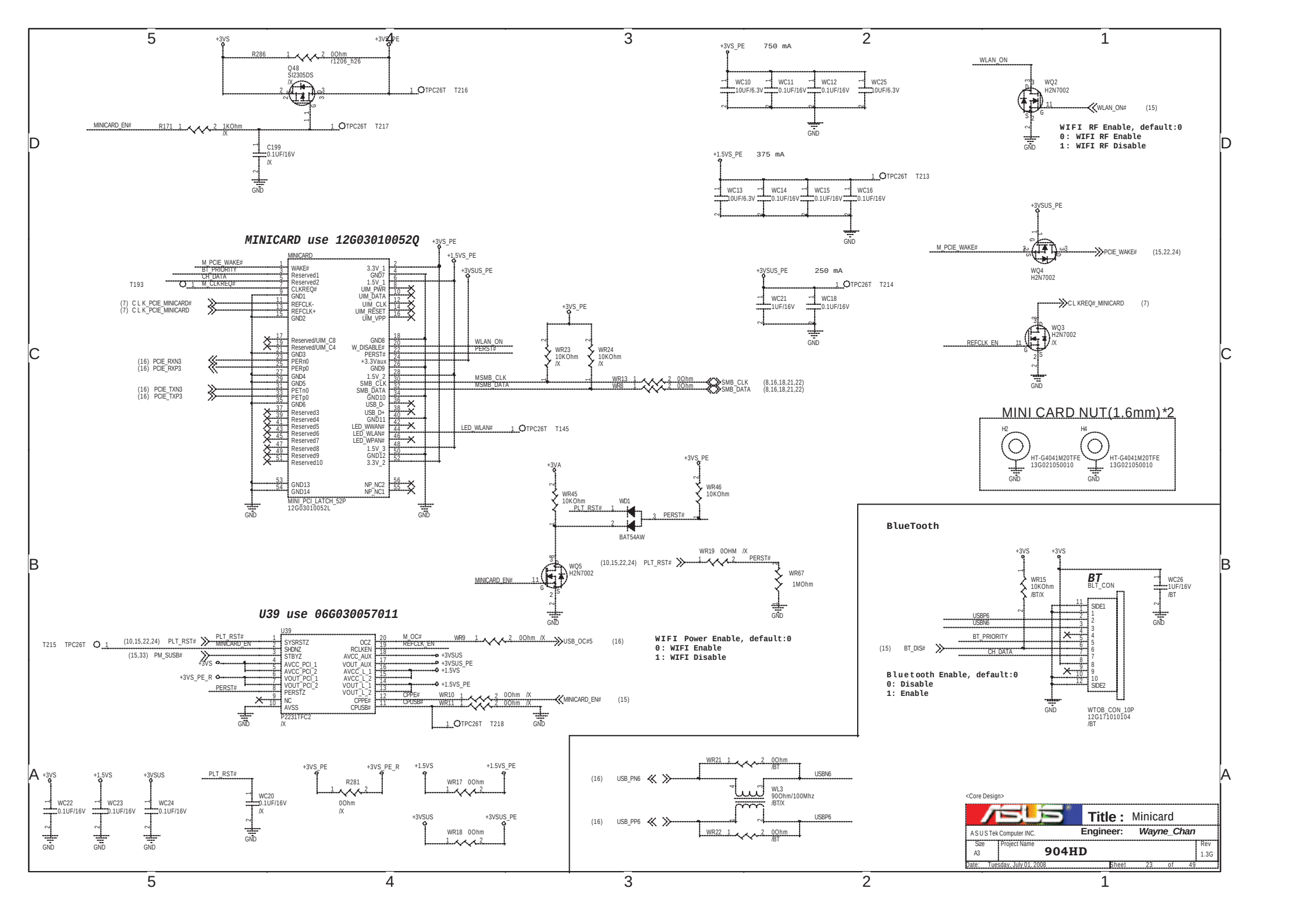
3.5G Module & External Antenna

Title :

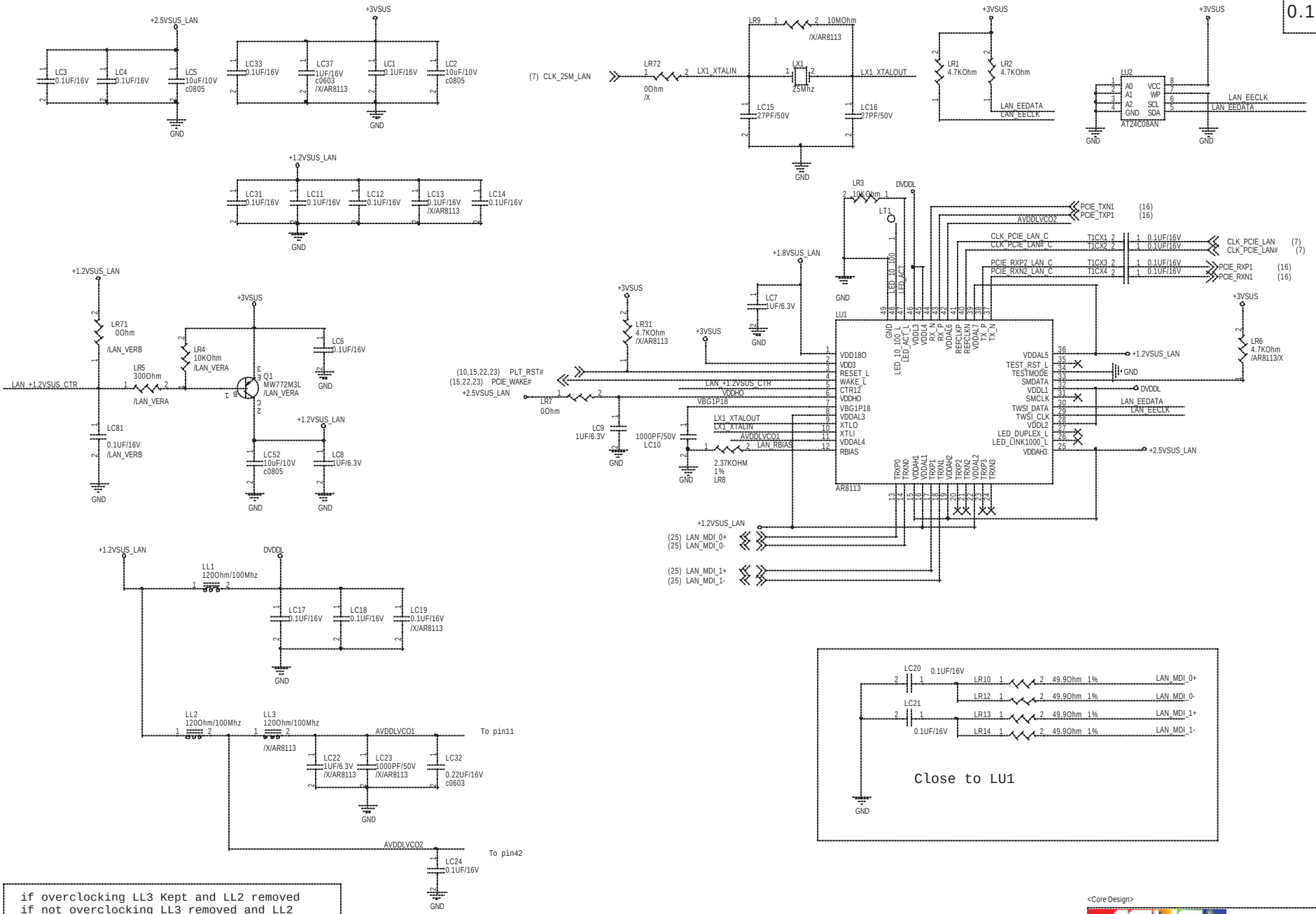
ASUS Tek Computer INC. **Engineer:** *Wayne_Chan*

Size	Project Name	Rev
A3	**904HD**	1.3G

Date: Tuesday, July 01, 2008 Sheet 22 of 49


MINICARD use 12G030010052Q
U39 use 06G030057011
MINI CARD NUT(1.6mm)*2
BlueTooth
WIFI RF Enable, default:0
0: WIFI RF Enable
1: WIFI RF Disable
WIFI Power Enable, default:0
0: WIFI Enable
1: WIFI Disable
Bluetooth Enable, default:0
0: Disable
1: Enable
Title : Minicard
Engineer: Wayne_Chan
ASUS Tek Computer INC.
904HD
Tuesday, July 01, 2008

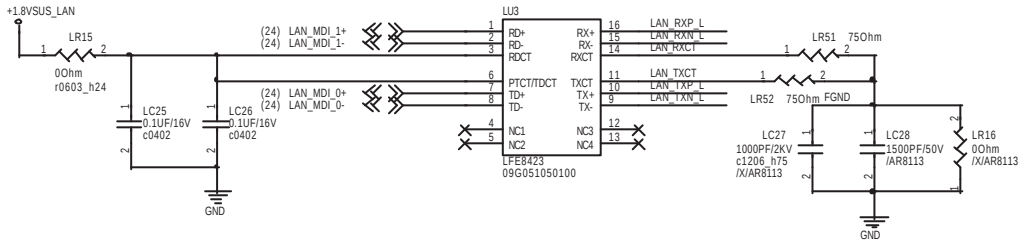
0.1A Beta



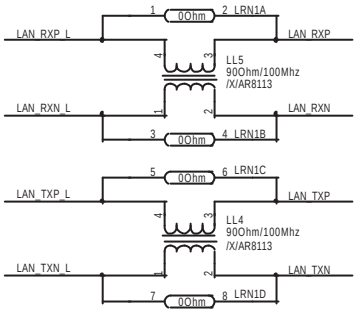
if overclocking LL3 Kept and LL2 removed
if not overclocking LL3 removed and LL2 Kept

<Core Design>

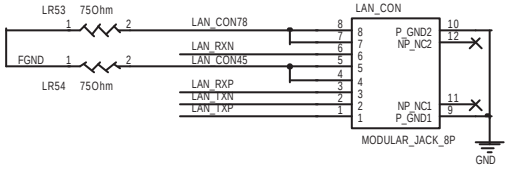
ASUS	Title : AR8113	
A S U S Tek Computer INC.	Engineer: *Wayne_Chan*	
Size: A3	Project Name: **904HD**	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 24 of 49	



4R8P 0603

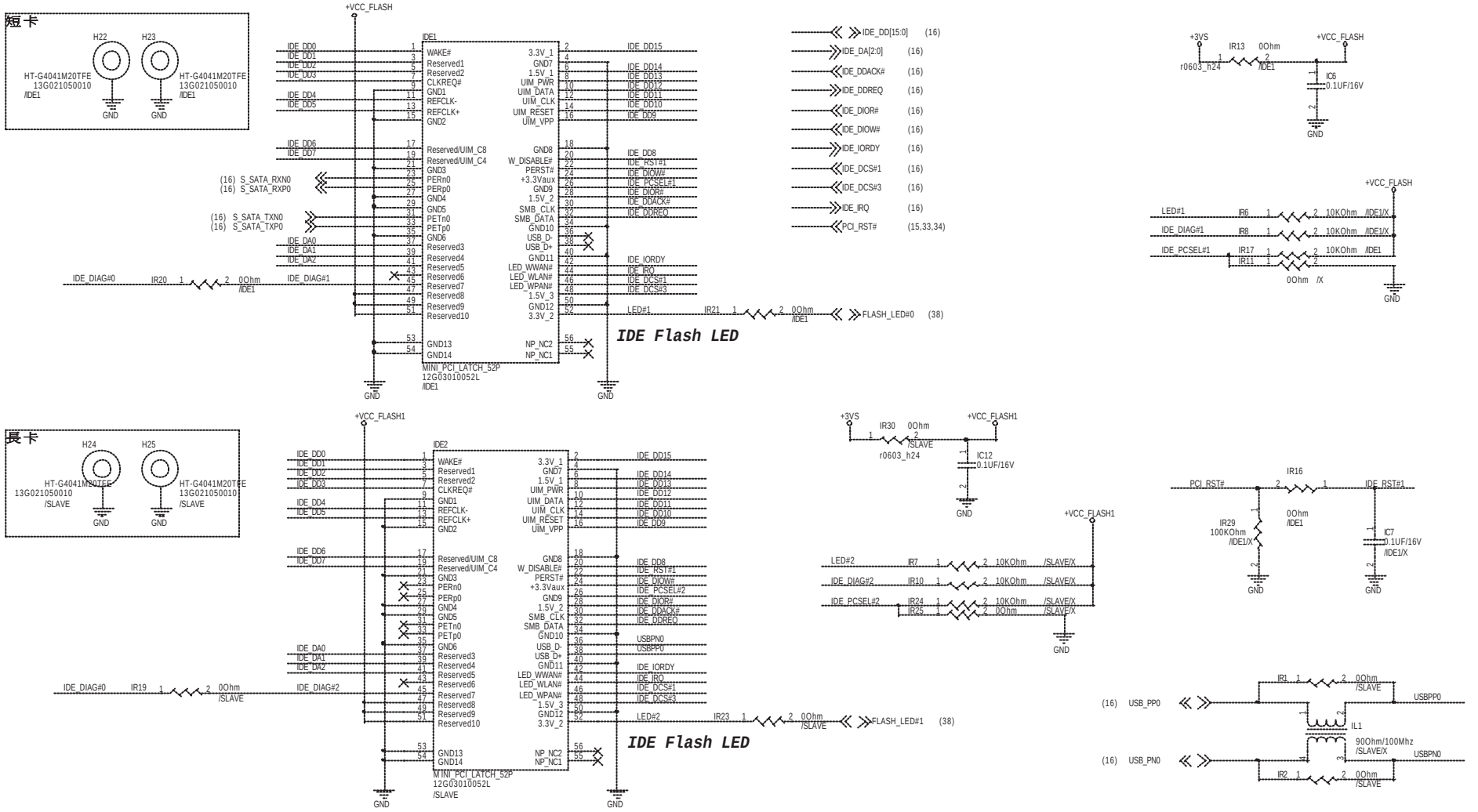


LAN connector: 12G148301086



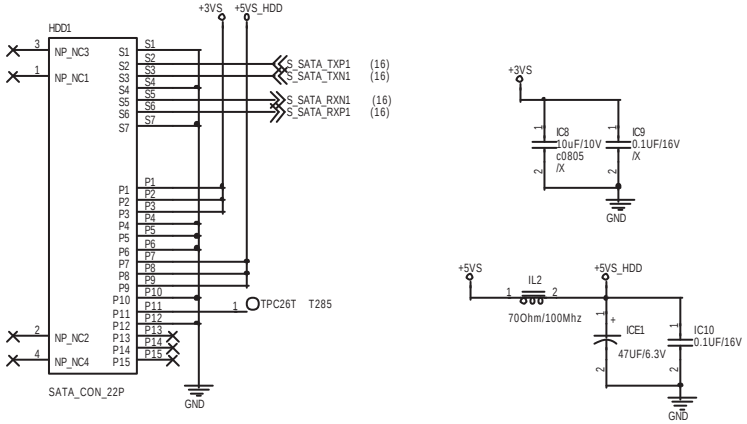
<Core Design>

ASUS	**Title :** MDC_RJ45	
A S U S Tek Computer INC.	**Engineer:** *Wayne_Chan*	
Size: A3	Project Name: **904HD**	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 25 of 49	


短卡
H22
H23
HT-G4041M20TFE
13G021050010
/IDE1
GND
+VCC_FLASH
IDE1
WAKE#
Reserved1
Reserved2
CLKREQ#
GND1
REFCLK-
REFCLK+
GND2
Reserved/UIM_C8
Reserved/UIM_C4
GND3
PERn0
PERp0
GND4
GND5
PETn0
PETp0
GND6
Reserved3
Reserved4
Reserved5
Reserved6
Reserved7
Reserved8
Reserved9
Reserved10
GND13
GND14
3.3V_1
GND7
1.5V_1
UIM_PWR
UIM_DATA
UIM_CLK
UIM_RESET
UIM_VPP
GND8
W_DISABLE#
PERST#
+3.3Vaux
GND9
1.5V_2
SMB_CLK
SMB_DATA
GND10
USB_D-
USB_D+
GND11
LED_WWAN#
LED_WLAN#
LED_WPAN#
1.5V_3
GND12
3.3V_2
NP_NC2
NP_NC1
MINI_PCI_LATCH_52P
12G03010052L
/IDE1
IDE_DD0
IDE_DD1
IDE_DD2
IDE_DD3
IDE_DD4
IDE_DD5
IDE_DD6
IDE_DD7
IDE_DA0
IDE_DA1
IDE_DA2
IDE_DD15
IDE_DD14
IDE_DD13
IDE_DD12
IDE_DD11
IDE_DD10
IDE_DD9
IDE_DD8
IDE_RST#1
IDE_DIOW#
IDE_PCSEL#1
IDE_DIOR#
IDE_DDACK#
IDE_DDREQ
IDE_IORDY
IDE_IRQ
IDE_DCS#1
IDE_DCS#3
(16) S_SATA_RXN0
(16) S_SATA_RXP0
(16) S_SATA_TXN0
(16) S_SATA_TXP0
IDE_DIAG#0
IR20 1 2 0Ohm
/IDE1
IDE_DIAG#1
IDE_DD[15:0] (16)
IDE_DA[2:0] (16)
IDE_DDACK# (16)
IDE_DDREQ (16)
IDE_DIOR# (16)
IDE_DIOW# (16)
IDE_IORDY (16)
IDE_DCS#1 (16)
IDE_DCS#3 (16)
IDE_IRQ (16)
PCI_RST# (15,33,34)
LED#1
IR21 1 2 0Ohm
/IDE1
FLASH_LED#0 (38)
IDE Flash LED
+3VS
IR13 0Ohm
r0603_h24
+VCC_FLASH
IC6
0.1UF/16V
LED#1
IR6 1 2 10KOhm /IDE1/X
IDE_DIAG#1
IR8 1 2 10KOhm /IDE1/X
IDE_PCSEL#1
IR17 1 2 10KOhm /IDE1
IR11 1 2 0Ohm /X
長卡
H24
H25
HT-G4041M20TFE
13G021050010
/SLAVE
+VCC_FLASH1
IDE2
MINI_PCI_LATCH_52P
12G03010052L
/SLAVE
IDE_DIAG#0
IR19 1 2 0Ohm
/SLAVE
IDE_DIAG#2
LED#2
IR23 1 2 0Ohm
/SLAVE
FLASH_LED#1 (38)
IDE Flash LED
+3VS
IR30 0Ohm
/SLAVE
r0603_h24
IC12
0.1UF/16V
LED#2
IR7 1 2 10KOhm /SLAVE/X
IDE_DIAG#2
IR10 1 2 10KOhm /SLAVE/X
IDE_PCSEL#2
IR24 1 2 10KOhm /SLAVE/X
IR25 1 2 0Ohm /SLAVE/X
IR16
PCI_RST#
IDE_RST#1
0Ohm
/IDE1
IR29
100KOhm
/IDE1/X
IC7
0.1UF/16V
/IDE1/X
(16) USB_PP0
IR1 1 2 0Ohm
/SLAVE
USBPP0
IL1
90Ohm/100Mhz
/SLAVE/X
(16) USB_PN0
IR2 1 2 0Ohm
/SLAVE
USBPN0
Naming Rule:
IC:IU?
R:IR?
C:IC?
L:IL?
<Core Design>
Title : Flash Conn
A S U S Tek Computer INC.
Engineer: Wayne_Chan
Size
A3
Project Name
904HD
Rev
1.3G
Date: Tuesday, July 01, 2008
Sheet 26 of 49

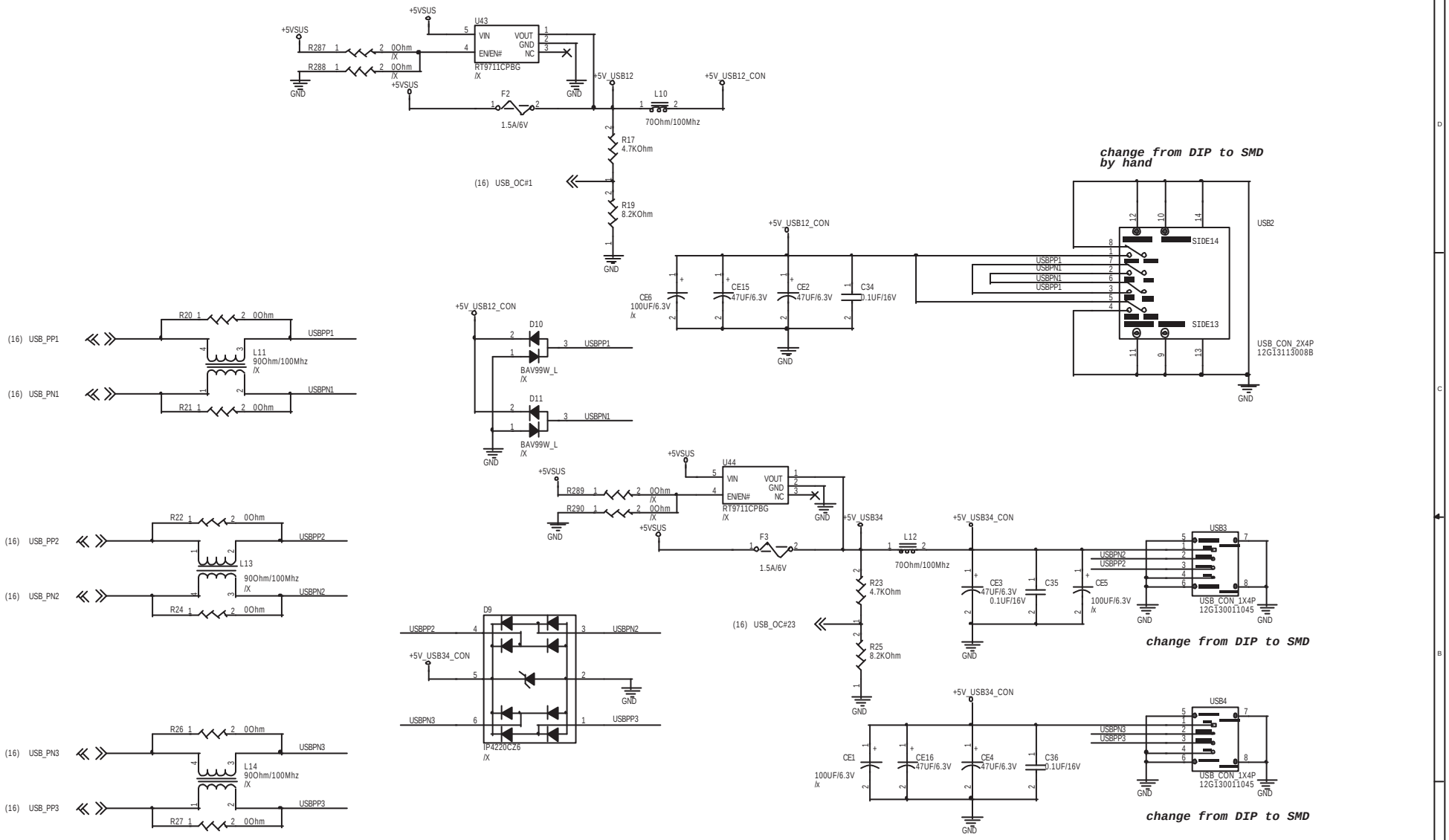
Change ODD to SATA IF

SATA HDD Connector



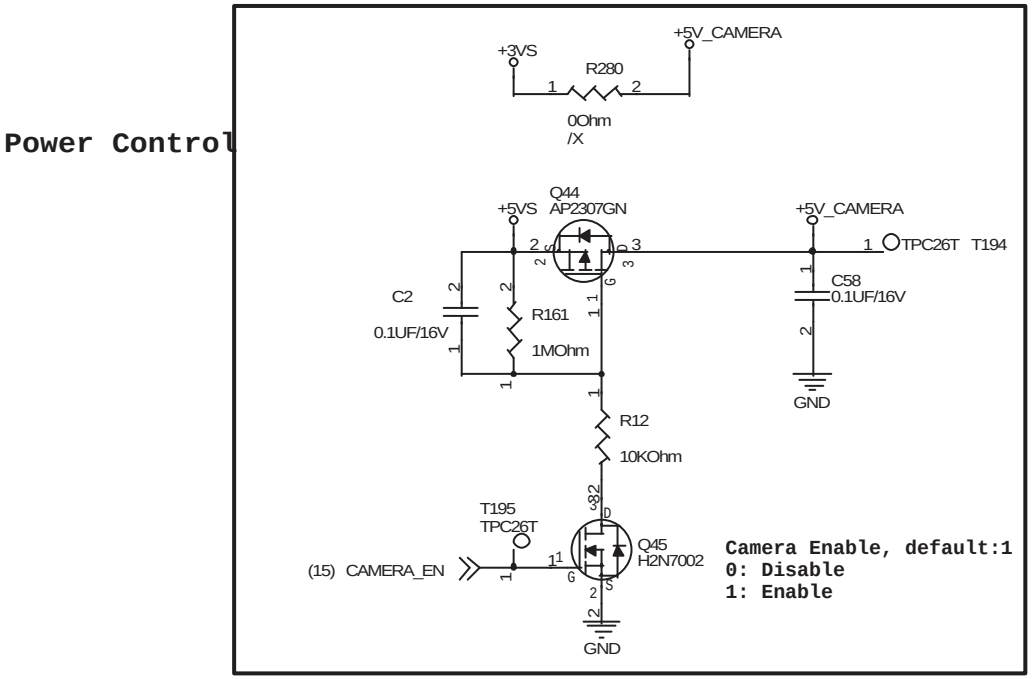
<Core Design>

ASUSTek Computer INC.	Title : HD + Flash Conn	
	Engineer: *Wayne_Chan*	
Size: A3	Project Name: 904HD	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 27 of 49	

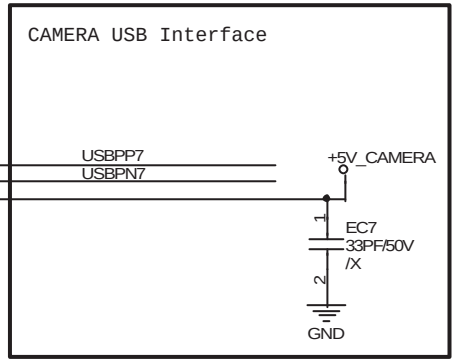


<Core Design>

ASUS Tek Computer INC.	Title : USB Port	
	Engineer: Wayne_Chan	
Size: A3	Project Name: 904HD	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 28 of 49	

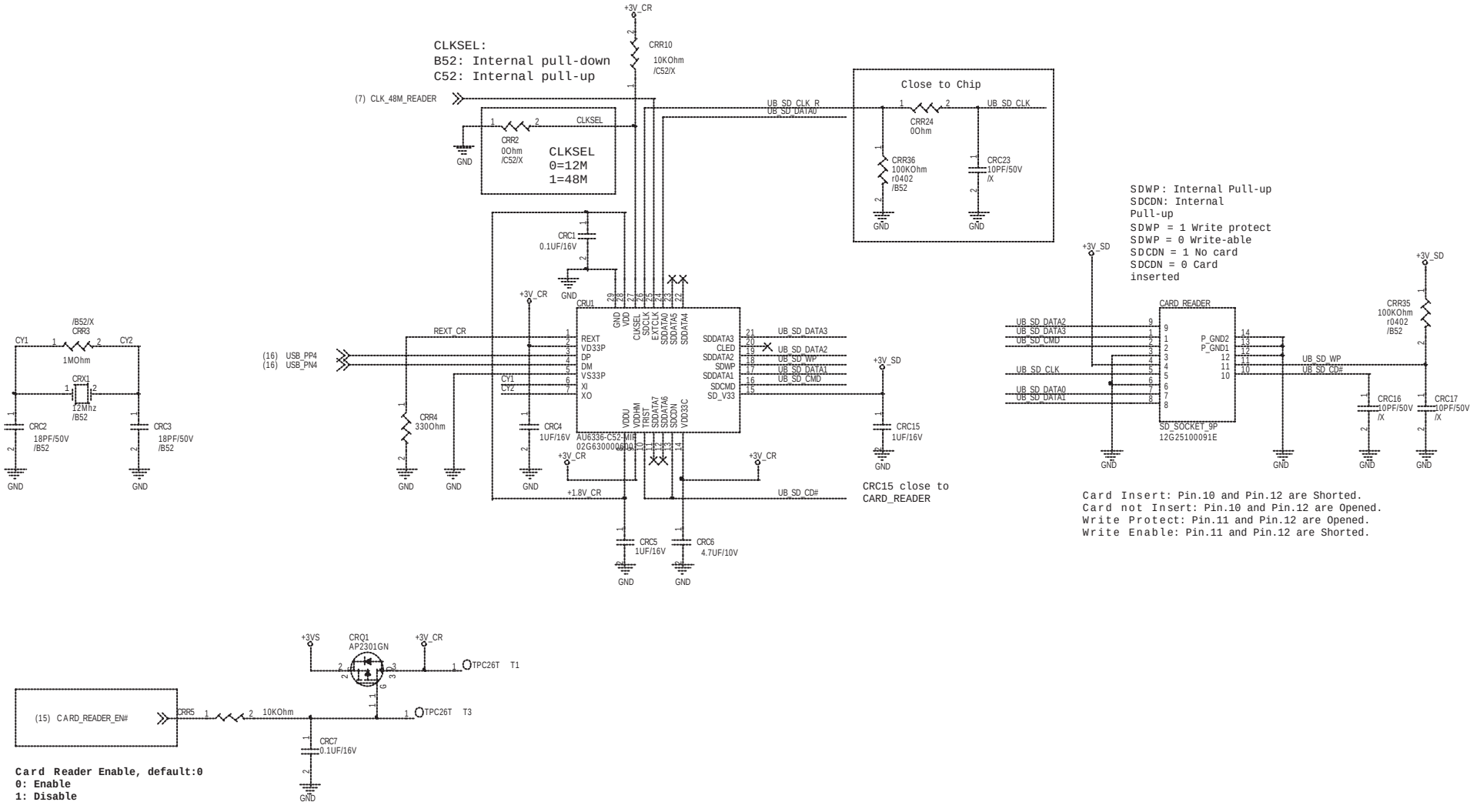






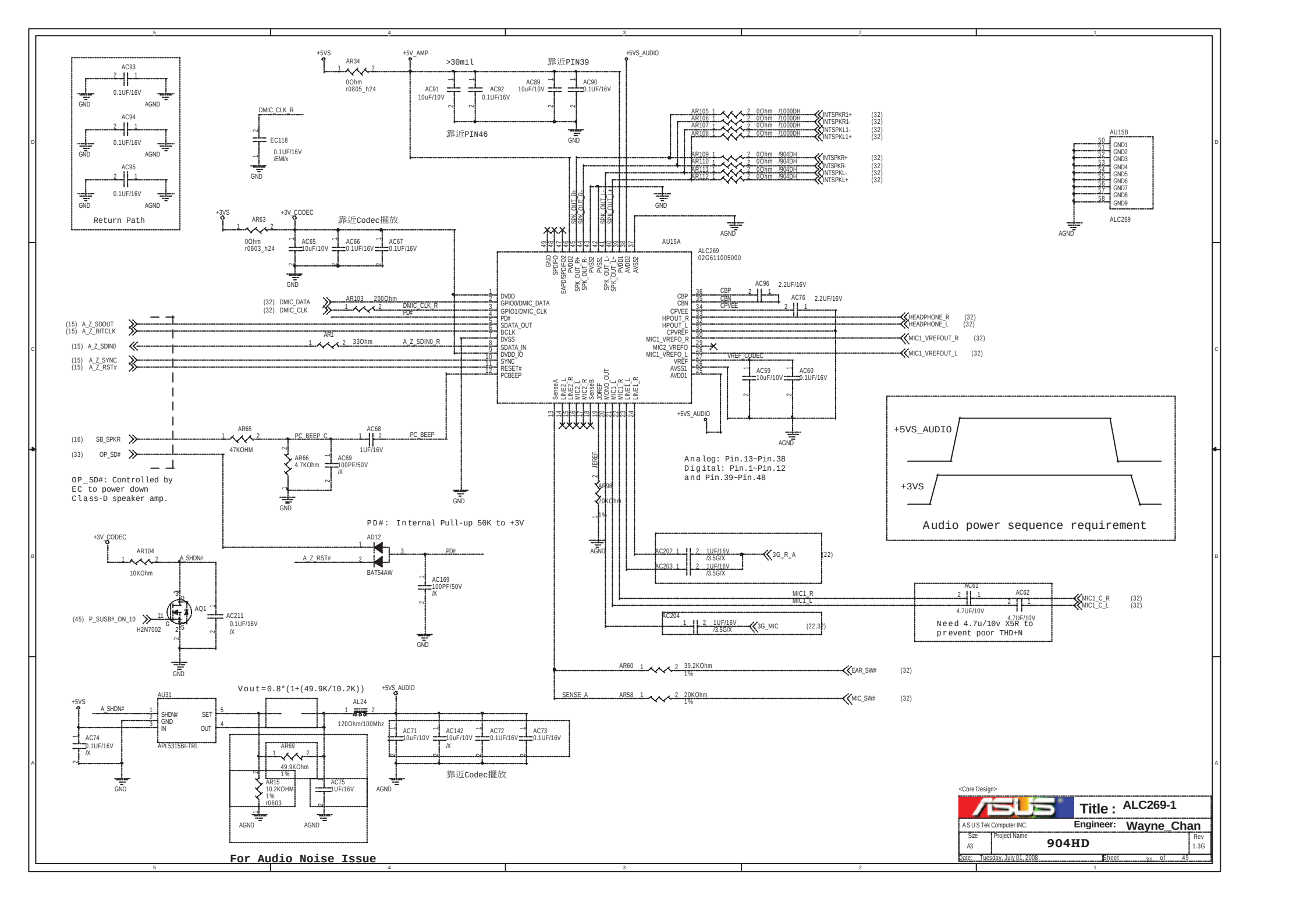
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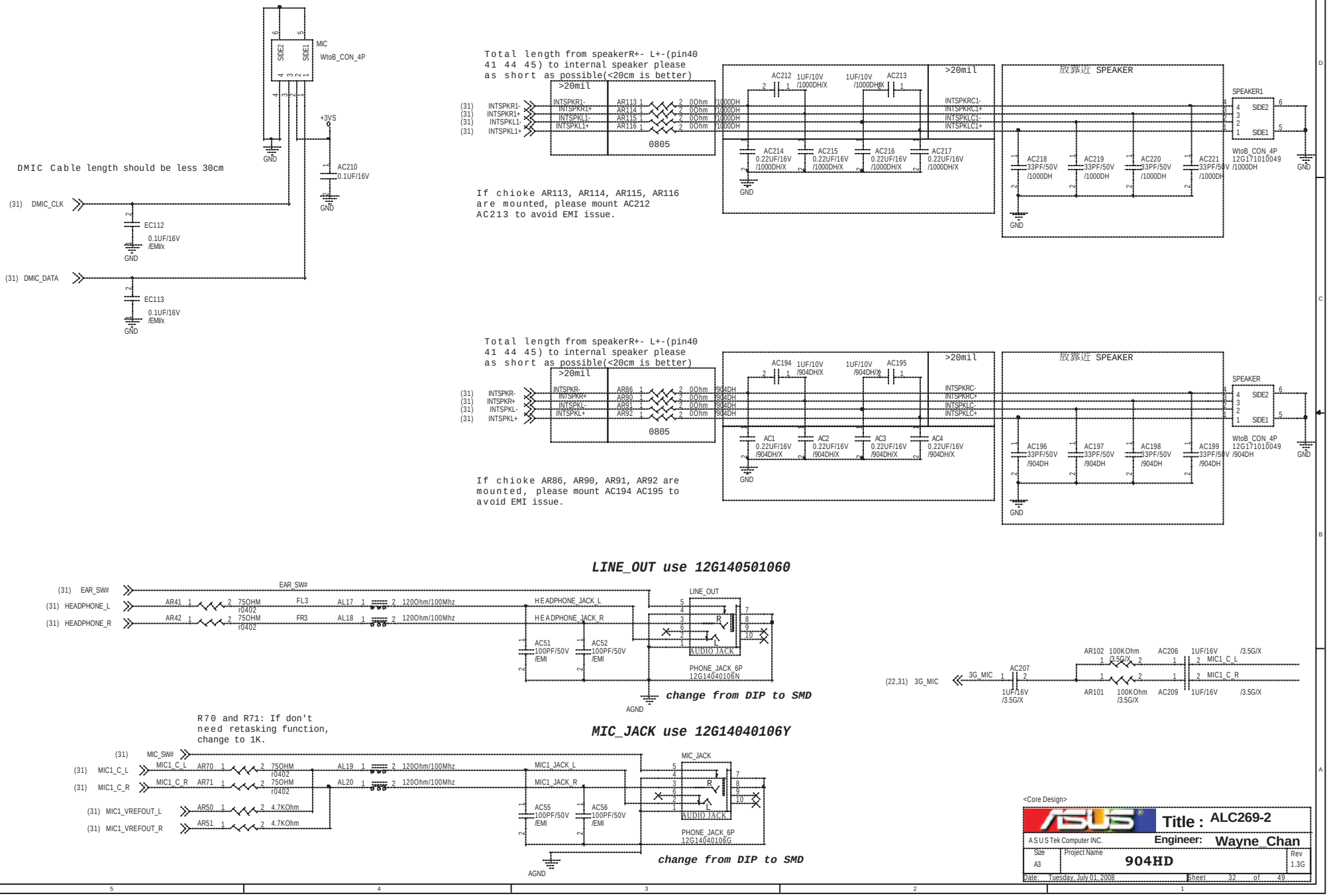
ASUSTek Computer INC.	Title : Camera Power	
	Engineer: Wayne_Chan	
Size: A4	Project Name: 904HD	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 29 of 49	

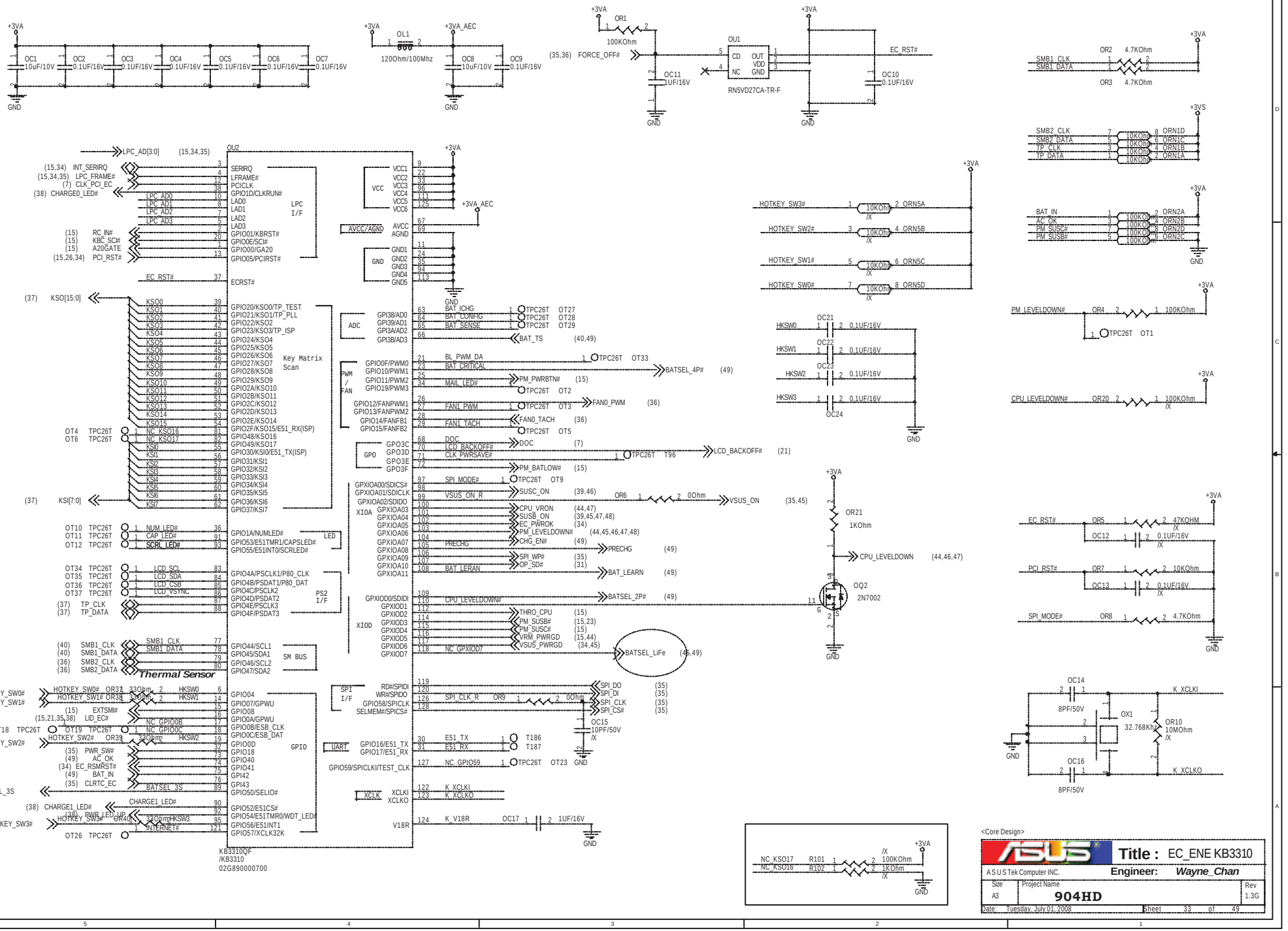


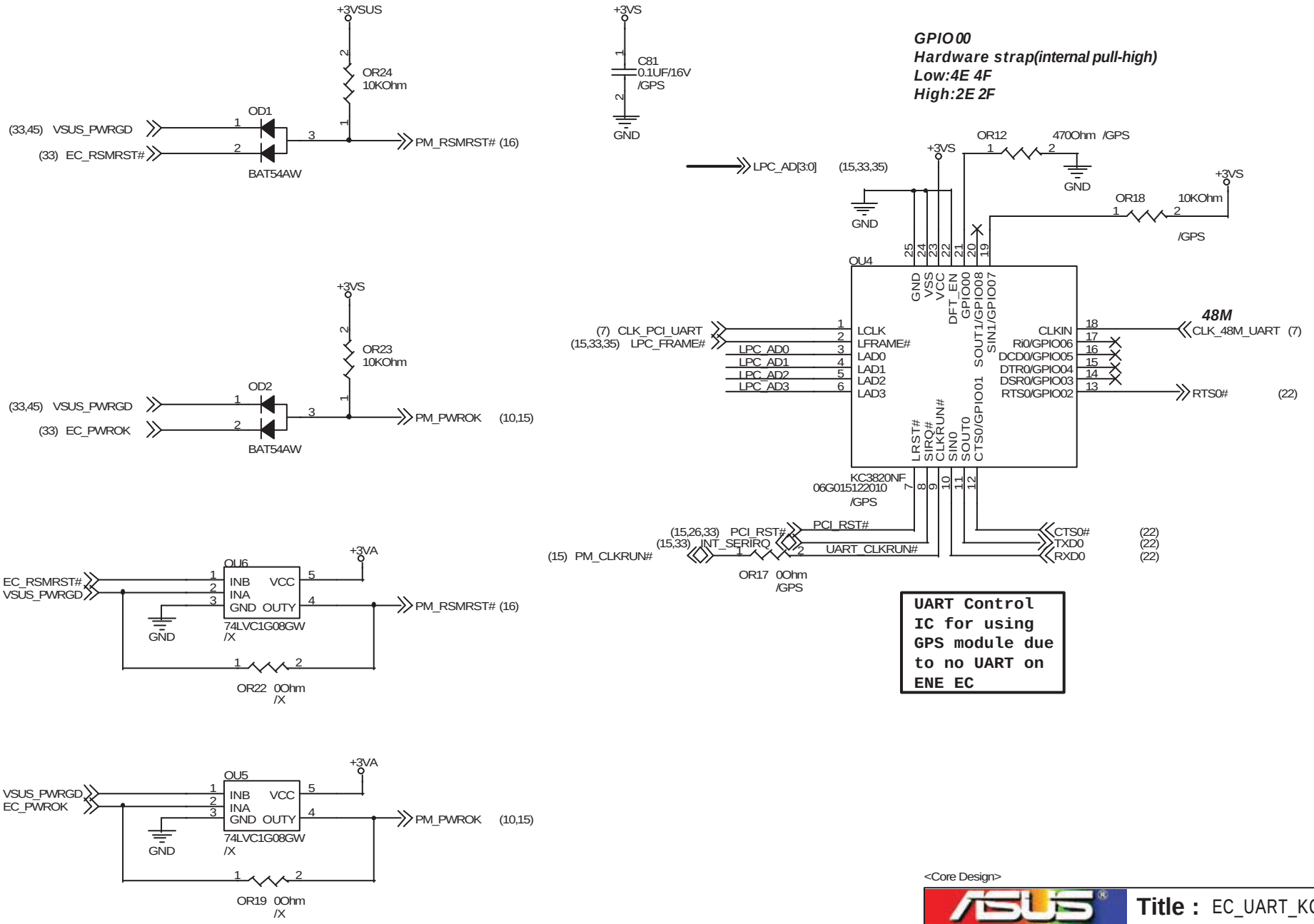
<Core Design>

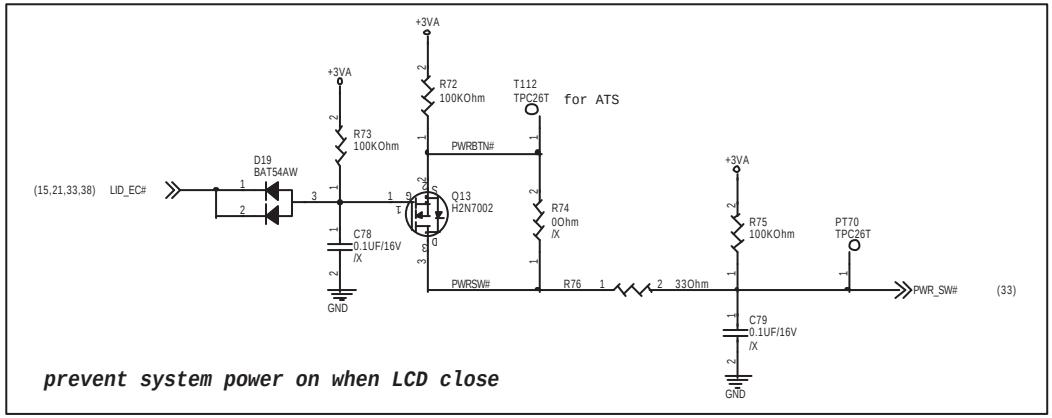
ASUS Tek Computer INC.	Title : AU6336-C52	
	Engineer: Wayne_Chan	
Size: A3	Project Name: 904HD	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 30 of 49	

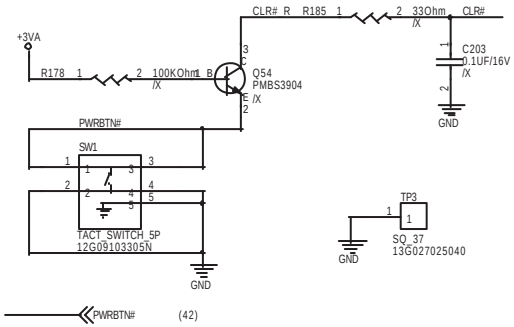

Return Path
AC93 0.1UF/16V
AC94 0.1UF/16V
AC95 0.1UF/16V
GND
AGND
+5VS
AR34 0Ohm r0805_h24
+5V_AMP
>30mil
靠近PIN39
+5VS_AUDIO
AC91 10uF/10V
AC92 0.1UF/16V
AC89 10uF/10V
AC90 0.1UF/16V
靠近PIN46
DMIC_CLK_R
EC118 0.1UF/16V /EMI/x
+3VS
AR63 0Ohm r0603_h24
+3V_CODEC
靠近Codec擺放
AC65 10uF/10V
AC66 0.1UF/16V
AC67 0.1UF/16V
AU15A
ALC269 02G611005000
AU15B
ALC269
AR105 AR106 AR107 AR108 0Ohm /1000DH
AR109 AR110 AR111 AR112 0Ohm /804DH
INTSPKR1+ INTSPKR1- INTSPKL1- INTSPKL1+
INTSPKR+ INTSPKR- INTSPKL- INTSPKL+
(32)
DVDD
GPIO0/DMIC_DATA
GPIO1/DMIC_CLK
PD#
SDATA_OUT
BCLK
DVSS
SDATA_IN
DVDD_IO
SYNC
RESET#
PCBEEP
(32) DMIC_DATA
(32) DMIC_CLK
AR103 200Ohm
DMIC_CLK_R
PD#
(15) A_Z_SDOUT
(15) A_Z_BITCLK
(15) A_Z_SDIN0
(15) A_Z_SYNC
(15) A_Z_RST#
AR1 33Ohm
A_Z_SDIN0_R
CBP
CBN
CPVEE
HPOUT_R
HPOUT_L
CPVREF
MIC1_VREFO_R
MIC2_VREFO
MIC1_VREFO_L
VREF
AVSS1
AVDD1
AC96 2.2UF/16V
AC76 2.2UF/16V
HEADPHONE_R
HEADPHONE_L
MIC1_VREFOUT_R
MIC1_VREFOUT_L
VREF_CODEC
AC59 10uF/10V
AC60 0.1UF/16V
(16) SB_SPKR
(33) OP_SD#
AR65 47KOHM
PC_BEEP_C
PC_BEEP
AC68 1UF/16V
AR66 4.7KOhm
AC69 100PF/50V /X
OP_SD#: Controlled by EC to power down Class-D speaker amp.
PD#: Internal Pull-up 50K to +3V
Analog: Pin.13~Pin.38
Digital: Pin.1~Pin.12
and Pin.39~Pin.48
+5VS_AUDIO
+3VS
Audio power sequence requirement
JDREF
AR98 20KOhm 1%
AC202 AC203 1UF/16V /3.5G/X
3G_R_A (22)
3G_MIC (22,32)
MIC1_R
MIC1_L
AC61 AC62 4.7UF/10V
MIC1_C_R
MIC1_C_L
Need 4.7u/10v X5R to prevent poor THD+N
+3V_CODEC
AR104 10KOhm
A_SHDN#
AQ1 H2N7002
(45) P_SUSB#_ON_10
AC211 0.1UF/16V /X
AD12 BAT54AW
A_Z_RST#
PD#
AC169 100PF/50V /X
AR60 39.2KOhm 1%
EAR_SW#
SENSE_A
AR58 20KOhm 1%
MIC_SW#
Vout=0.8*(1+(49.9K/10.2K))
AU31
APL5315BI-TRL
SHDN#
GND
IN
SET
OUT
AL24 120Ohm/100Mhz
AC74 0.1UF/16V /X
AC71 10uF/10V
AC142 10uF/10V /X
AC72 0.1UF/16V
AC73 0.1UF/16V
AR69 49.9KOhm 1%
AR15 10.2KOHM 1% r0603
AC75 1UF/16V
For Audio Noise Issue
<Core Design>
Title : ALC269-1
A S U S Tek Computer INC.
Engineer: Wayne_Chan
Size A3
Project Name 904HD
Rev 1.3G
Date: Tuesday, July 01, 2008
Sheet 21 of 49

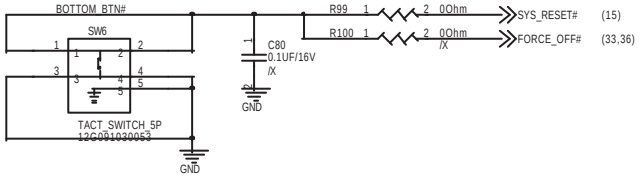

MIC
WtoB_CON_4P
SIDE2
SIDE1
+3VS
GND
AC210
0.1UF/16V
/EMIx
DMIC Cable length should be less 30cm
(31) DMIC_CLK
(31) DMIC_DATA
EC112
EC113
0.1UF/16V
/EMIx
Total length from speakerR+- L+-(pin40 41 44 45) to internal speaker please as short as possible(<20cm is better)
>20mil
INTSPKR1-
INTSPKR1+
INTSPKL1-
INTSPKL1+
AR113
AR114
AR115
AR116
0Ohm
/1000DH
0805
AC212
AC213
1UF/10V
/1000DH/X
AC214
AC215
AC216
AC217
0.22UF/16V
/1000DH/X
INTSPKRC1-
INTSPKRC1+
INTSPKLC1-
INTSPKLC1+
放靠近 SPEAKER
AC218
AC219
AC220
AC221
33PF/50V
/1000DH
SPEAKER1
WtoB_CON_4P
12G171010049
If chioke AR113, AR114, AR115, AR116 are mounted, please mount AC212 AC213 to avoid EMI issue.
Total length from speakerR+- L+-(pin40 41 44 45) to internal speaker please as short as possible(<20cm is better)
INTSPKR-
INTSPKR+
INTSPKL-
INTSPKL+
AR86
AR90
AR91
AR92
/904DH
AC194
AC195
AC1
AC2
AC3
AC4
/904DH/X
INTSPKRC-
INTSPKRC+
INTSPKLC-
INTSPKLC+
AC196
AC197
AC198
AC199
/904DH
If chioke AR86, AR90, AR91, AR92 are mounted, please mount AC194 AC195 to avoid EMI issue.
LINE_OUT use 12G140501060
(31) EAR_SW#
(31) HEADPHONE_L
(31) HEADPHONE_R
AR41
AR42
75OHM
r0402
FL3
FR3
AL17
AL18
120Ohm/100Mhz
HEADPHONE_JACK_L
HEADPHONE_JACK_R
LINE_OUT
AC51
AC52
100PF/50V
/EMI
AUDIO JACK
PHONE_JACK_6P
12G140401O6N
AGND
change from DIP to SMD
(22,31) 3G_MIC
AC207
1UF/16V
/3.5G/X
AR102
AR101
100KOhm
/3.5G/X
AC206
AC209
MIC1_C_L
MIC1_C_R
R70 and R71: If don't need retasking function, change to 1K.
MIC1_SW#
MIC1_C_L
MIC1_C_R
AR70
AR71
MIC1_JACK_L
MIC1_JACK_R
MIC_JACK
AC55
AC56
PHONE_JACK_6P
12G14040106G
(31) MIC1_VREFOUT_L
(31) MIC1_VREFOUT_R
AR50
AR51
4.7KOhm
MIC_JACK use 12G14040106Y
change from DIP to SMD
<Core Design>
Title : ALC269-2
ASUSTek Computer INC.
Engineer: Wayne_Chan
Size
A3
Project Name
904HD
Rev
1.3G
Date: Tuesday, July 01, 2008
Sheet 32 of 49

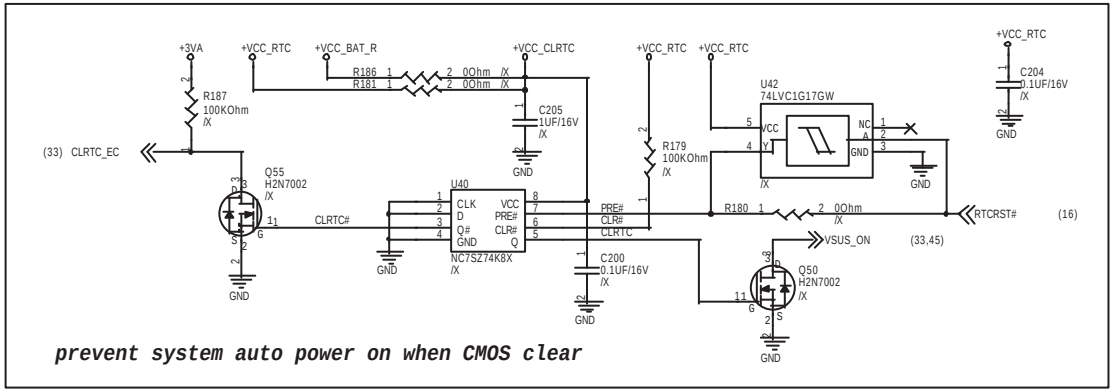

OU2
KB3310QF
/KB3310
02G890000700
Thermal Sensor
Key Matrix Scan
LPC I/F
PS2 I/F
SM BUS
LED
GPIO
SPI I/F
PWM / FAN
ADC
GPO
XIOA
XIOD
UART
XCLK
Title : EC_ENE KB3310
ASUS Tek Computer INC.
Engineer: Wayne_Chan
Project Name
904HD
Size
A3
Rev
1.3G
Date: Tuesday, July 01, 2008
Sheet 33 of 49
<Core Design>


+3VSUS
OR24
10KOhm
OD1
(33,45) VSUS_PWRGD
(33) EC_RSMRST#
BAT54AW
PM_RSMRST# (16)
+3VS
OR23
10KOhm
OD2
(33,45) VSUS_PWRGD
(33) EC_PWROK
BAT54AW
PM_PWROK (10,15)
+3VA
OU6
(33) EC_RSMRST#
(33,45) VSUS_PWRGD
INB VCC
INA
GND OUTY
74LVC1G08GW
/X
GND
PM_RSMRST# (16)
OR22 0Ohm
/X
OU5
(33,45) VSUS_PWRGD
(33) EC_PWROK
74LVC1G08GW
/X
PM_PWROK (10,15)
OR19 0Ohm
/X
+3VS
C81
0.1UF/16V
/GPS
GND
GPIO00
Hardware strap(internal pull-high)
Low:4E 4F
High:2E 2F
LPC_AD[3:0] (15,33,35)
OR12 470Ohm /GPS
OR18 10KOhm
/GPS
OU4
GND VSS VCC DFT_EN GPIO00 SOUT1/GPIO08 SIN1/GPIO07
(7) CLK_PCI_UART
(15,33,35) LPC_FRAME#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LCLK
LFRAME#
LAD0
LAD1
LAD2
LAD3
CLKIN
Ri0/GPIO06
DCD0/GPIO05
DTR0/GPIO04
DSR0/GPIO03
RTS0/GPIO02
48M
CLK_48M_UART (7)
RTS0# (22)
LRST# SIRQ# CLKRUN# SIN0 SOUT0 CTS0/GPIO01
KC3820NF
06G015122010
/GPS
(15,26,33) PCI_RST#
PCI_RST#
(15,33) INT_SERIRQ
UART_CLKRUN#
(15) PM_CLKRUN#
OR17 0Ohm
/GPS
CTS0# (22)
TXD0 (22)
RXD0 (22)
UART Control IC for using GPS module due to no UART on ENE EC
<Core Design>
Title : EC_UART_KC3820
ASUSTek Computer INC.
Engineer: Wayne_Chan
Size A4
Project Name 904HD
Rev 1.3G
Date: Tuesday, July 01, 2008
Sheet 34 of 49

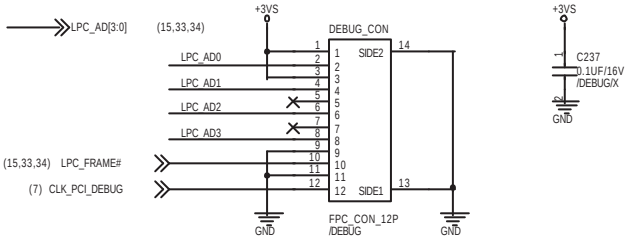




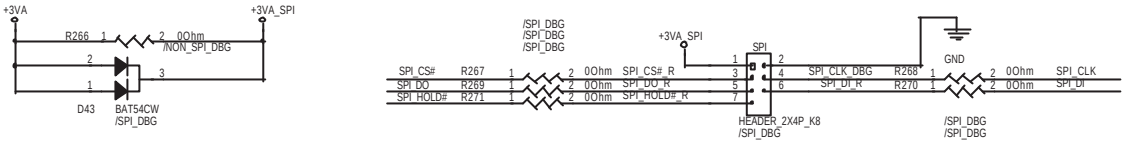


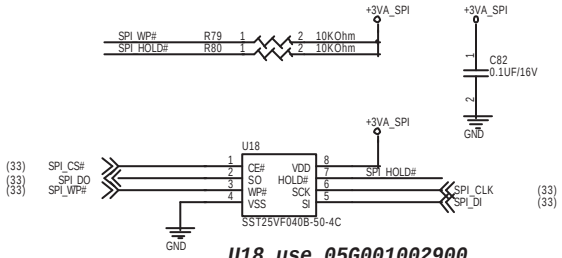


For Debug

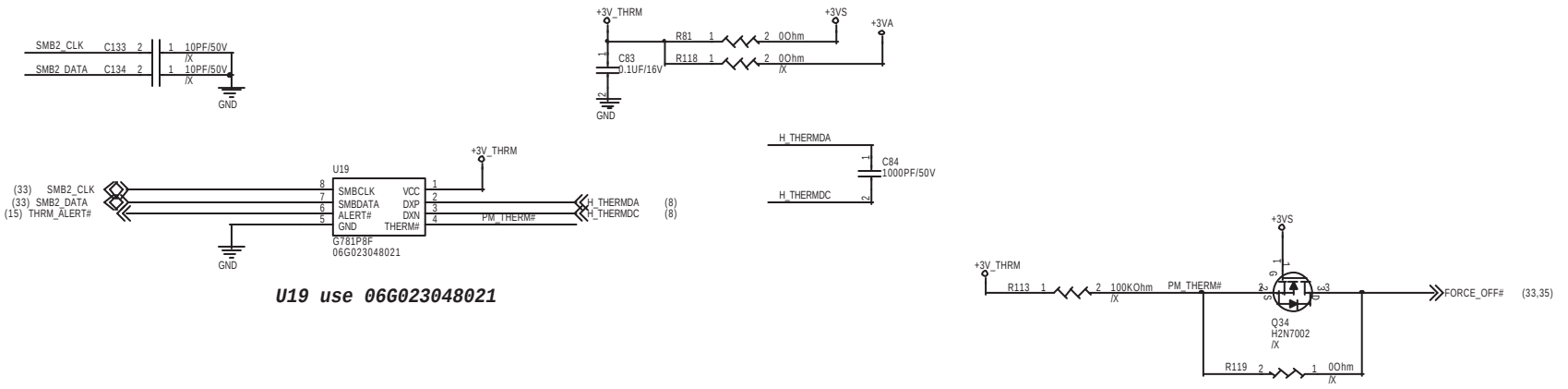


Debug Card cable use Z96 Touch Pad cable, P/N: 14G124110126, 14G124110120, 14G124110121 14G124110124, 14G124110125

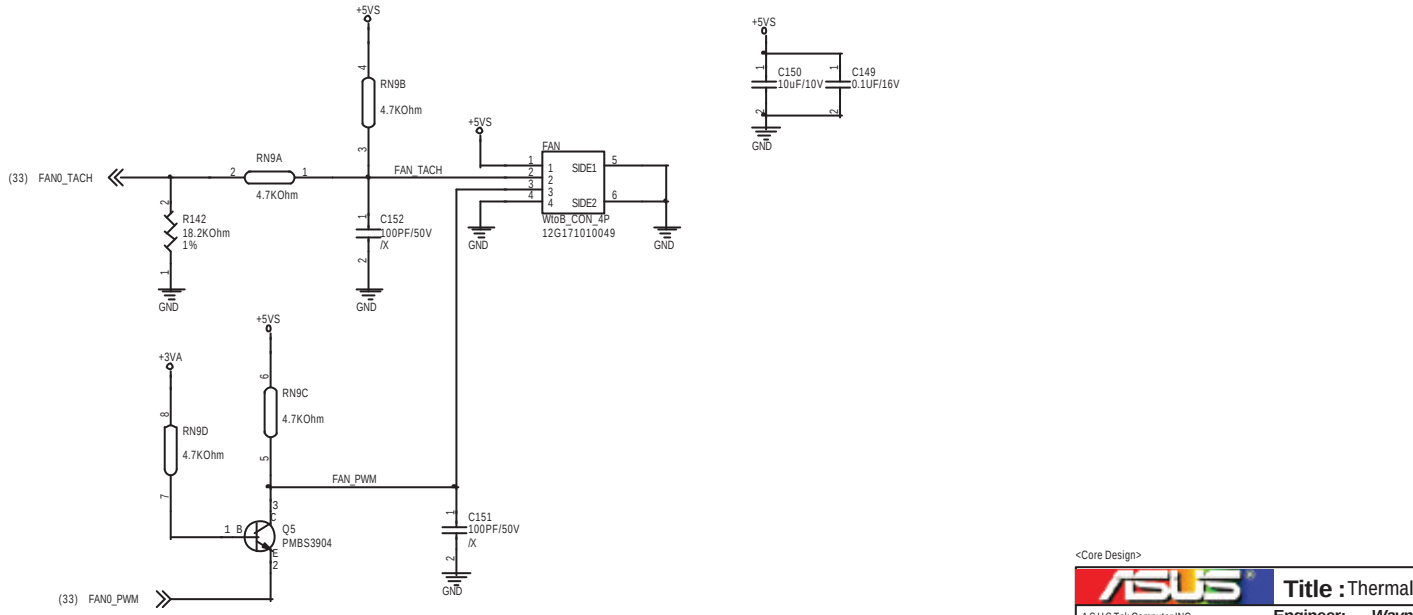




U18 use 05G001002900 & 05G00100F130



U19 use 06G023048021

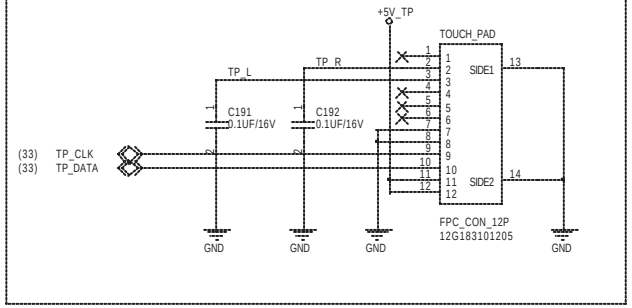


<Core Design>

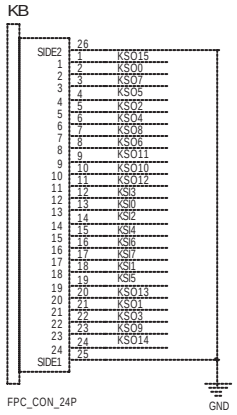
ASUS Tek Computer INC.	Title : Thermal Sensor_FAN	
	Engineer: *Wayne_Chan*	
Size: A3	Project Name: **904HD**	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 36 of 49	

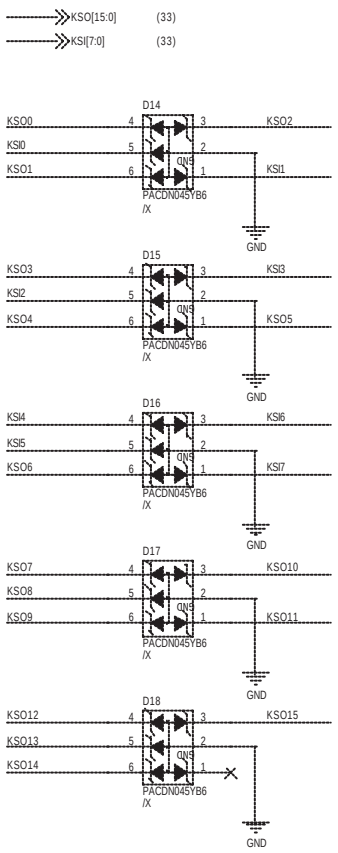
For Touch-Pad

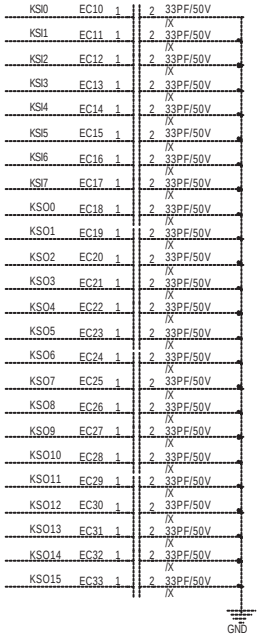
P900 R1.0G



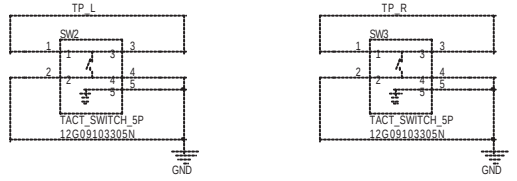
For Keyboard Connector

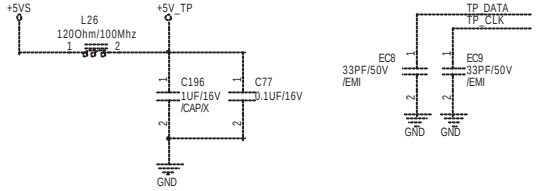


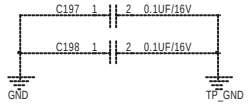


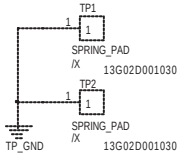


SW2, SW3 use 12G09103305N





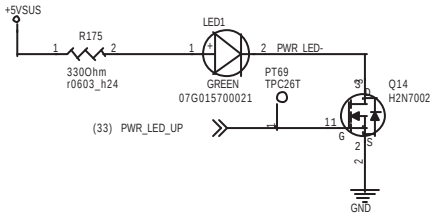




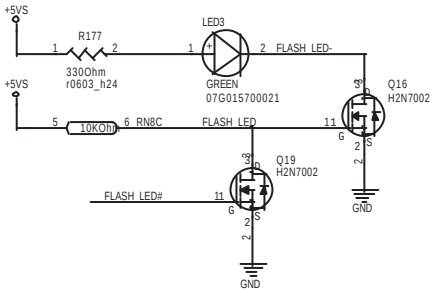
<Core Design>

ASUS Tek Computer INC.	Title : KB_Touch Pad	
	Engineer: Wayne_Chan	
Size: A3	Project Name: 904HD	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 37 of 49	

for POWER LED

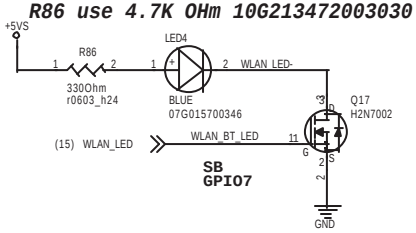


for FLASH LED



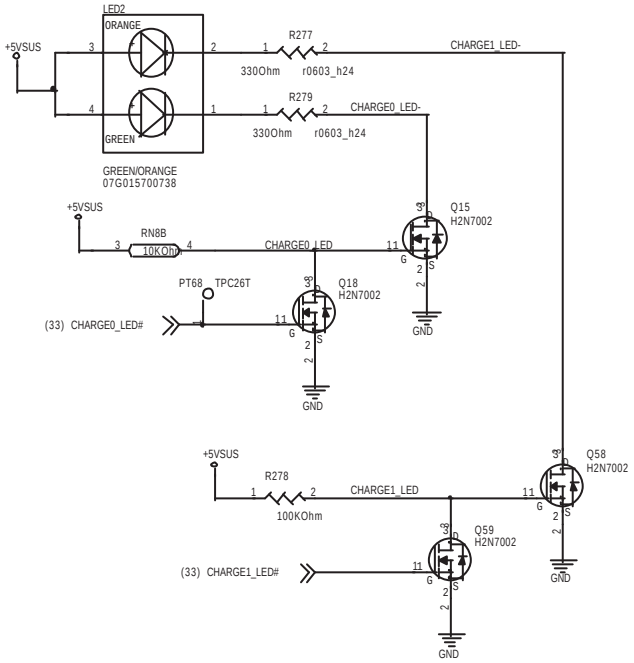
for WLAN/BlueTooth LED

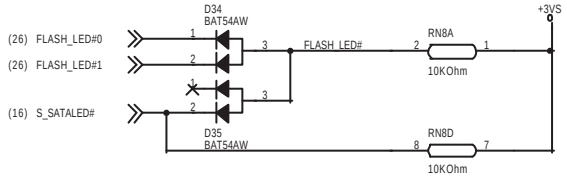
R86 use 4.7K OHm 10G213472003030



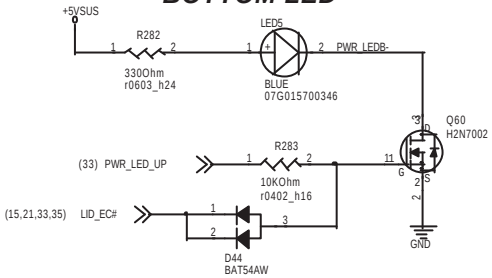
WIFI/BT LED Enable,default:1
0: WIFI and BT are both disabled
1: one of WIFI and BT is Enable or both are Enable

for CHARGE LED



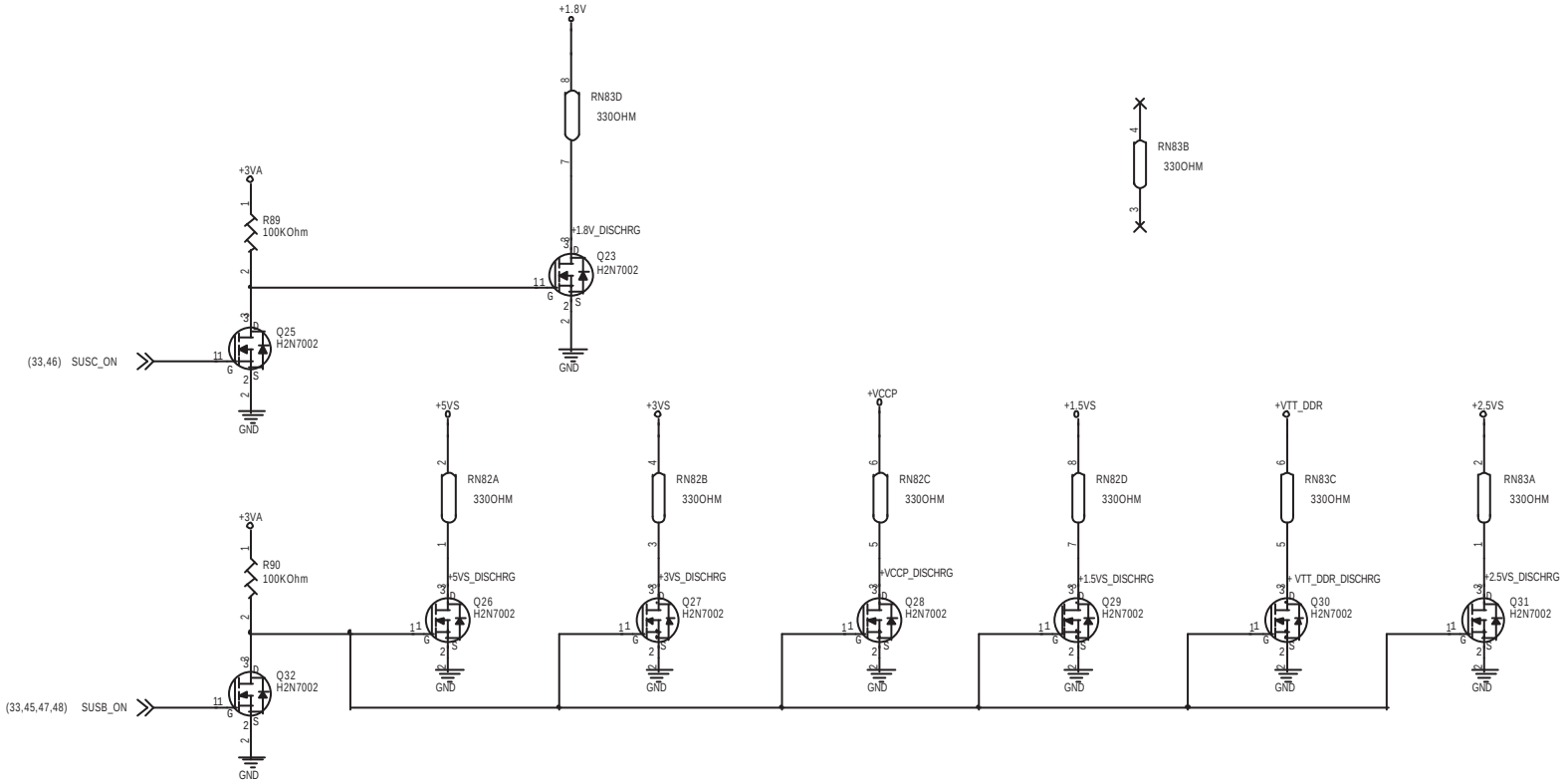


for POWER BOTTOM LED



<Core Design>

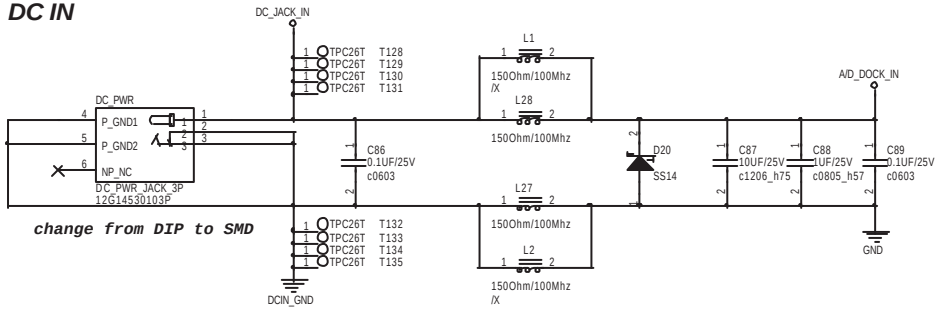
ASUS	Title : LED	
A S U S Tek Computer INC.	Engineer: *Wayne_Chan*	
Size: A3	Project Name: **904HD**	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 38 of 49	



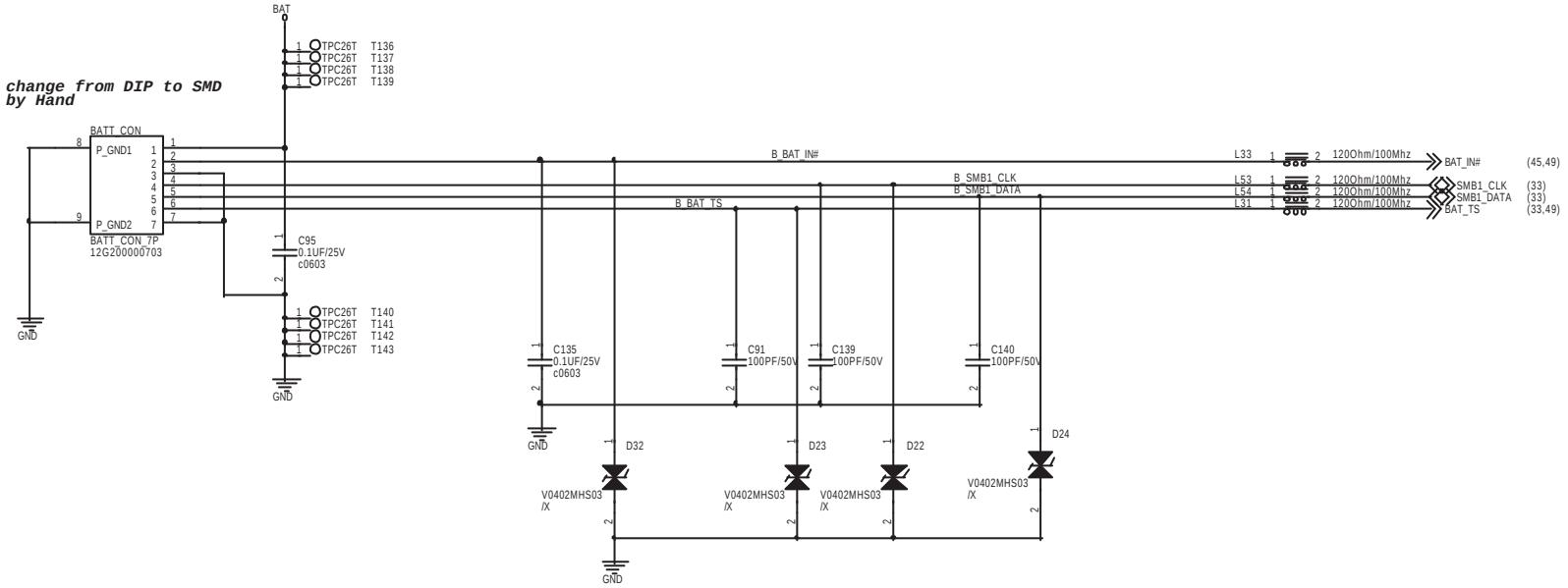
<Core Design>

ASUS	**Title :** Discharge	
A S U S Tek Computer INC.	**Engineer:** *Wayne_Chan*	
Size: A3	Project Name: **904HD**	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 39 of 49	

DC IN

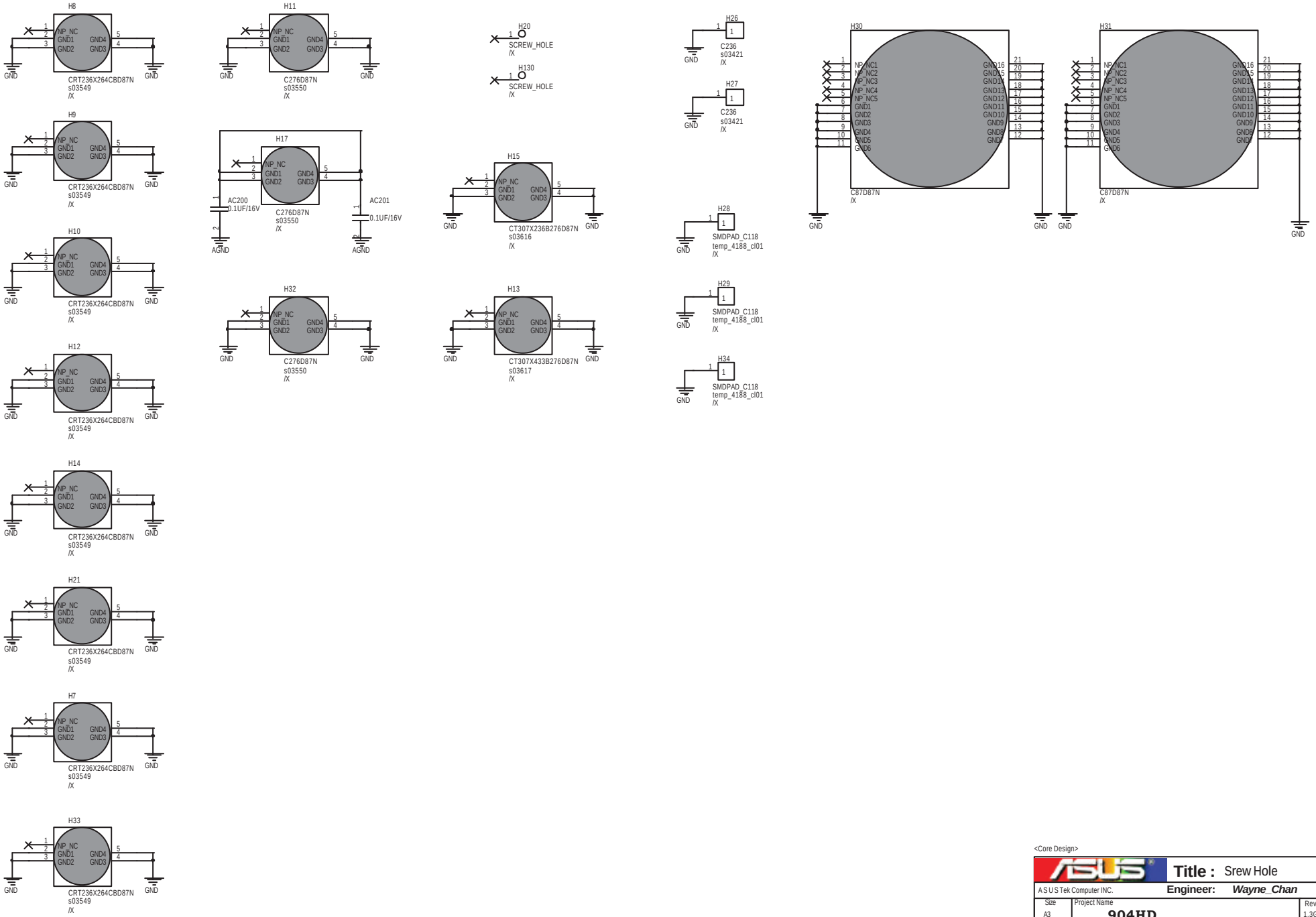


BAT IN



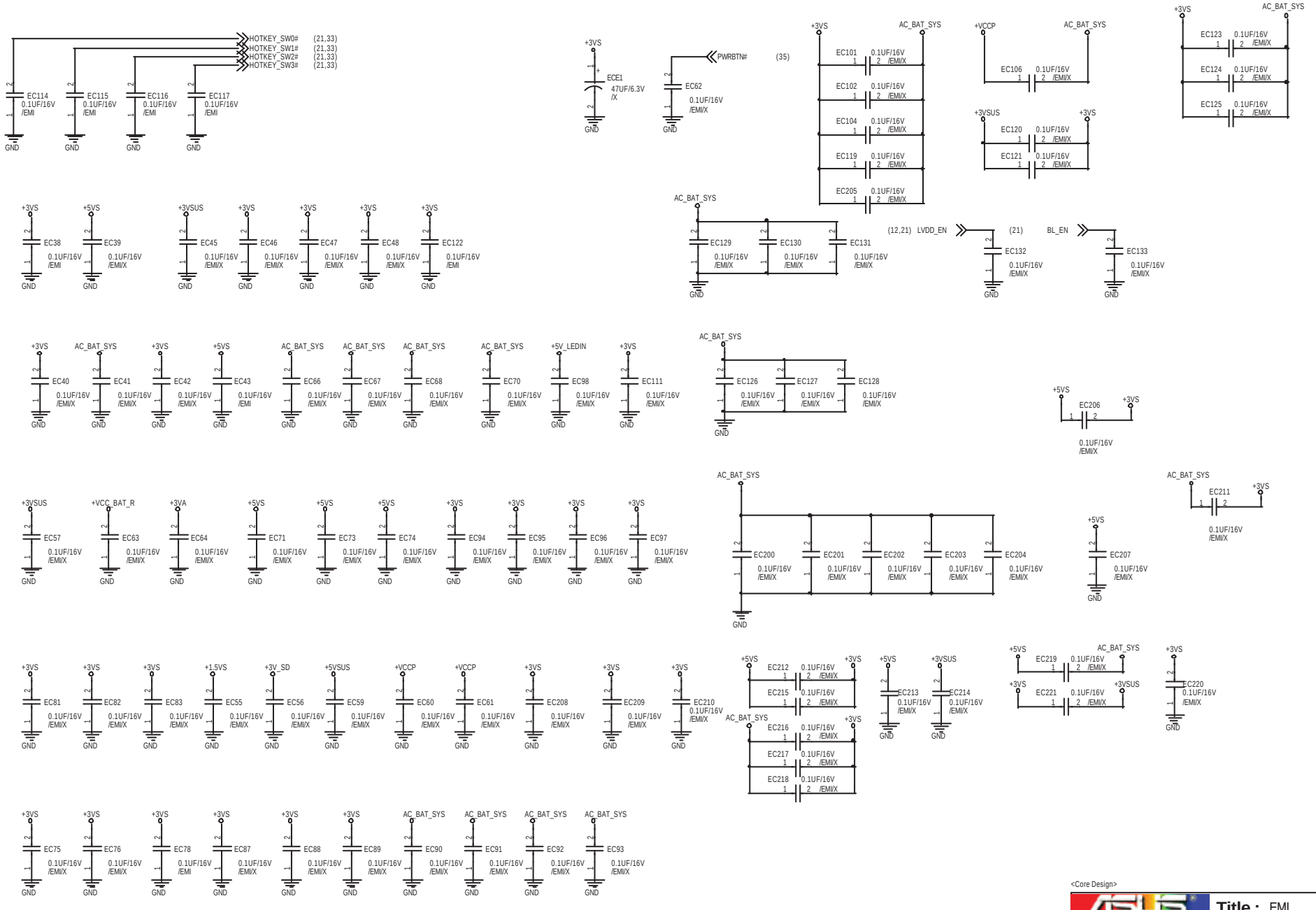
<Core Design>

ASUS Tek Computer INC.	Title : PWR Jack	
	Engineer: *Wayne_Chan*	
Size: A3	Project Name: 904HD	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 40 of 49	



<Core Design>

ASUS	**Title :** Srew Hole	
A S U S Tek Computer INC.	**Engineer:** *Wayne_Chan*	
Size: A3	Project Name: **904HD**	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 41 of 49	



<Core Design>

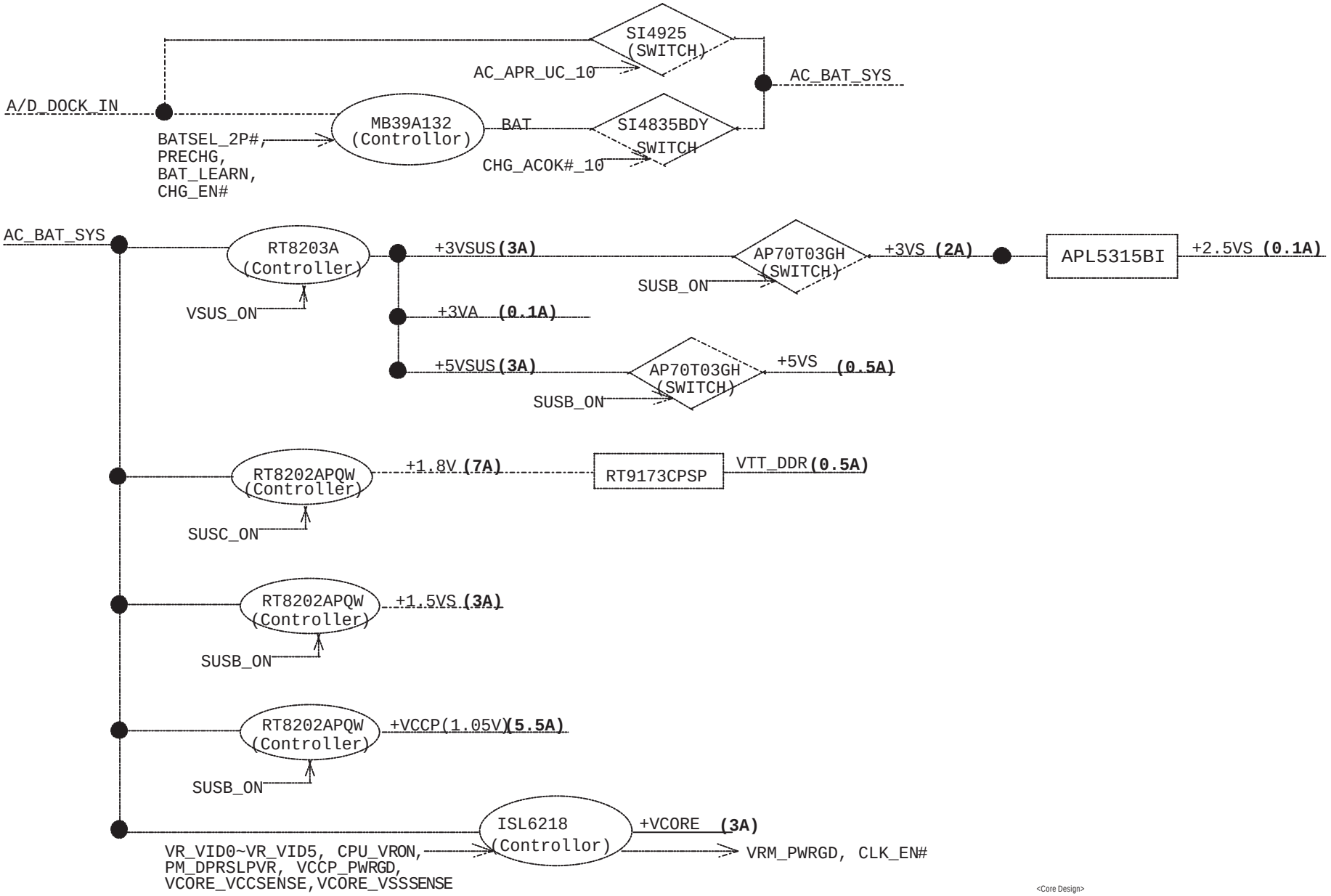
ASUS

Title : EMI

A S U S Tek Computer INC. **Engineer:** *Wayne_Chan*

Size	Project Name	Rev
A3	**904HD**	1.3G

Date: Tuesday, July 01, 2008 Sheet 42 of 49



<Core Design>

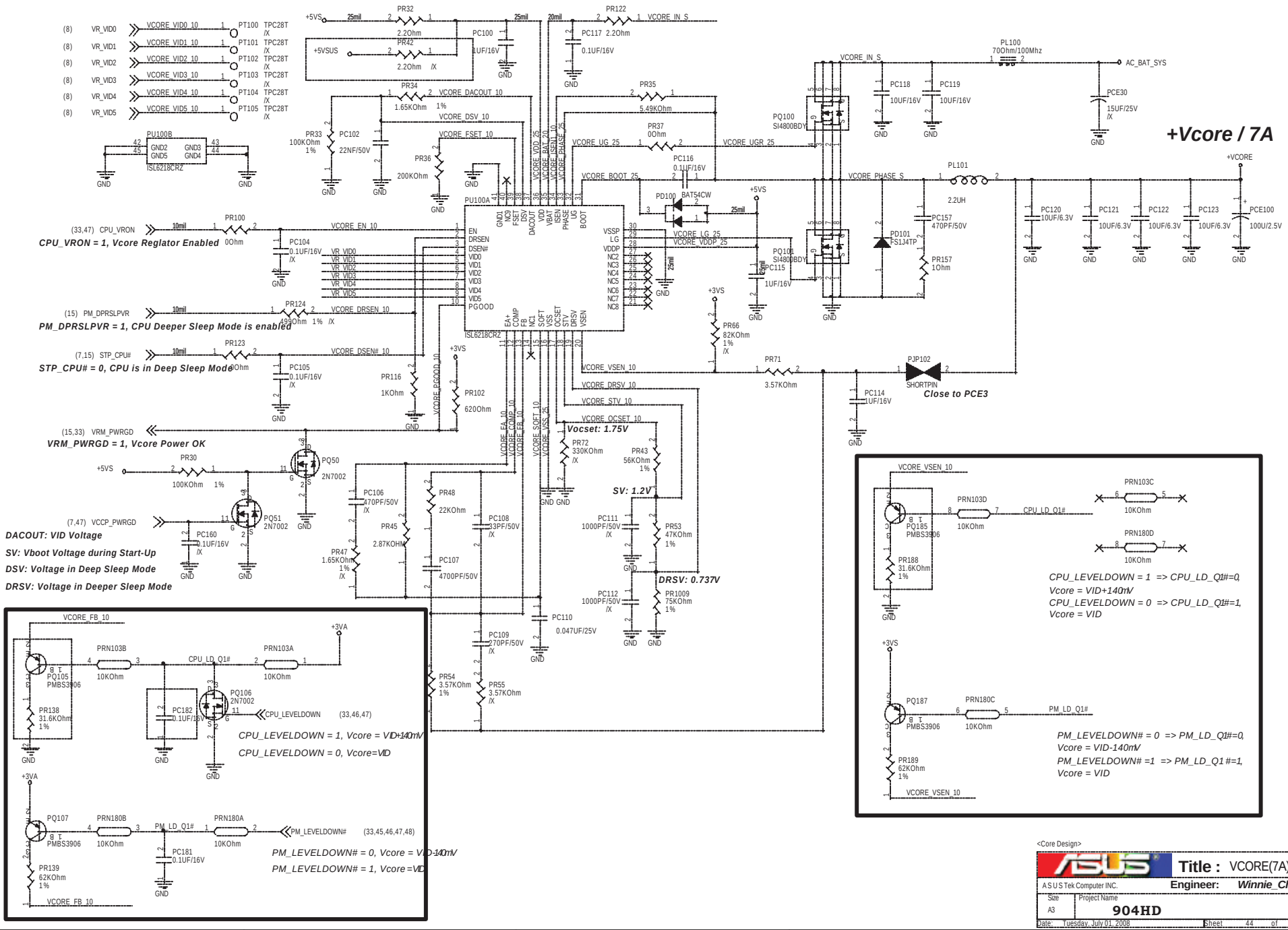
ASUS Tek Computer INC.

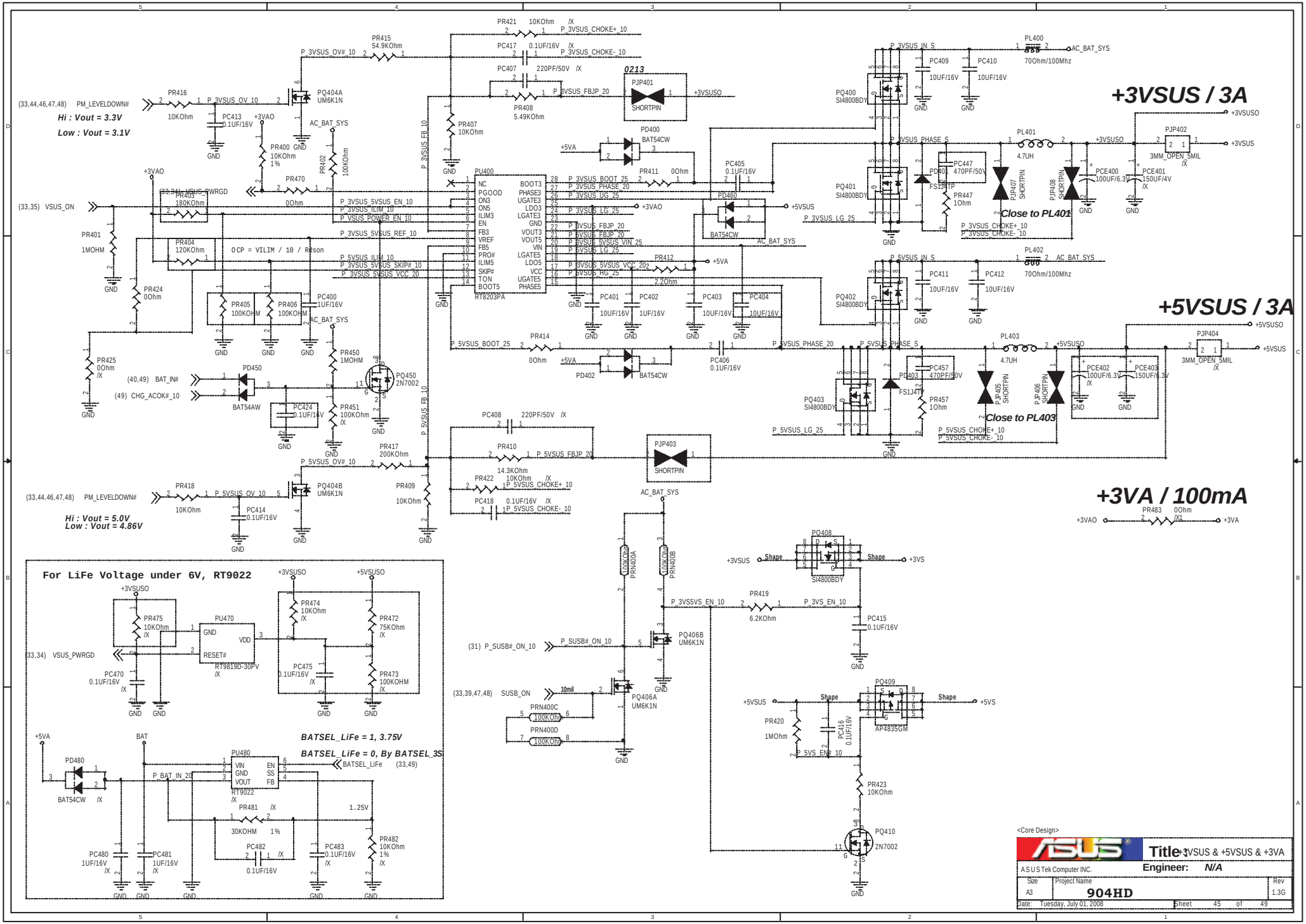
Title : Power Flow

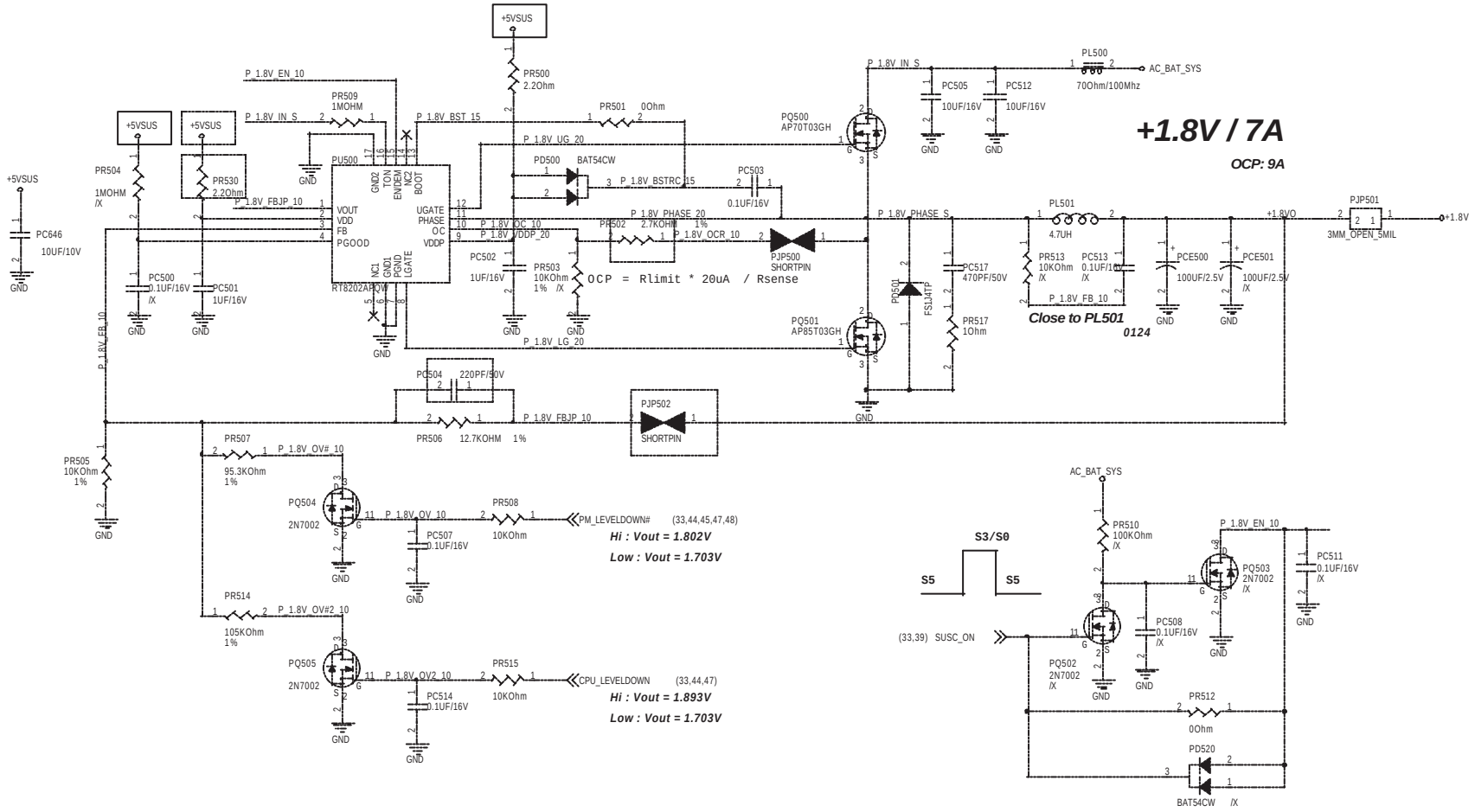
Engineer: Joy_Zhou

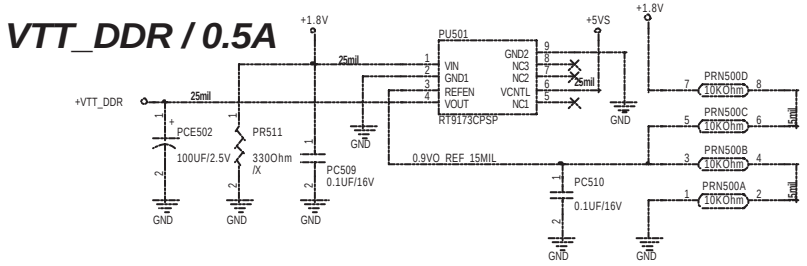
Size	Project Name	Rev
A3	904HD	1.3G

Date: Tuesday, July 01, 2008 Sheet 43 of 49


+Vcore / 7A
CPU_VRON = 1, Vcore Reglator Enabled
PM_DPRSLPVR = 1, CPU Deeper Sleep Mode is enabled
STP_CPU# = 0, CPU is in Deep Sleep Mode
VRM_PWRGD = 1, Vcore Power OK
Vocset: 1.75V
SV: 1.2V
DRSV: 0.737V
Close to PCE3
DACOUT: VID Voltage
SV: Vboot Voltage during Start-Up
DSV: Voltage in Deep Sleep Mode
DRSV: Voltage in Deeper Sleep Mode
CPU_LEVELDOWN = 1, Vcore = VID+140mV
CPU_LEVELDOWN = 0, Vcore=VID
CPU_LEVELDOWN = 1 => CPU_LD_Q1#=0, Vcore = VID+140mV
CPU_LEVELDOWN = 0 => CPU_LD_Q1#=1, Vcore = VID
PM_LEVELDOWN# = 0, Vcore = VID-140mV
PM_LEVELDOWN# = 1, Vcore = VID
PM_LEVELDOWN# = 0 => PM_LD_Q1#=0, Vcore = VID-140mV
PM_LEVELDOWN# =1 => PM_LD_Q1 #=1, Vcore = VID
ISL6218CRZ
PU100A
PU100B
PQ100 SI4800BDY
PQ101 SI4800BDY
PD100 BAT54CW
PD101 FS1J4TP
PQ50 2N7002
PQ51 2N7002
PQ105 PMBS3906
PQ106 2N7002
PQ107 PMBS3906
PQ185 PMBS3906
PQ187 PMBS3906
PJP102 SHORTPIN
PL100 70Ohm/100Mhz
PL101 2.2UH
AC_BAT_SYS
+VCORE
+5VS
+3VS
+3VA
GND
<Core Design>
Title : VCORE(7A)
A S U S Tek Computer INC.
Engineer: Winnie_Chen
Size A3
Project Name 904HD
Rev 1.3G
Date: Tuesday, July 01, 2008
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+3VSUS / 3A
+5VSUS / 3A
+3VA / 100mA
Close to PL401
Close to PL403
Hi : Vout = 3.3V
Low : Vout = 3.1V
Hi : Vout = 5.0V
Low : Vout = 4.86V
For LiFe Voltage under 6V, RT9022
BATSEL_LiFe = 1, 3.75V
BATSEL_LiFe = 0, By BATSEL_3S
PU400 RT8203PA
PU470 RT9819D-30PV
PU480 RT9022
PQ400 SI4800BDY
PQ401 SI4800BDY
PQ402 SI4800BDY
PQ403 SI4800BDY
PQ404A UM6K1N
PQ404B UM6K1N
PQ406A UM6K1N
PQ406B UM6K1N
PQ408 SI4800BDY
PQ409 AP4835GM
PQ410 2N7002
PQ450 2N7002
PJP401 SHORTPIN
PJP402 3MM_OPEN_5MIL
PJP403 SHORTPIN
PJP404 3MM_OPEN_5MIL
PL400 70Ohm/100Mhz
PL401 4.7UH
PL402 70Ohm/100Mhz
PL403 4.7UH
PD400 BAT54CW
PD401 FSJ3JTP
PD402 BAT54CW
PD403 FSJ4JTP
PD450 BAT54AW
PD460 BAT54CW
PD480 BAT54CW
PJP407 SHORTPIN
PJP408 SHORTPIN
PJP405 SHORTPIN
PJP406 SHORTPIN
PRN400A 100KOhm
PRN400B 100KOhm
PRN400C 100KOhm
PRN400D 100KOhm
AC_BAT_SYS
P_3VSUS_IN_S
P_3VSUS_PHASE_S
P_5VSUS_IN_S
P_5VSUS_PHASE_S
P_3VSUS_BOOT_25
P_3VSUS_PHASE_20
P_3VSUS_UG_25
P_3VSUS_LG_25
P_3VSUS_FBJP_20
P_3VSUS_5VSUS_VIN_25
P_3VSUS_5VSUS_VCC_20
P_3VSUS_5VSUS_REF_10
P_3VSUS_5VSUS_EN_10
P_3VSUS_ILIM_10
P_3VSUS_POWER_EN_10
P_3VSUS_CHOKE+_10
P_3VSUS_CHOKE-_10
P_5VSUS_BOOT_25
P_5VSUS_PHASE_20
P_5VSUS_LG_25
P_5VSUS_FBJP_20
P_5VSUS_CHOKE+_10
P_5VSUS_CHOKE-_10
P_3VS5VS_EN_10
P_3VS_EN_10
P_5VS_EN_10
P_BAT_IN_20
BATSEL_LiFe (33,49)
(33,44,46,47,48) PM_LEVELDOWN#
(33,34) VSUS_PWRGD
(33,35) VSUS_ON
(40,49) BAT_IN#
(49) CHG_ACOK#_10
(31) P_SUSB#_ON_10
(33,39,47,48) SUSB_ON
OCP = VILIM / 10 / Rsnon
0213
<Core Design>
Title: +3VSUS & +5VSUS & +3VA
ASUS Tek Computer INC.
Engineer: N/A
Size: A3
Project Name: 904HD
Rev: 1.3G
Date: Tuesday, July 01, 2008
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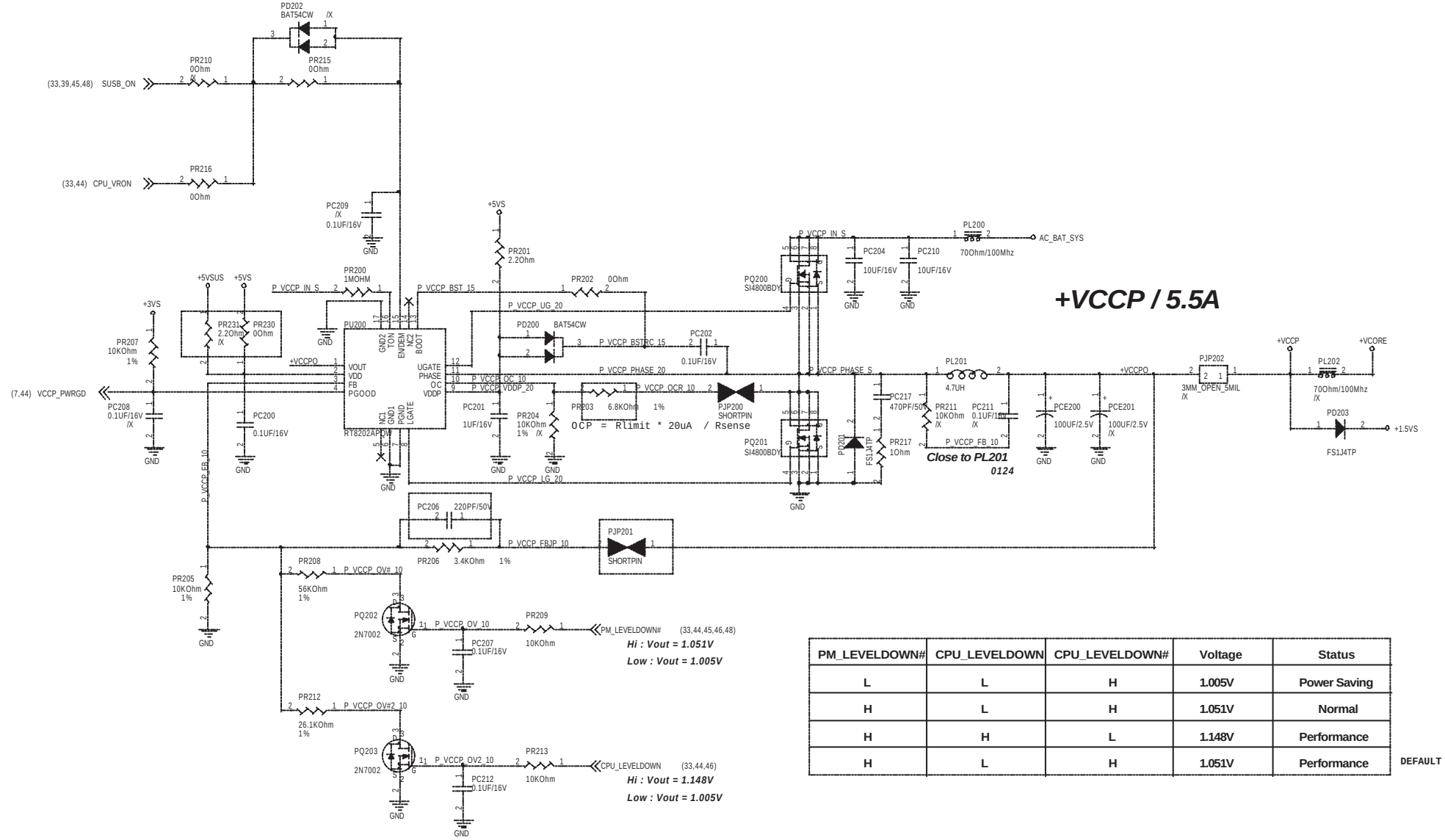




PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status	
L	L	H	1.703V	Power Saving	
H	L	H	1.802V	Normal	
H	H	L	1.893V	Performance	
H	L	H	1.802V	Performance	DEFAULT

<Core Design>

ASUSTek Computer INC.	Title : +1.8V & VTTDDR	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 904HD	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 46 of 49	



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status	
L	L	H	1.005V	Power Saving	
H	L	H	1.051V	Normal	
H	H	L	1.148V	Performance	
H	L	H	1.051V	Performance	DEFAULT

<Core Design>

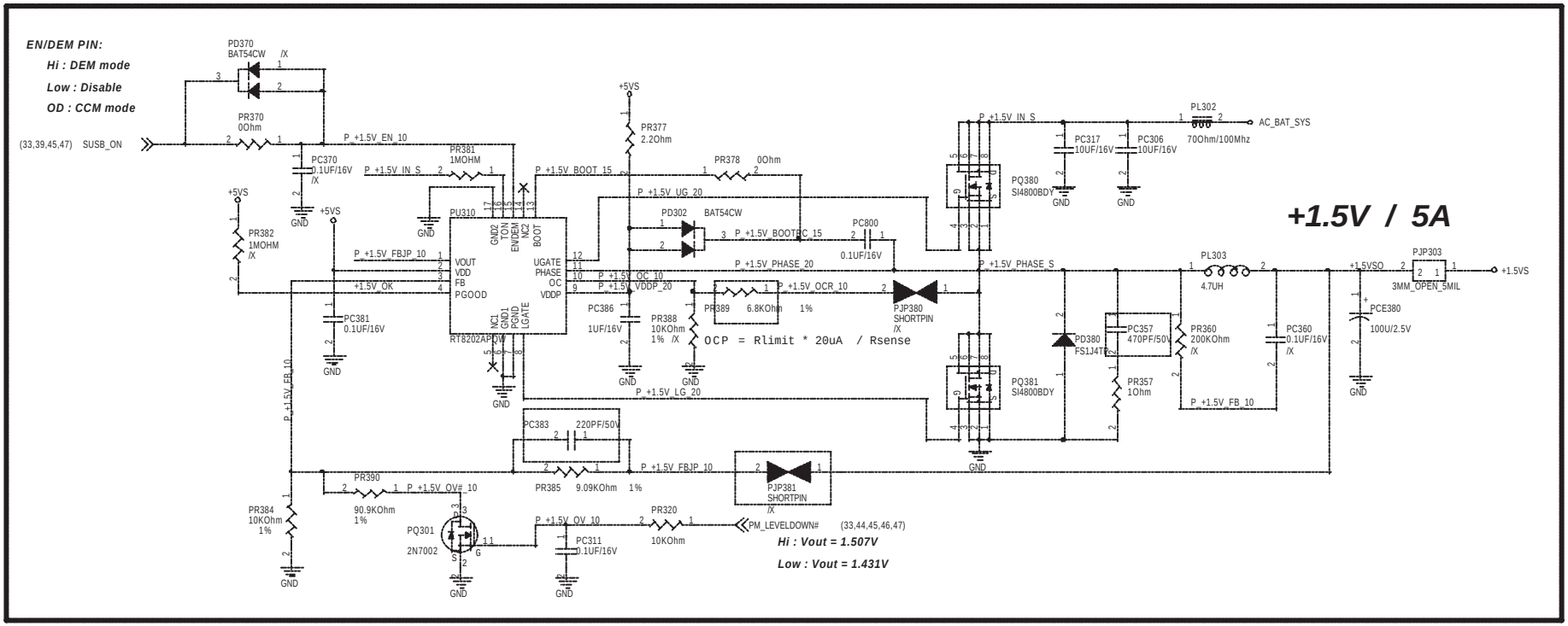
ASUSTek Computer INC.

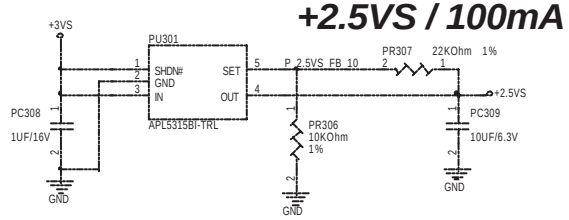
Title : VCCP

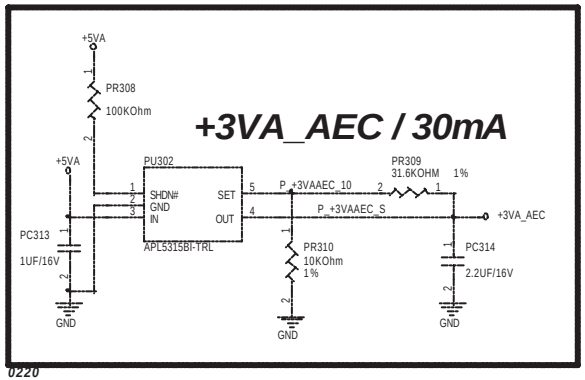
Engineer: Joy_Zhou

Size	Project Name	Rev
A3	904HD	1.3G

Date: Tuesday, July 01, 2008 Sheet 47 of 49



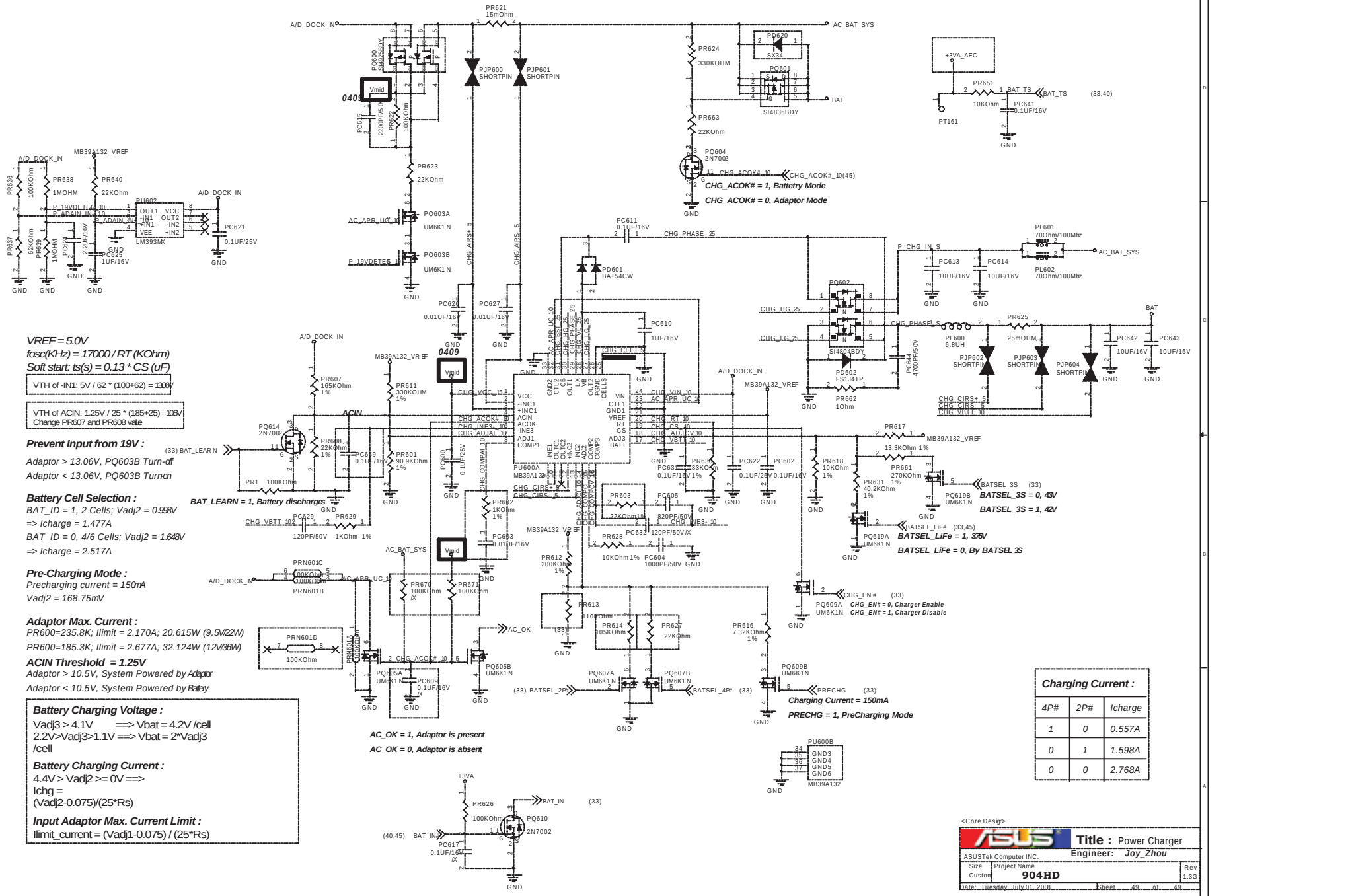




0220

<Core Design>

ASUS Tek Computer INC.	Title : +1.5VS & +2.5VS	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 904HD	Rev: 1.3G
Date: Tuesday, July 01, 2008	Sheet 48 of 49	


VREF = 5.0V
fosc(KHz) = 17000 / RT (KOhm)
Soft start: ts(s) = 0.13 * CS (uF)
VTH of -IN1: 5V / 62 * (100+62) = 1.308V
VTH of ACIN: 1.25V / 25 * (185+25) = 10.5V
Change PR607 and PR608 value
Prevent Input from 19V :
Adaptor > 13.06V, PQ603B Turn-off
Adaptor < 13.06V, PQ603B Turn-on
Battery Cell Selection :
BAT_ID = 1, 2 Cells; Vadj2 = 0.998V
=> Icharge = 1.477A
BAT_ID = 0, 4/6 Cells; Vadj2 = 1.648V
=> Icharge = 2.517A
Pre-Charging Mode :
Precharging current = 150mA
Vadj2 = 168.75mV
Adaptor Max. Current :
PR600=235.8K; Ilimit = 2.170A; 20.615W (9.5V/22W)
PR600=185.3K; Ilimit = 2.677A; 32.124W (12V/36W)
ACIN Threshold = 1.25V
Adaptor > 10.5V, System Powered by Adaptor
Adaptor < 10.5V, System Powered by Battery
Battery Charging Voltage :
Vadj3 > 4.1V ==> Vbat = 4.2V /cell
2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell
Battery Charging Current :
4.4V > Vadj2 >= 0V ==>
Ichg =
(Vadj2-0.075)/(25*Rs)
Input Adaptor Max. Current Limit :
Ilimit_current = (Vadj1-0.075) / (25*Rs)
A/D_DOCK_IN
AC_BAT_SYS
BAT
MB39A132_VREF
ACIN
BAT_LEARN = 1, Battery discharges
CHG_ACOK# = 1, Battery Mode
CHG_ACOK# = 0, Adaptor Mode
AC_OK = 1, Adaptor is present
AC_OK = 0, Adaptor is absent
BATSEL_3S = 0, 4S
BATSEL_3S = 1, 2S
BATSEL_LiFe = 1, 3S
BATSEL_LiFe = 0, By BATSEL_3S
CHG_EN# = 0, Charger Enable
CHG_EN# = 1, Charger Disable
Charging Current = 150mA
PRECHG = 1, PreCharging Mode
Charging Current :
4P# 2P# Icharge
1 0 0.557A
0 1 1.598A
0 0 2.768A
Title : Power Charger
Engineer: Joy_Zhou
ASUSTek Computer INC.
Size Custom
Project Name 904HD
Rev 1.3G
Date: Tuesday, July 01, 2008
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