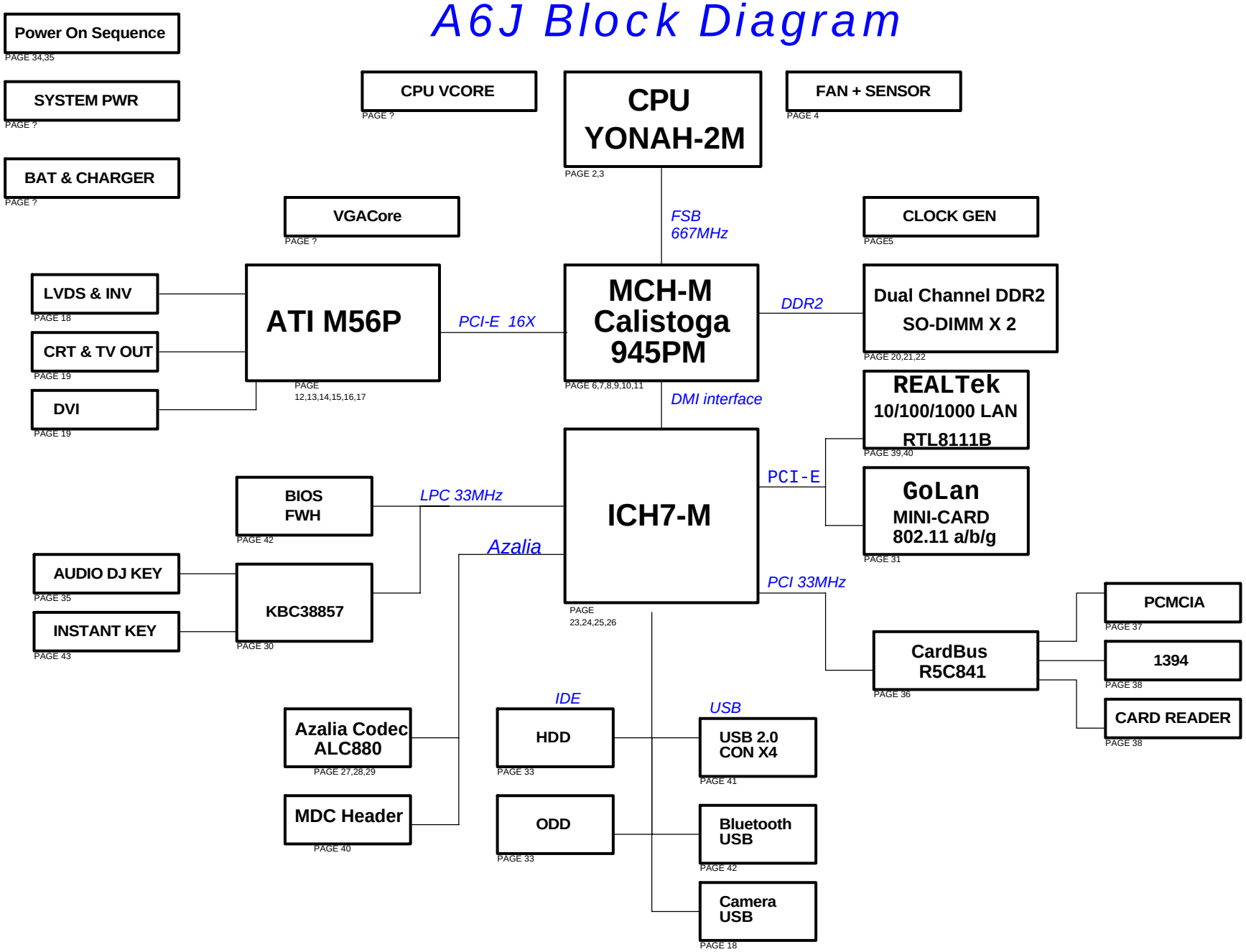
A6J Block Diagram



<Variant Name>

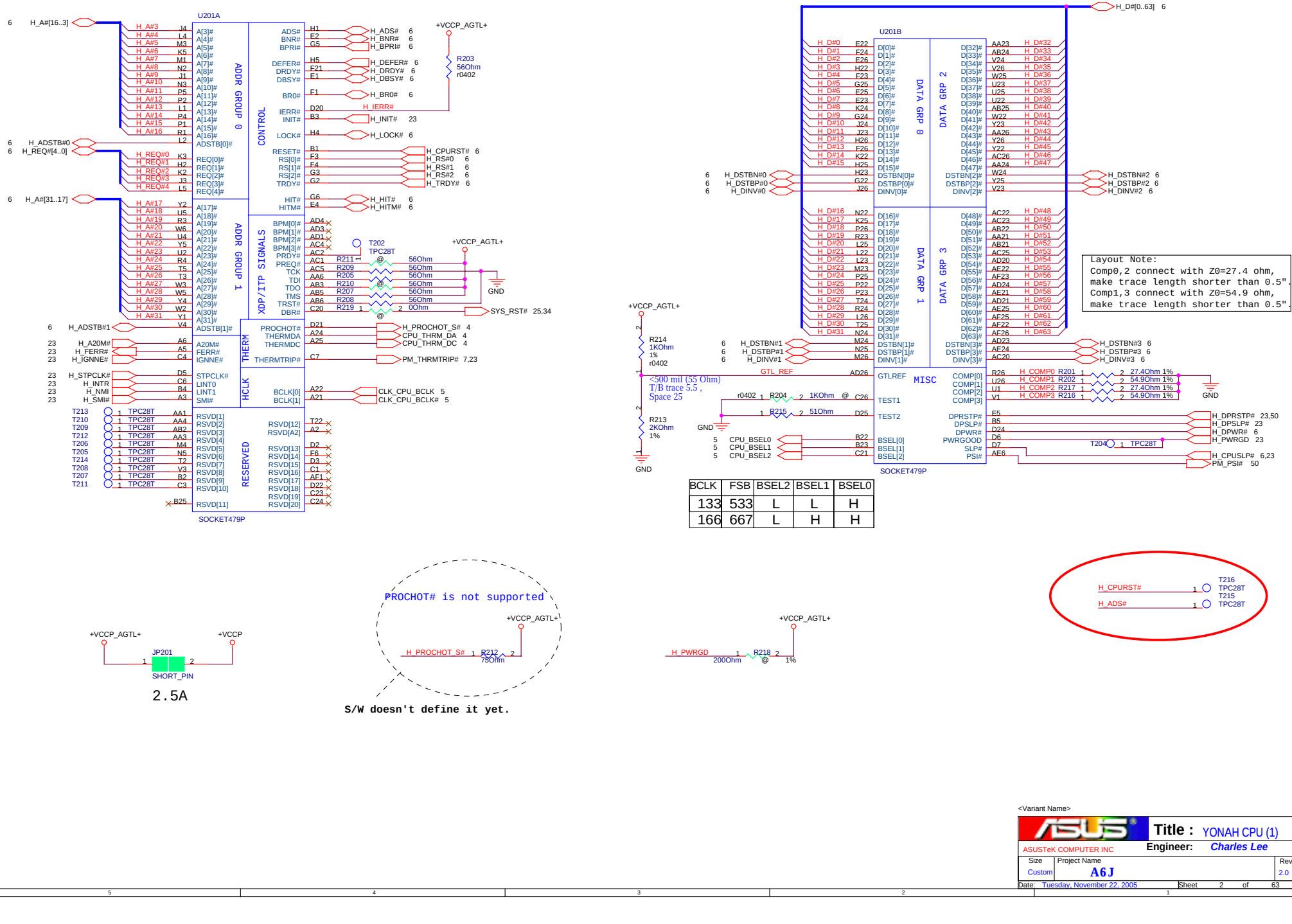
Title : BLOCK DIAGRAM

Engineer: Marco Chen

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 1 of 63



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

<Variant Name>

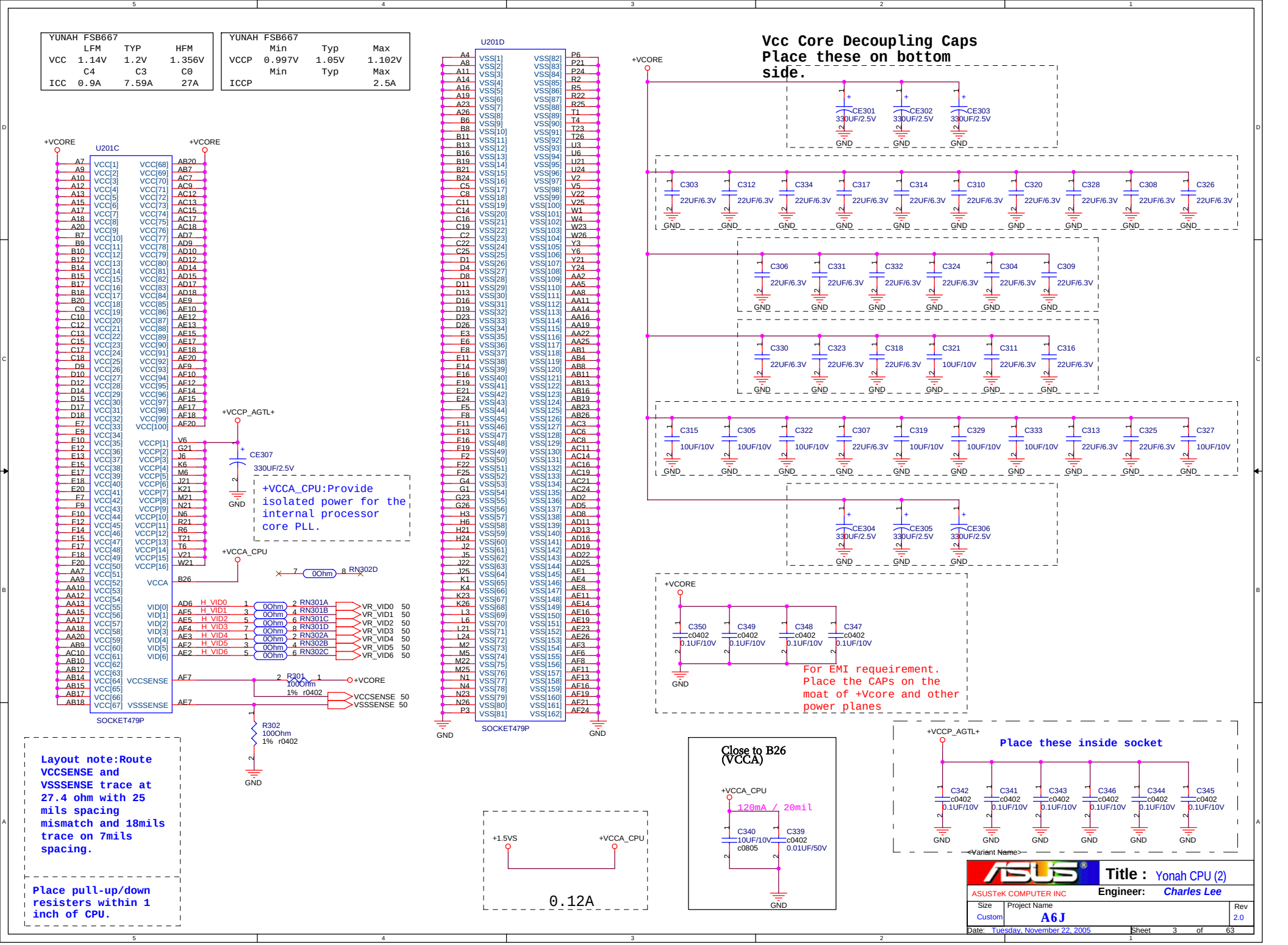
ASUSTeK COMPUTER INC

Title : YONAH CPU (1)

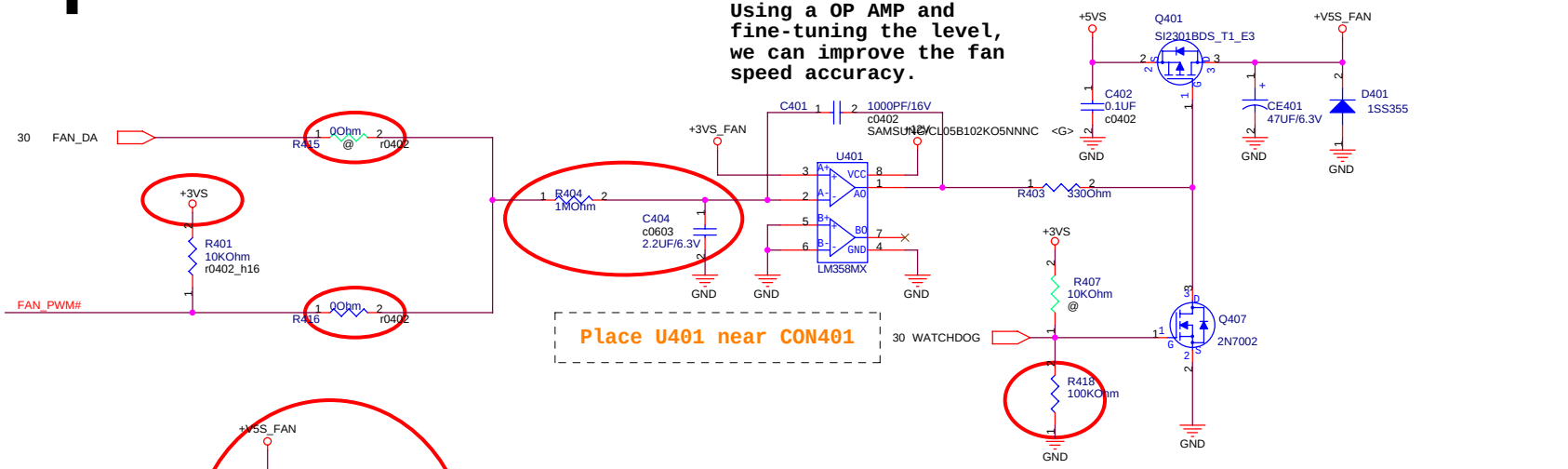
Engineer: Charles Lee

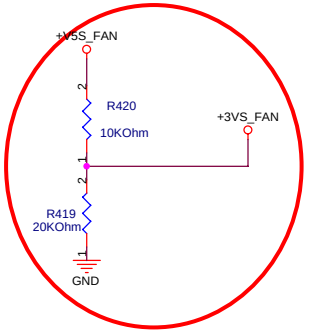
Size	Project Name	Rev
Custom	A6J	2.0

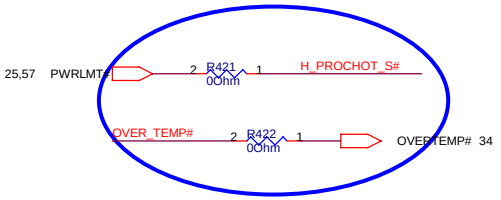
Date: Tuesday, November 22, 2005 Sheet 2 of 63


YUNAH FSB667
LFM TYP HFM
VCC 1.14V 1.2V 1.356V
C4 C3 C0
ICC 0.9A 7.59A 27A
YUNAH FSB667
Min Typ Max
VCCP 0.997V 1.05V 1.102V
Min Typ Max
ICCP 2.5A
Vcc Core Decoupling Caps
Place these on bottom side.
U201C
SOCKET479P
U201D
SOCKET479P
+VCORE
+VCCP_AGTL+
+VCCA_CPU
+VCCA_CPU:Provide isolated power for the internal processor core PLL.
For EMI requeirement. Place the CAPs on the moat of +Vcore and other power planes
Place these inside socket
Close to B26 (VCCA)
120mA / 20mil
+1.5VS
0.12A
Layout note:Route VCCSENSE and VSSSENSE trace at 27.4 ohm with 25 mils spacing mismatch and 18mils trace on 7mils spacing.
Place pull-up/down resisters within 1 inch of CPU.
Title : Yonah CPU (2)
ASUSTeK COMPUTER INC
Engineer: Charles Lee
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 3 of 63

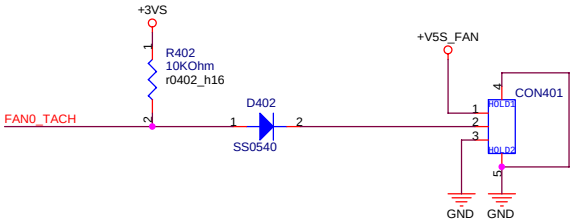
Fan Speed Control

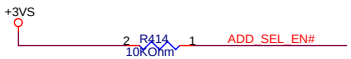


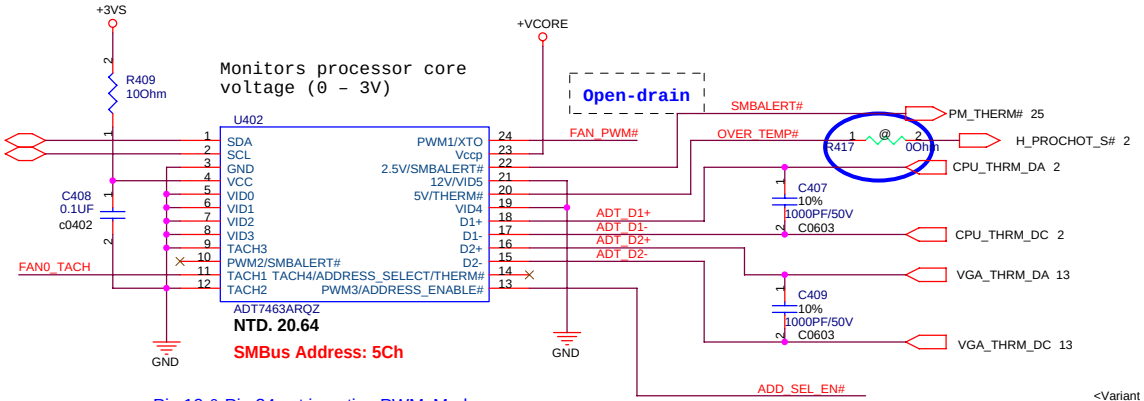




CPU FAN







Pin 10 & Pin 24 set inverting PWM Mode
Set INV=1 to invert PWM output

Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

<Variant Name>

ASUSTeK COMPUTER INC

Title : THER-SENSOR,FAN

Engineer: *Marco Chen*

Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 4 of 63

Place termination closed to source IC

	FSLC	FSLB	FSLA
Bclk / FSB	BSEL2	BSEL1	BSEL0
133 / 533	L	L	H
166 / 667	L	H	H

SMBus Slave Address:D2H

U501

ICS954310BGLFT

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD1(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#)	CLK_MCH_3GPLL(#)

<Variant Name>

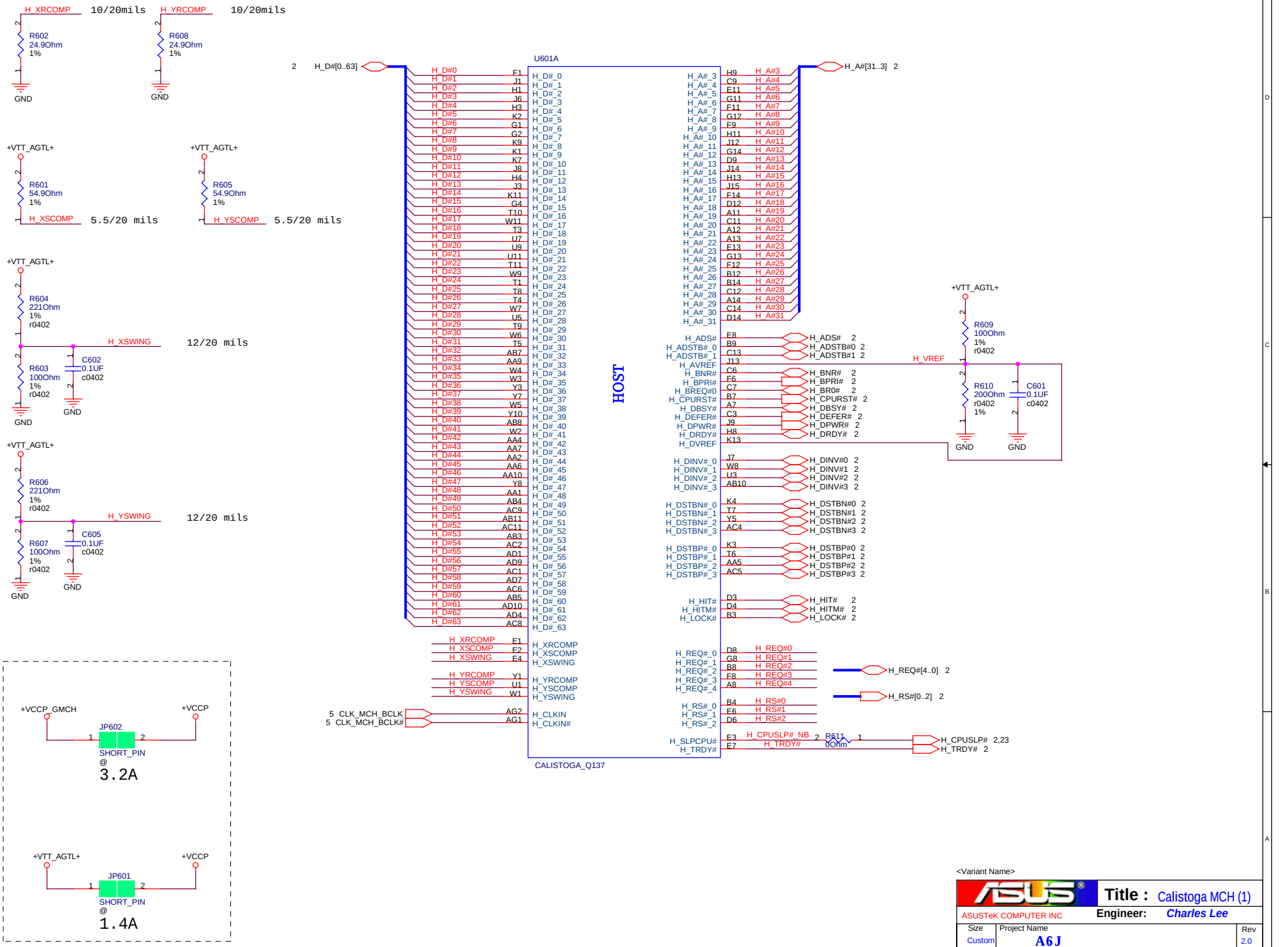
Title : CLOCK GEN

ASUSTeK COMPUTER INC

Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 5 of 63



<Variant Name>

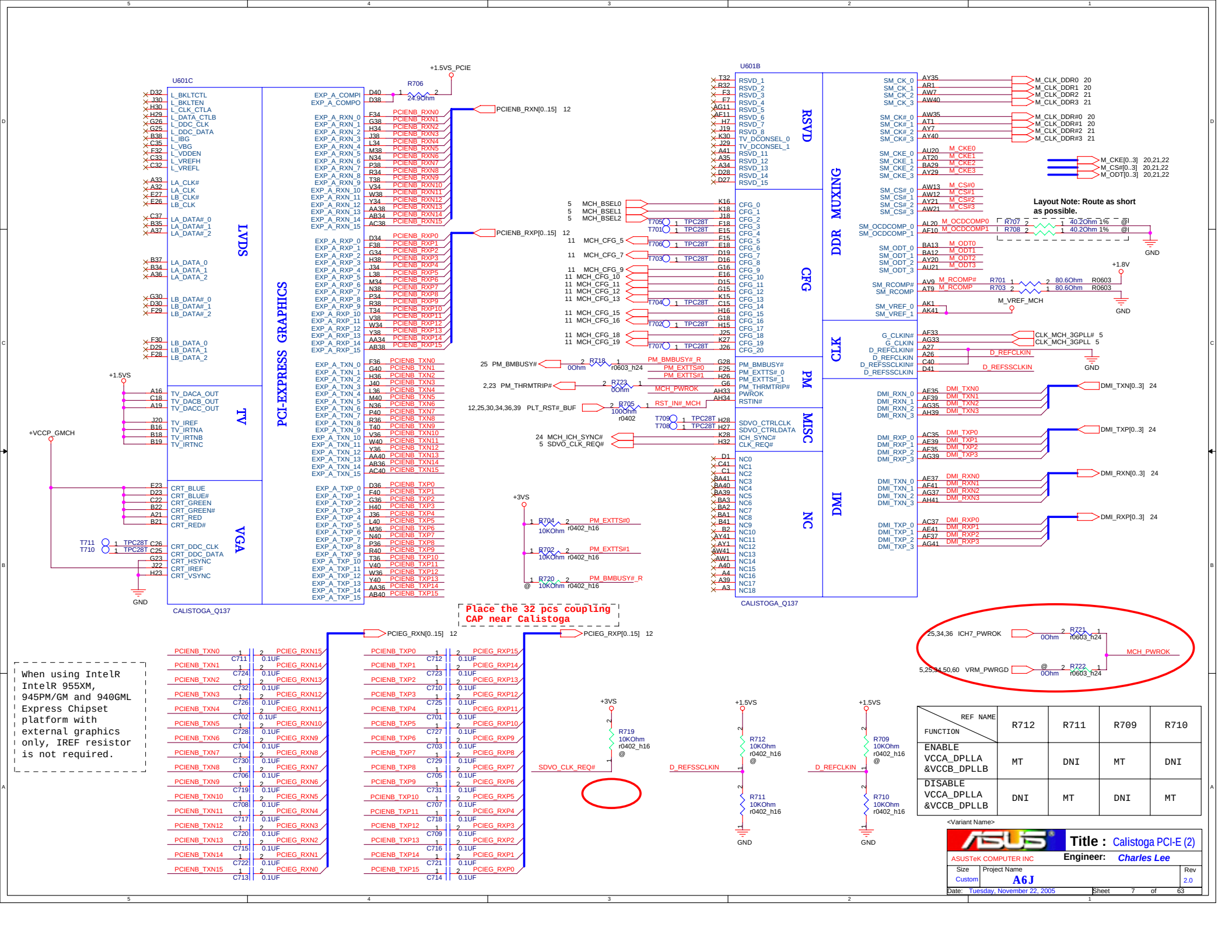
ASUSTeK COMPUTER INC

Title : Calistoga MCH (1)

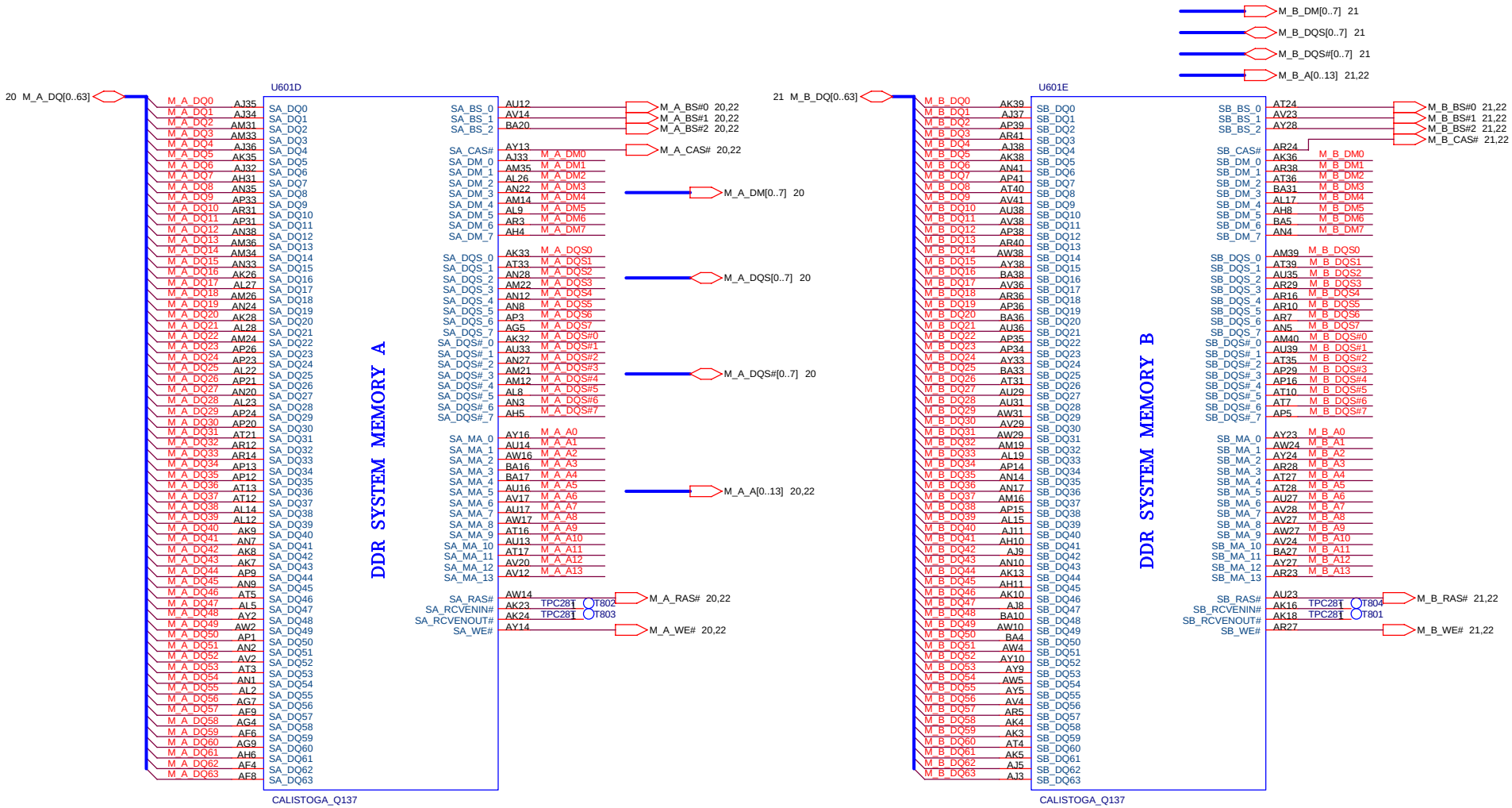
Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 6 of 63



FUNCTION \ REF NAME	R712	R711	R709	R710
ENABLE VCCA_DPLLA &VCCB_DPLLB	MT	DNI	MT	DNI
DISABLE VCCA_DPLLA &VCCB_DPLLB	DNI	MT	DNI	MT



<Variant Name>

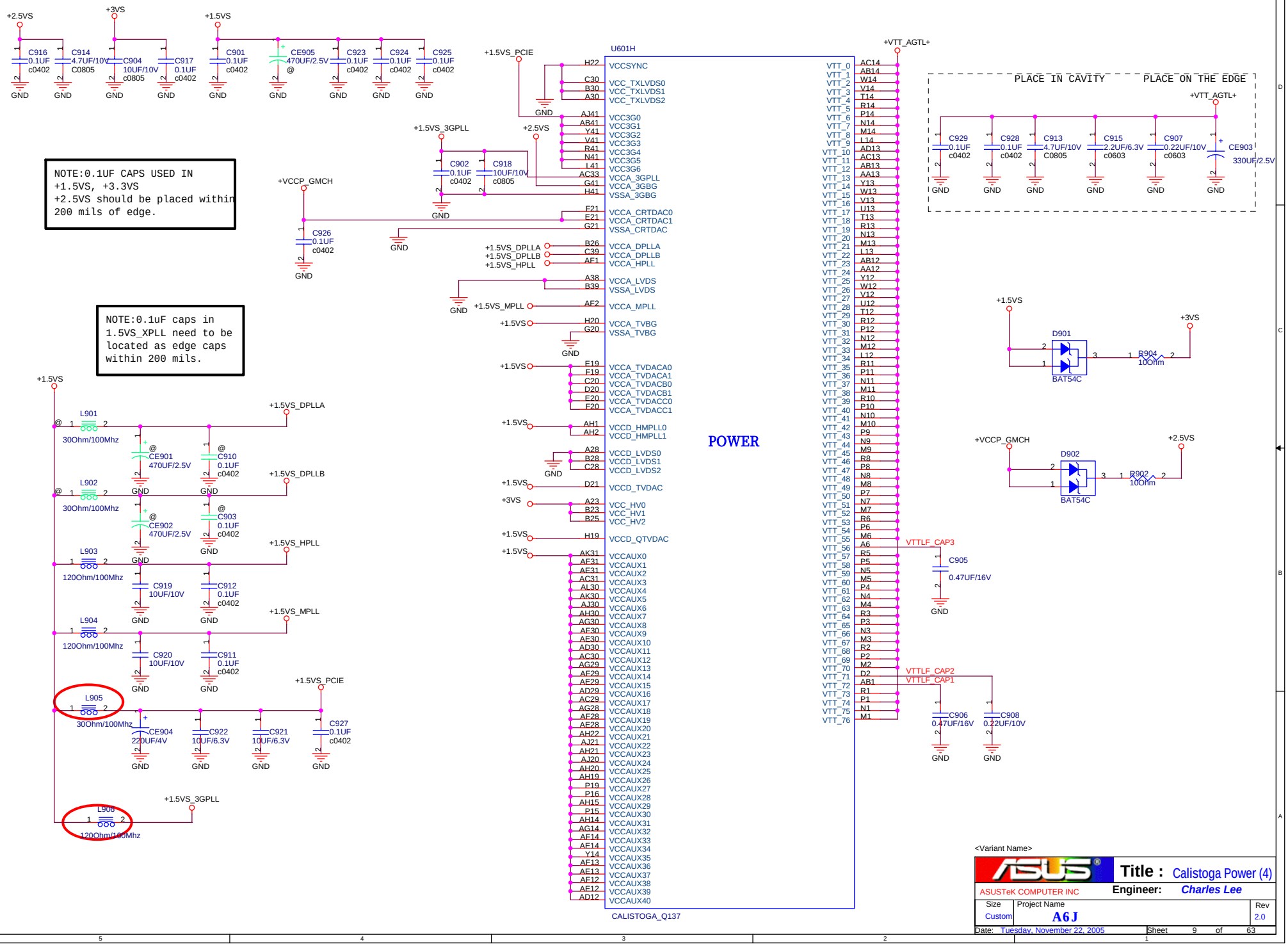
ASUSTeK COMPUTER INC

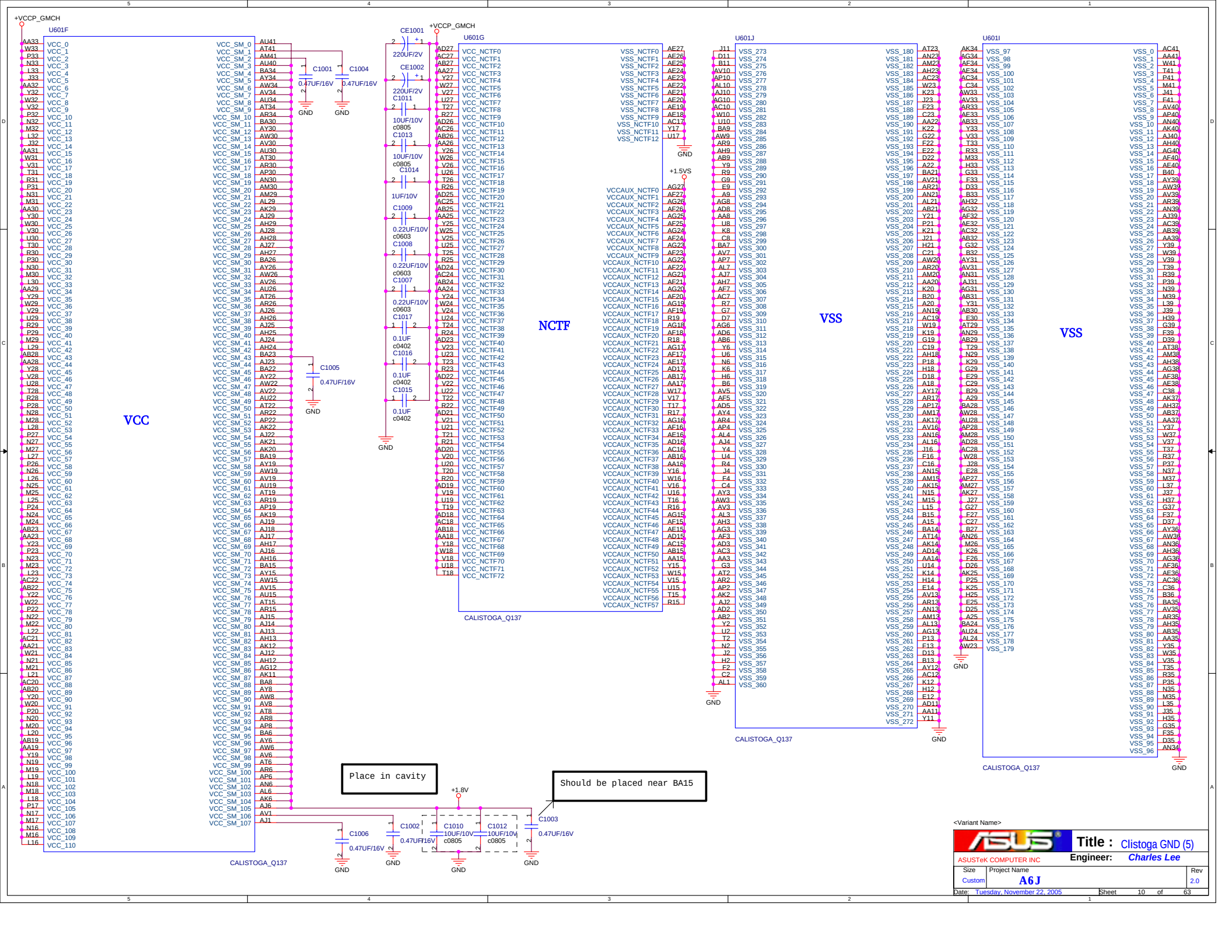
Title : Calistoga DDR2 (3)

Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 8 of 63

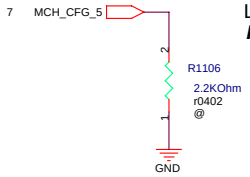

NOTE:0.1UF CAPS USED IN
+1.5VS, +3.3VS
+2.5VS should be placed within
200 mils of edge.
NOTE:0.1uF caps in
1.5VS_XPLL need to be
located as edge caps
within 200 mils.
U601H
POWER
CALISTOGA_Q137
PLACE IN CAVITY
PLACE ON THE EDGE
+2.5VS
+3VS
+1.5VS
+1.5VS_PCIE
+1.5VS_3GPLL
+VCCP_GMCH
+VTT_AGTL+
+1.5VS_DPLLA
+1.5VS_DPLLB
+1.5VS_HPLL
+1.5VS_MPLL
VTTLF_CAP3
VTTLF_CAP2
VTTLF_CAP1
D901
D902
BAT54C
R904
R902
10Ohm
C916 0.1UF c0402
C914 4.7UF/10V C0805
C904 10UF/10V c0805
C917 0.1UF c0402
C901 0.1UF c0402
CE905 470UF/2.5V
C923 0.1UF c0402
C924 0.1UF c0402
C925 0.1UF c0402
C902 0.1UF c0402
C918 10UF/10V c0805
C926 0.1UF c0402
C929 0.1UF c0402
C928 0.1UF c0402
C913 4.7UF/10V C0805
C915 2.2UF/6.3V c0603
C907 0.22UF/10V c0603
CE903 330UF/2.5V
L901 30Ohm/100Mhz
L902 30Ohm/100Mhz
L903 120Ohm/100Mhz
L904 120Ohm/100Mhz
L905 30Ohm/100Mhz
L906 120Ohm/100Mhz
CE901 470UF/2.5V
CE902 470UF/2.5V
CE904 220UF/4V
C910 0.1UF c0402
C903 0.1UF c0402
C919 10UF/10V
C912 0.1UF c0402
C920 10UF/10V
C911 0.1UF c0402
C922 10UF/6.3V
C921 10UF/6.3V
C927 0.1UF c0402
C905 0.47UF/16V
C906 0.47UF/16V
C908 0.22UF/10V
GND
H22 VCCSYNC
C30 VCC_TXLVDS0
B30 VCC_TXLVDS1
A30 VCC_TXLVDS2
AJ41 VCC3G0
AB41 VCC3G1
Y41 VCC3G2
V41 VCC3G3
R41 VCC3G4
N41 VCC3G5
L41 VCC3G6
AC33 VCCA_3GPLL
G41 VCCA_3GBG
H41 VSSA_3GBG
F21 VCCA_CRTDAC0
E21 VCCA_CRTDAC1
G21 VSSA_CRTDAC
B26 VCCA_DPLLA
C39 VCCA_DPLLB
AF1 VCCA_HPLL
A38 VCCA_LVDS
B39 VSSA_LVDS
AF2 VCCA_MPLL
H20 VCCA_TVBG
G20 VSSA_TVBG
E19 VCCA_TVDACA0
F19 VCCA_TVDACA1
C20 VCCA_TVDACB0
D20 VCCA_TVDACB1
E20 VCCA_TVDACC0
F20 VCCA_TVDACC1
AH1 VCCD_HMPLL0
AH2 VCCD_HMPLL1
A28 VCCD_LVDS0
B28 VCCD_LVDS1
C28 VCCD_LVDS2
D21 VCCD_TVDAC
A23 VCC_HV0
B23 VCC_HV1
B25 VCC_HV2
H19 VCCD_QTVDAC
AK31 VCCAUX0
AF31 VCCAUX1
AE31 VCCAUX2
AC31 VCCAUX3
AL30 VCCAUX4
AK30 VCCAUX5
AJ30 VCCAUX6
AH30 VCCAUX7
AG30 VCCAUX8
AF30 VCCAUX9
AE30 VCCAUX10
AD30 VCCAUX11
AC30 VCCAUX12
AG29 VCCAUX13
AF29 VCCAUX14
AE29 VCCAUX15
AD29 VCCAUX16
AC29 VCCAUX17
AG28 VCCAUX18
AF28 VCCAUX19
AE28 VCCAUX20
AH22 VCCAUX21
AJ21 VCCAUX22
AH21 VCCAUX23
AJ20 VCCAUX24
AH20 VCCAUX25
AH19 VCCAUX26
P19 VCCAUX27
P16 VCCAUX28
AH15 VCCAUX29
P15 VCCAUX30
AH14 VCCAUX31
AG14 VCCAUX32
AF14 VCCAUX33
AE14 VCCAUX34
Y14 VCCAUX35
AF13 VCCAUX36
AE13 VCCAUX37
AF12 VCCAUX38
AE12 VCCAUX39
AD12 VCCAUX40
VTT_0 AC14
VTT_1 AB14
VTT_2 W14
VTT_3 V14
VTT_4 T14
VTT_5 R14
VTT_6 P14
VTT_7 N14
VTT_8 M14
VTT_9 L14
VTT_10 AD13
VTT_11 AC13
VTT_12 AB13
VTT_13 AA13
VTT_14 Y13
VTT_15 W13
VTT_16 V13
VTT_17 U13
VTT_18 T13
VTT_19 R13
VTT_20 N13
VTT_21 M13
VTT_22 L13
VTT_23 AB12
VTT_24 AA12
VTT_25 Y12
VTT_26 W12
VTT_27 V12
VTT_28 U12
VTT_29 T12
VTT_30 R12
VTT_31 P12
VTT_32 N12
VTT_33 M12
VTT_34 L12
VTT_35 R11
VTT_36 P11
VTT_37 N11
VTT_38 M11
VTT_39 R10
VTT_40 P10
VTT_41 N10
VTT_42 M10
VTT_43 P9
VTT_44 N9
VTT_45 M9
VTT_46 R8
VTT_47 P8
VTT_48 N8
VTT_49 M8
VTT_50 P7
VTT_51 N7
VTT_52 M7
VTT_53 R6
VTT_54 P6
VTT_55 M6
VTT_56 A6
VTT_57 R5
VTT_58 P5
VTT_59 N5
VTT_60 M5
VTT_61 P4
VTT_62 N4
VTT_63 M4
VTT_64 R3
VTT_65 P3
VTT_66 N3
VTT_67 M3
VTT_68 R2
VTT_69 P2
VTT_70 M2
VTT_71 D2
VTT_72 AB1
VTT_73 R1
VTT_74 P1
VTT_75 N1
VTT_76 M1
<Variant Name>
Title : Calistoga Power (4)
ASUSTeK COMPUTER INC
Engineer: Charles Lee
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 9 of 63


+VCCP_GMCH
U601F
VCC
CALISTOGA_Q137
U601G
NCTF
CALISTOGA_Q137
U601J
VSS
CALISTOGA_Q137
U601I
VSS
CALISTOGA_Q137
+1.5VS
+1.8V
GND
C1001
C1004
C1005
C1006
C1002
C1010
C1012
C1003
0.47UF/16V
CE1001
CE1002
220UF/2V
C1011
C1013
C1014
C1009
C1008
C1007
C1017
C1016
C1015
10UF/10V
c0805
1UF/10V
0.22UF/10V
c0603
0.1UF
c0402
Place in cavity
Should be placed near BA15
<Variant Name>
Title : Clistoga GND (5)
ASUSTeK COMPUTER INC
Engineer: Charles Lee
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 10 of 63

CFG[17..3] have internal pullup resistors.
CFG[20..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

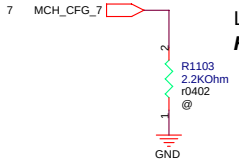
CFG5 : DMI STRAP

LOW = DMI X 2
HIGH = DMI X 4 (Default)



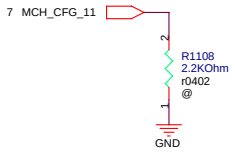
CFG7 : CPU STRAP

LOW = Mobile Prescott
HIGH = Dothan CPU (Default)



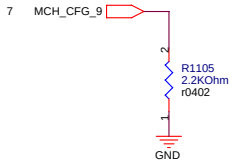
CFG11 : PSB 4X CLK ENABLE

LOW = REVERSAL
HIGH =Calistoga(Default)



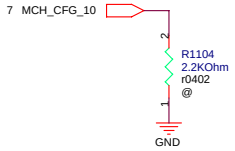
CFG9 : PCIE GRAPHIC LANE

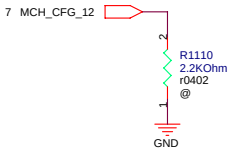
LOW = REVERSE LANE (Default)
HIGH = NORMAL OPERATION

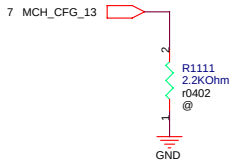


CFG10: HOST PLL VCO SELECT

LOW = RESERVED
HIGH = MOBILITY

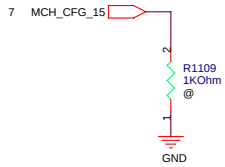






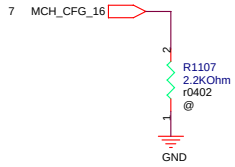
CFG15 :ICH RESET DISABLE

LOW = ICH RESET DISABLE
HIGH = NORMAL OPERATION



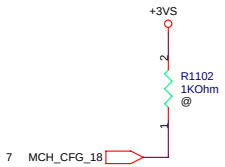
CFG16 : FSB DYNAMIC ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



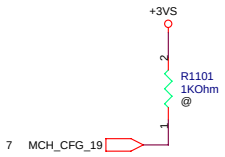
CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)
HIGH = 1.5V



CFG19 : DMI LANE REVERSAL

LOW = NORMAL
HIGH = LANES REVERSED



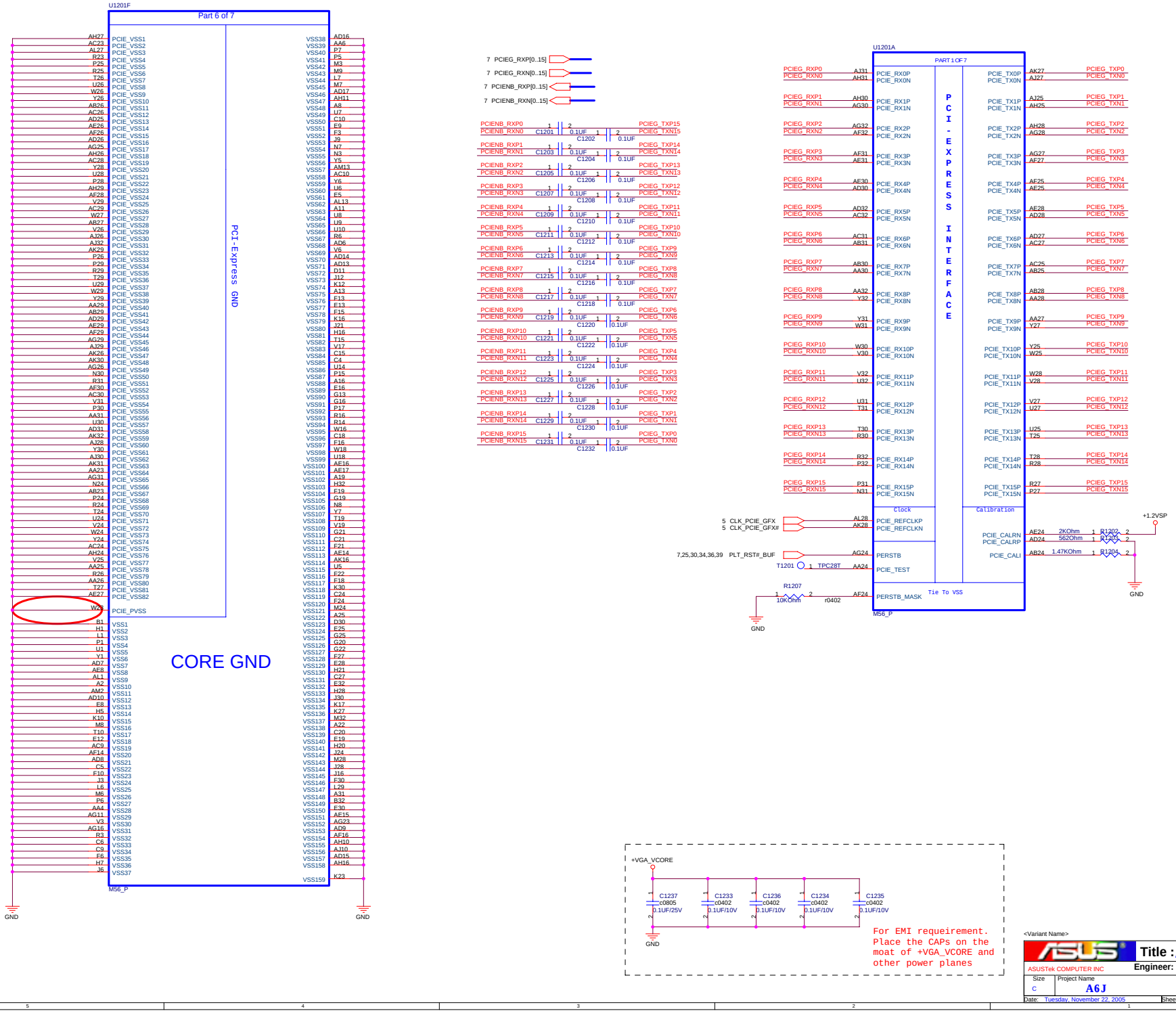
<Variant Name>

Title : Calistoga Strapping

ASUSTeK COMPUTER INC Engineer: *Charles Lee*

Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 11 of 63



<Variant Name>

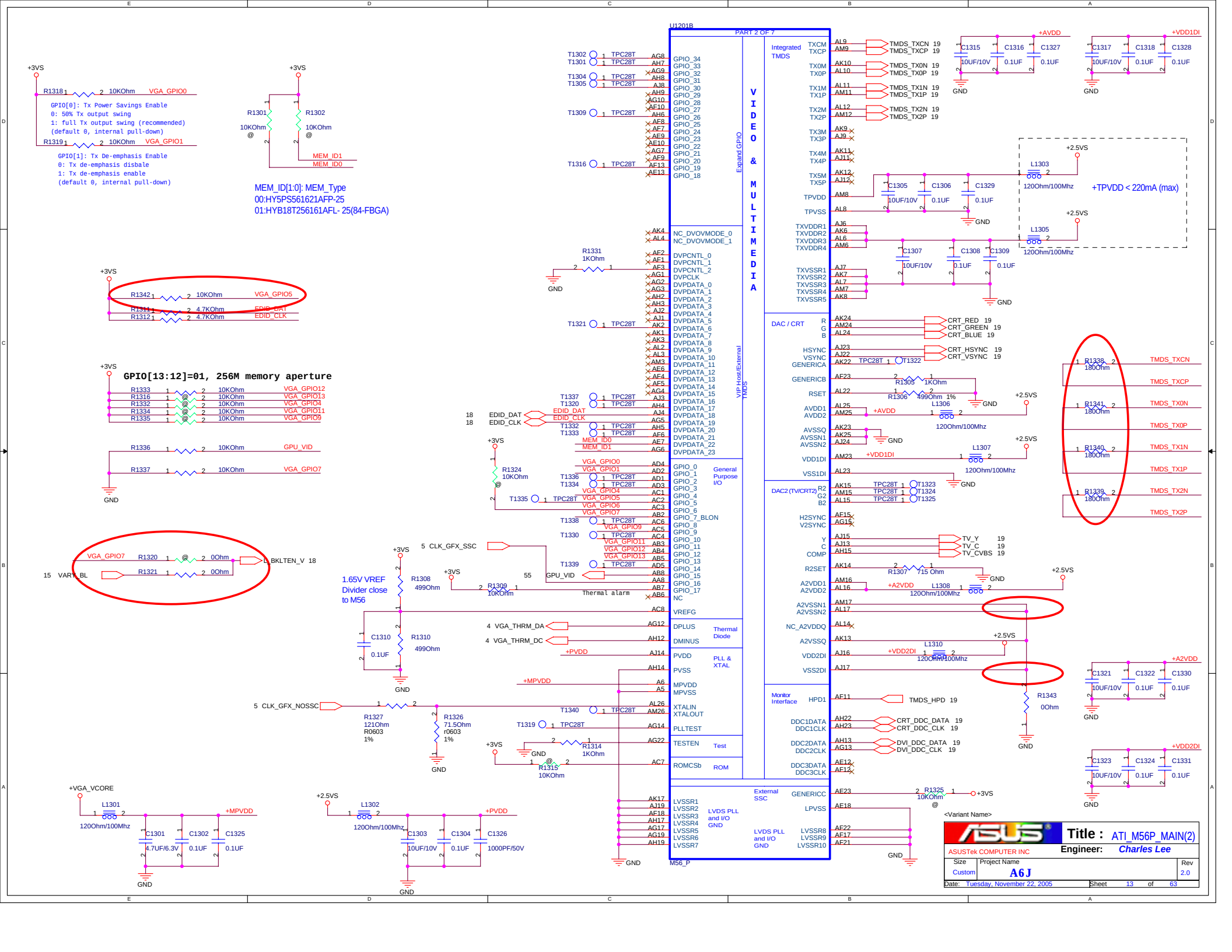
ASUSTek COMPUTER INC

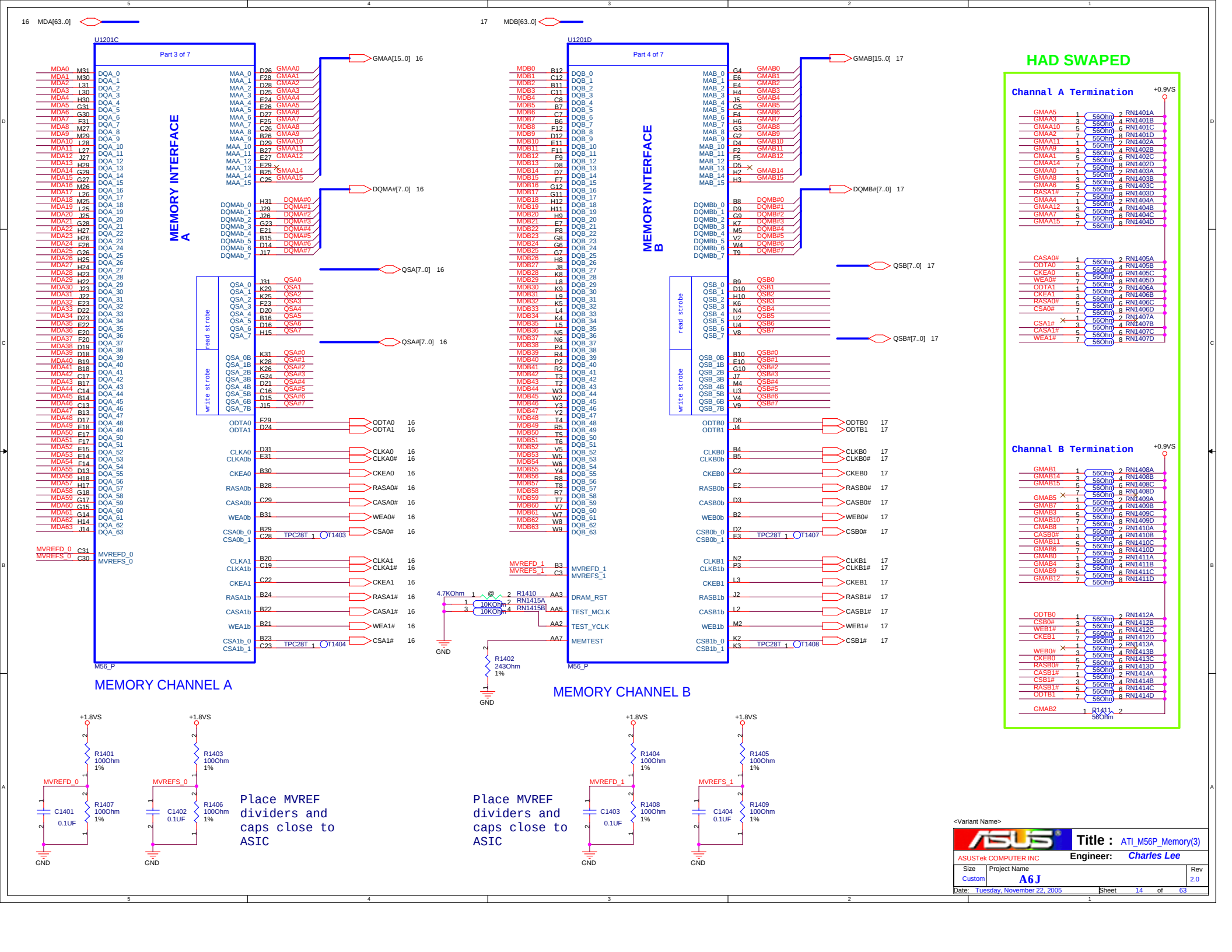
Title : ATI_M56P_PCI-E(1)

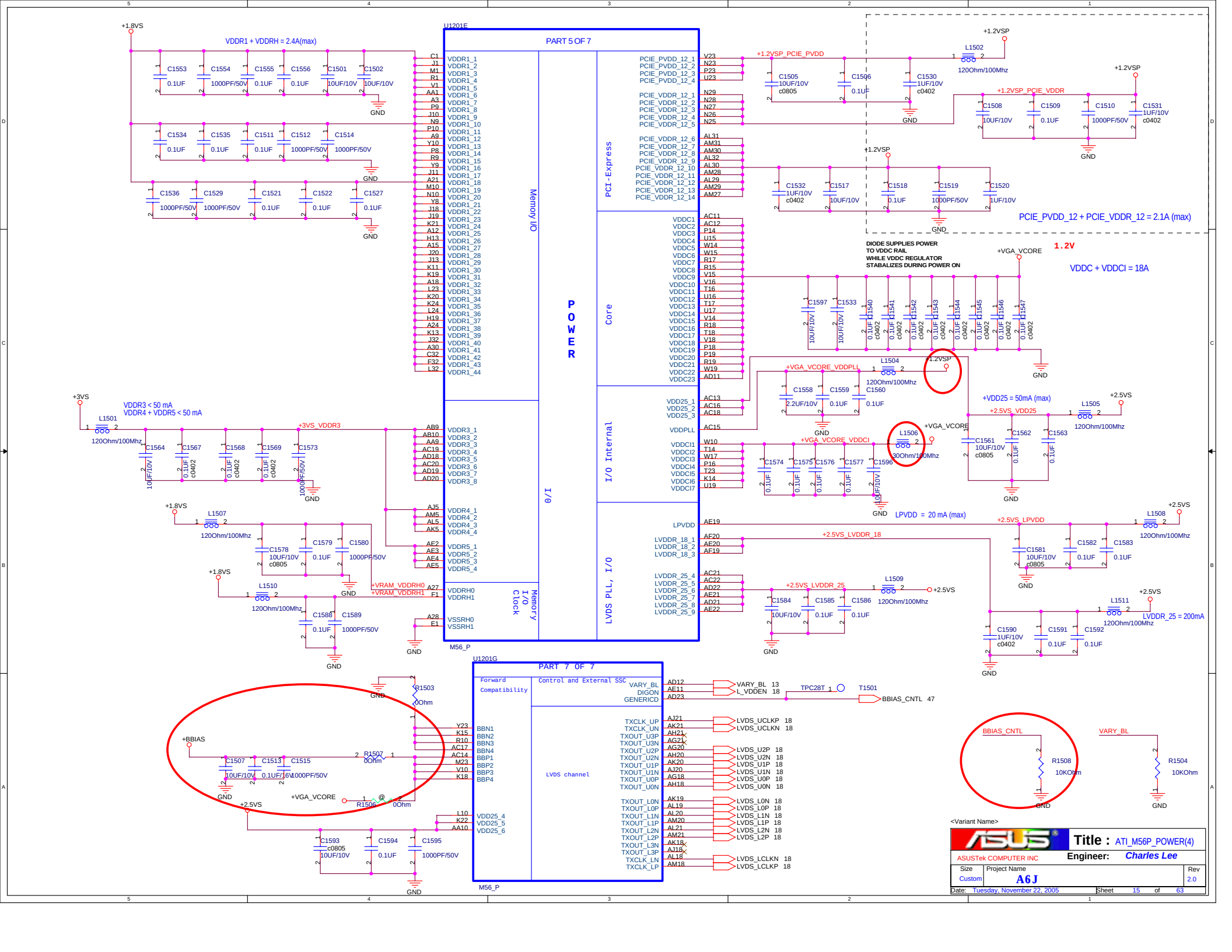
Engineer: Charles Lee

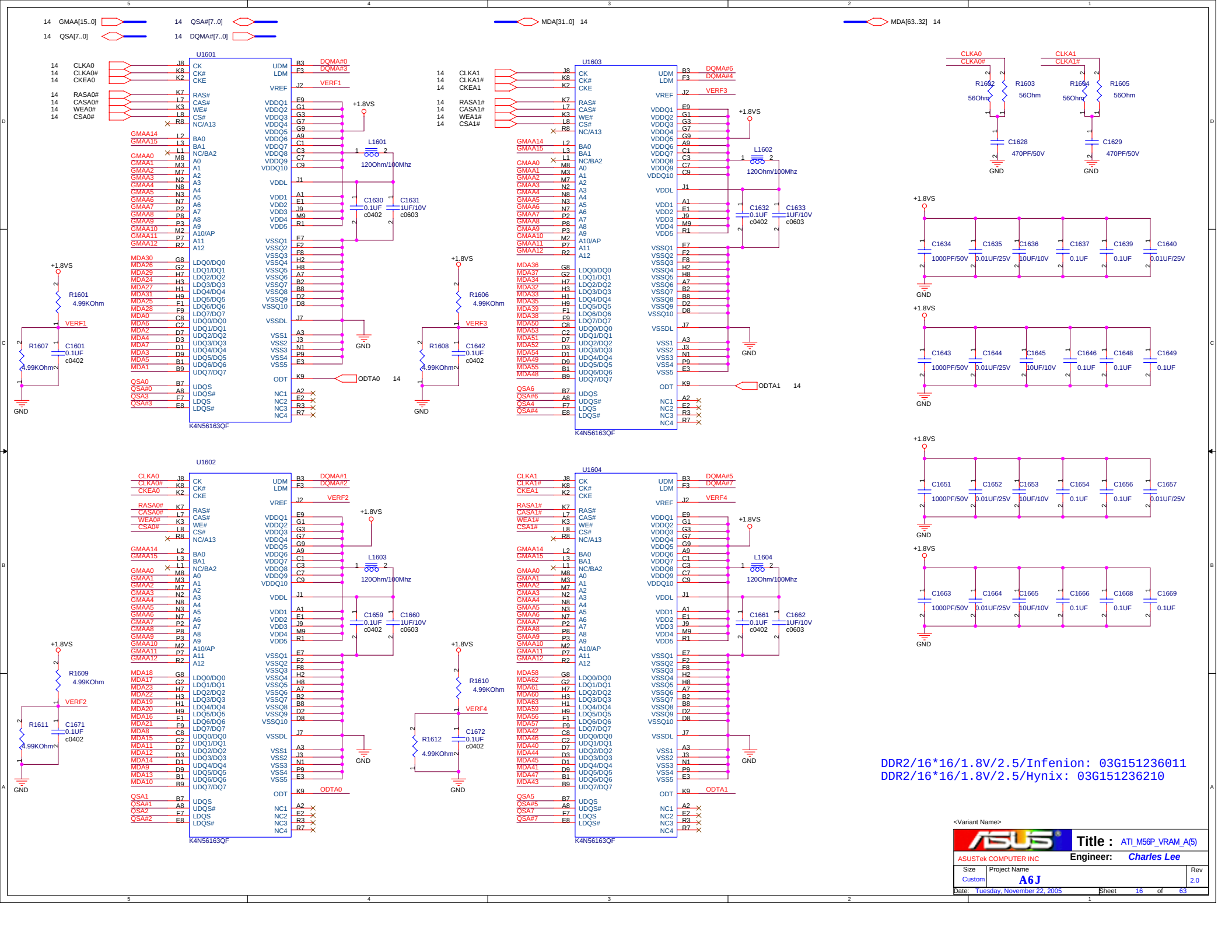
Size	Project Name	Rev
C	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 12 of 63

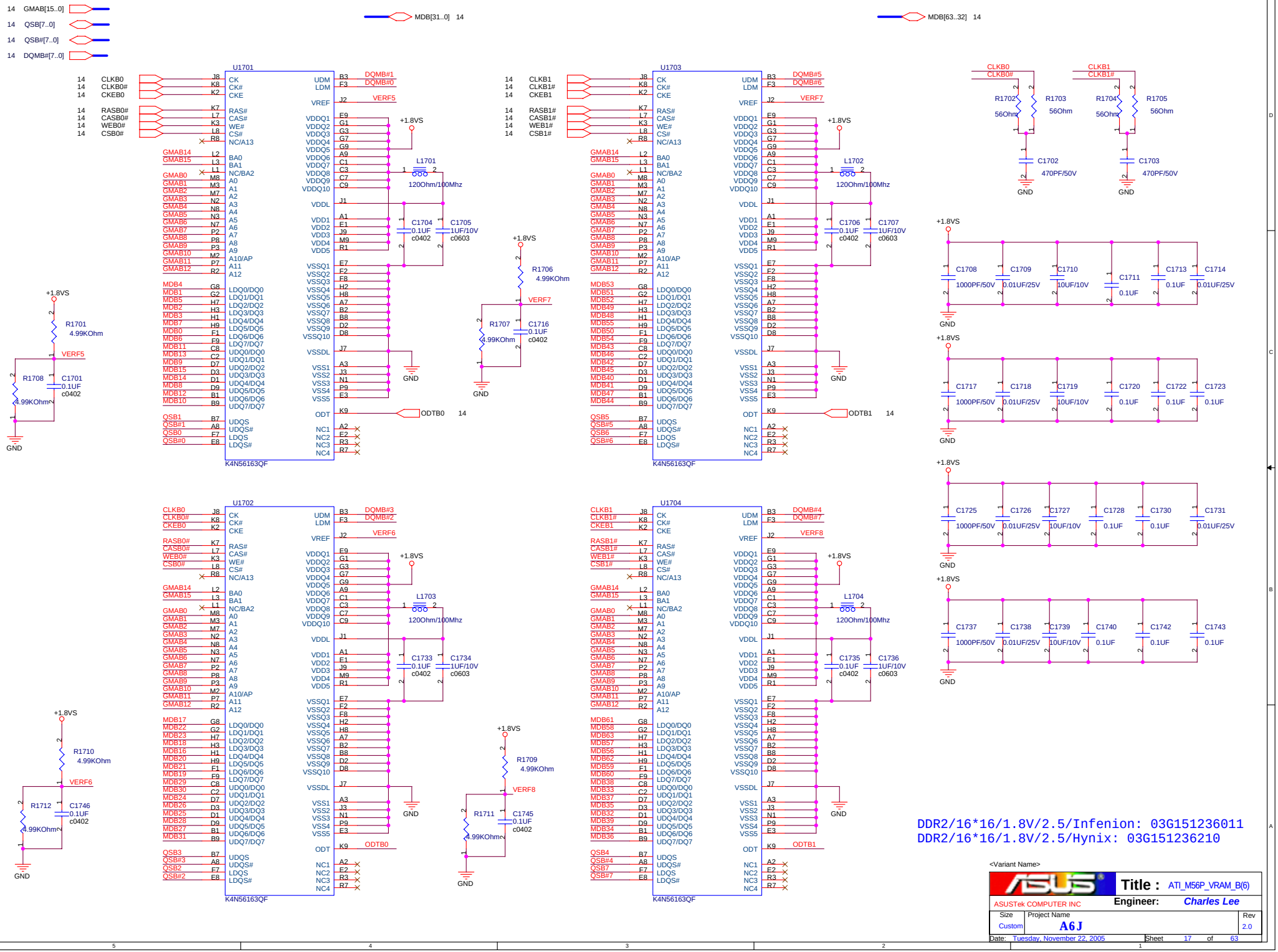

U1201B
PART 2 OF 7
VIDEO & MULTIMEDIA
Expand GPIO
VIP Host/External TMDS
GPIO_34
GPIO_33
GPIO_32
GPIO_31
GPIO_30
GPIO_29
GPIO_28
GPIO_27
GPIO_26
GPIO_25
GPIO_24
GPIO_23
GPIO_22
GPIO_21
GPIO_20
GPIO_19
GPIO_18
NC_DVOVMODE_0
NC_DVOVMODE_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7_BLON
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13
GPIO_14
GPIO_15
GPIO_16
GPIO_17
NC
VREFG
DPLUS
DMINUS
PVDD
PVSS
MPVDD
MPVSS
XTALIN
XTALOUT
PLLTEST
TESTEN
ROMCSb
LVSSR1
LVSSR2
LVSSR3
LVSSR4
LVSSR5
LVSSR6
LVSSR7
Integrated TMDS
TXCM
TXCP
TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TX3M
TX3P
TX4M
TX4P
TX5M
TX5P
TPVDD
TPVSS
TXVDDR1
TXVDDR2
TXVDDR3
TXVDDR4
TXVSSR1
TXVSSR2
TXVSSR3
TXVSSR4
TXVSSR5
DAC / CRT
R
G
B
HSYNC
VSYNC
GENERICA
GENERICB
RSET
AVDD1
AVDD2
AVSSQ
AVSSN1
AVSSN2
VDD1DI
VSS1DI
DAC2 (TV/CRT2)
R2
G2
B2
H2SYNC
V2SYNC
Y
C
COMP
R2SET
A2VDD1
A2VDD2
A2VSSN1
A2VSSN2
NC_A2VDDQ
A2VSSQ
VDD2DI
VSS2DI
Monitor Interface
HPD1
DDC1DATA
DDC1CLK
DDC2DATA
DDC2CLK
DDC3DATA
DDC3CLK
General Purpose I/O
Thermal Diode
PLL & XTAL
Test
ROM
External SSC
GENERICC
LPVSS
LVDS PLL and I/O GND
LVSSR8
LVSSR9
LVSSR10
M56_P
MEM_ID[1:0]: MEM_Type
00:HY5PS561621AFP-25
01:HYB18T256161AFL- 25(84-FBGA)
GPIO[13:12]=01, 256M memory aperture
1.65V VREF Divider close to M56
<Variant Name>
ASUSTek COMPUTER INC
Title : ATI_M56P_MAIN(2)
Engineer: Charles Lee
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 13 of 63


16 MDA[63..0]
17 MDB[63..0]
U1201C
Part 3 of 7
MEMORY INTERFACE A
U1201D
Part 4 of 7
MEMORY INTERFACE B
GMAA[15..0] 16
GMAB[15..0] 17
DQMA#[7..0] 16
DQMB#[7..0] 17
QSA[7..0] 16
QSB[7..0] 17
QSA#[7..0] 16
QSB#[7..0] 17
read strobe
write strobe
ODTA0
ODTA1
ODTB0
ODTB1
CLKA0
CLKA0b
CLKA1
CLKA1b
CLKB0
CLKB0b
CLKB1
CLKB1b
CKEA0
CKEA1
CKEB0
CKEB1
RASA0b
RASA1b
RASB0b
RASB1b
CASA0b
CASA1b
CASB0b
CASB1b
WEA0b
WEA1b
WEB0b
WEB1b
CSA0b_0
CSA0b_1
CSA1b_0
CSA1b_1
CSB0b_0
CSB0b_1
CSB1b_0
CSB1b_1
TPC28T 1 T1403
TPC28T 1 T1404
TPC28T 1 T1407
TPC28T 1 T1408
MVREFD_0
MVREFS_0
MVREFD_1
MVREFS_1
DRAM_RST
TEST_MCLK
TEST_YCLK
MEMTEST
4.7KOhm
10KOhm
RN1415A
RN1415B
R1410
R1402
243Ohm
1%
GND
M56_P
MEMORY CHANNEL A
MEMORY CHANNEL B
HAD SWAPED
Channal A Termination
Channal B Termination
+0.9VS
RN1401A
RN1401B
RN1401C
RN1401D
RN1402A
RN1402B
RN1402C
RN1402D
RN1403A
RN1403B
RN1403C
RN1403D
RN1404A
RN1404B
RN1404C
RN1404D
RN1405A
RN1405B
RN1405C
RN1405D
RN1406A
RN1406B
RN1406C
RN1406D
RN1407A
RN1407B
RN1407C
RN1407D
RN1408A
RN1408B
RN1408C
RN1408D
RN1409A
RN1409B
RN1409C
RN1409D
RN1410A
RN1410B
RN1410C
RN1410D
RN1411A
RN1411B
RN1411C
RN1411D
RN1412A
RN1412B
RN1412C
RN1412D
RN1413A
RN1413B
RN1413C
RN1413D
RN1414A
RN1414B
RN1414C
RN1414D
56Ohm
+1.8VS
R1401 100Ohm 1%
R1403 100Ohm 1%
R1404 100Ohm 1%
R1405 100Ohm 1%
R1407 100Ohm 1%
R1406 100Ohm 1%
R1408 100Ohm 1%
R1409 100Ohm 1%
C1401 0.1UF
C1402 0.1UF
C1403 0.1UF
C1404 0.1UF
Place MVREF dividers and caps close to ASIC
Place MVREF dividers and caps close to ASIC
<Variant Name>
Title : ATI_M56P_Memory(3)
ASUSTek COMPUTER INC
Engineer: Charles Lee
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 14 of 63

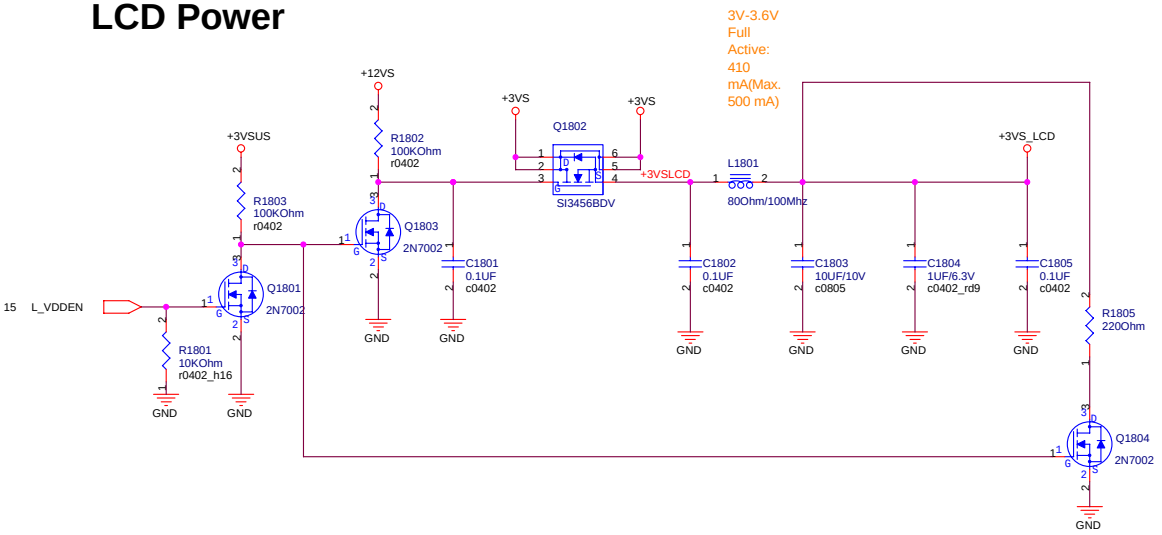

U1201E
PART 5 OF 7
POWER
Memory I/O
PCI-Express
Core
I/O Internal
LVDS PLL, I/O
Memory I/O Clock
VDDR1 + VDDRH = 2.4A(max)
PCIE_PVDD_12 + PCIE_VDDR_12 = 2.1A (max)
DIODE SUPPLIES POWER TO VDDC RAIL WHILE VDDC REGULATOR STABALIZES DURING POWER ON
1.2V
VDDC + VDDCI = 18A
VDDR3 < 50 mA
VDDR4 + VDDR5 < 50 mA
VDD25 = 50mA (max)
LPVDD = 20 mA (max)
LVDDR_25 = 200mA
U1201G
PART 7 OF 7
Forward Compatibility
Control and External SSC
LVDS channel
M56_P
<Variant Name>
Title : ATI_M56P_POWER(4)
ASUSTek COMPUTER INC
Engineer: Charles Lee
Size: Custom
Project Name: A6J
Rev: 2.0
Date: Tuesday, November 22, 2005
Sheet 15 of 63



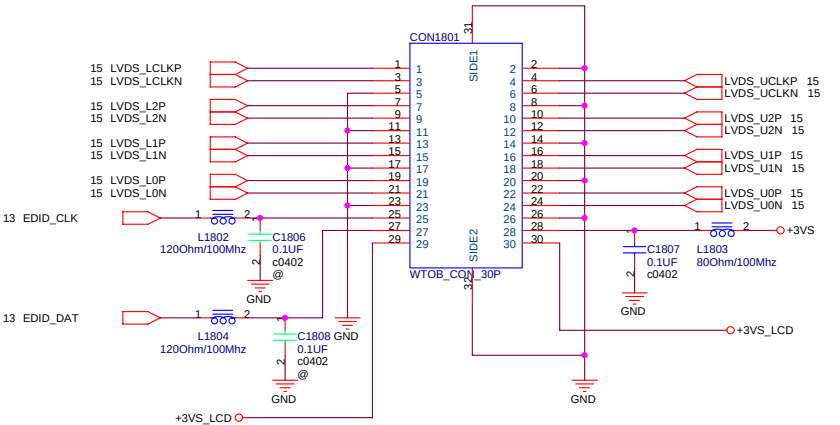
GMAA[15..0]
QSA[7..0]
QSA#[7..0]
DQMA#[7..0]
MDA[31..0]
MDA[63..32]
U1601
U1602
U1603
U1604
K4N56163QF
CLKA0
CLKA0#
CKEA0
RASA0#
CASA0#
WEA0#
CSA0#
CLKA1
CLKA1#
CKEA1
RASA1#
CASA1#
WEA1#
CSA1#
+1.8VS
GND
L1601
L1602
L1603
L1604
120Ohm/100Mhz
C1630 0.1UF c0402
C1631 1UF/10V c0603
C1632 0.1UF c0402
C1633 1UF/10V c0603
C1659 0.1UF c0402
C1660 1UF/10V c0603
C1661 0.1UF c0402
C1662 1UF/10V c0603
R1601 4.99KOhm
R1607 4.99KOhm
C1601 0.1UF c0402
R1606 4.99KOhm
R1608 4.99KOhm
C1642 0.1UF c0402
R1609 4.99KOhm
R1611 4.99KOhm
C1671 0.1UF c0402
R1610 4.99KOhm
R1612 4.99KOhm
C1672 0.1UF c0402
R1602 56Ohm
R1603 56Ohm
R1604 56Ohm
R1605 56Ohm
C1628 470PF/50V
C1629 470PF/50V
C1634 1000PF/50V
C1635 0.01UF/25V
C1636 10UF/10V
C1637 0.1UF
C1639 0.1UF
C1640 0.01UF/25V
C1643 1000PF/50V
C1644 0.01UF/25V
C1645 10UF/10V
C1646 0.1UF
C1648 0.1UF
C1649 0.1UF
C1651 1000PF/50V
C1652 0.01UF/25V
C1653 10UF/10V
C1654 0.1UF
C1656 0.1UF
C1657 0.01UF/25V
C1663 1000PF/50V
C1664 0.01UF/25V
C1665 10UF/10V
C1666 0.1UF
C1668 0.1UF
C1669 0.1UF
DDR2/16*16/1.8V/2.5/Infenion: 03G151236011
DDR2/16*16/1.8V/2.5/Hynix: 03G151236210
<Variant Name>
Title : ATI_M56P_VRAM_A(5)
ASUSTek COMPUTER INC
Engineer: Charles Lee
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 16 of 63


14 GMAB[15..0]
14 QSB[7..0]
14 QSB#[7..0]
14 DQMB#[7..0]
MDB[31..0] 14
MDB[63..32] 14
U1701
U1702
U1703
U1704
K4N56163QF
+1.8VS
GND
ODTB0 14
ODTB1 14
120Ohm/100Mhz
DDR2/16*16/1.8V/2.5/Infenion: 03G151236011
DDR2/16*16/1.8V/2.5/Hynix: 03G151236210
<Variant Name>
Title : ATI_M56P_VRAM_B(6)
ASUSTek COMPUTER INC
Engineer: Charles Lee
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 17 of 63

LCD Power



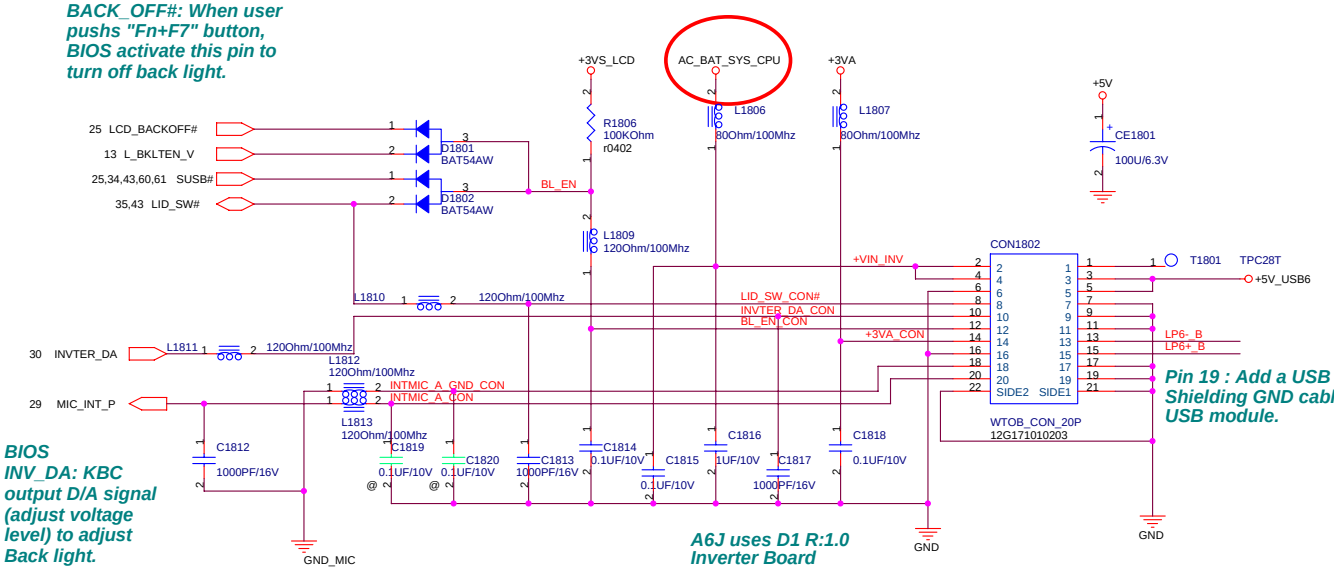
LCD LVDS Interface



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

INVERTER Interface

BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.

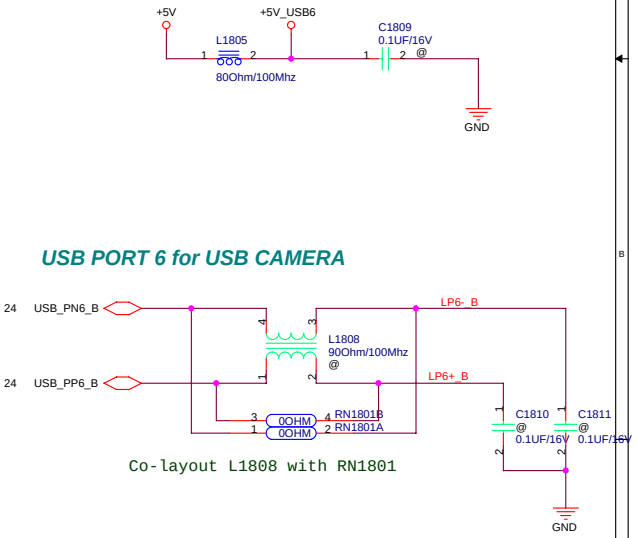


Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.

A6J uses D1 R:1.0 Inverter Board

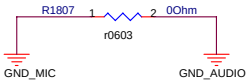
BIOS
INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.

USB PORT 6 for USB CAMERA



Co-layout L1808 with RN1801

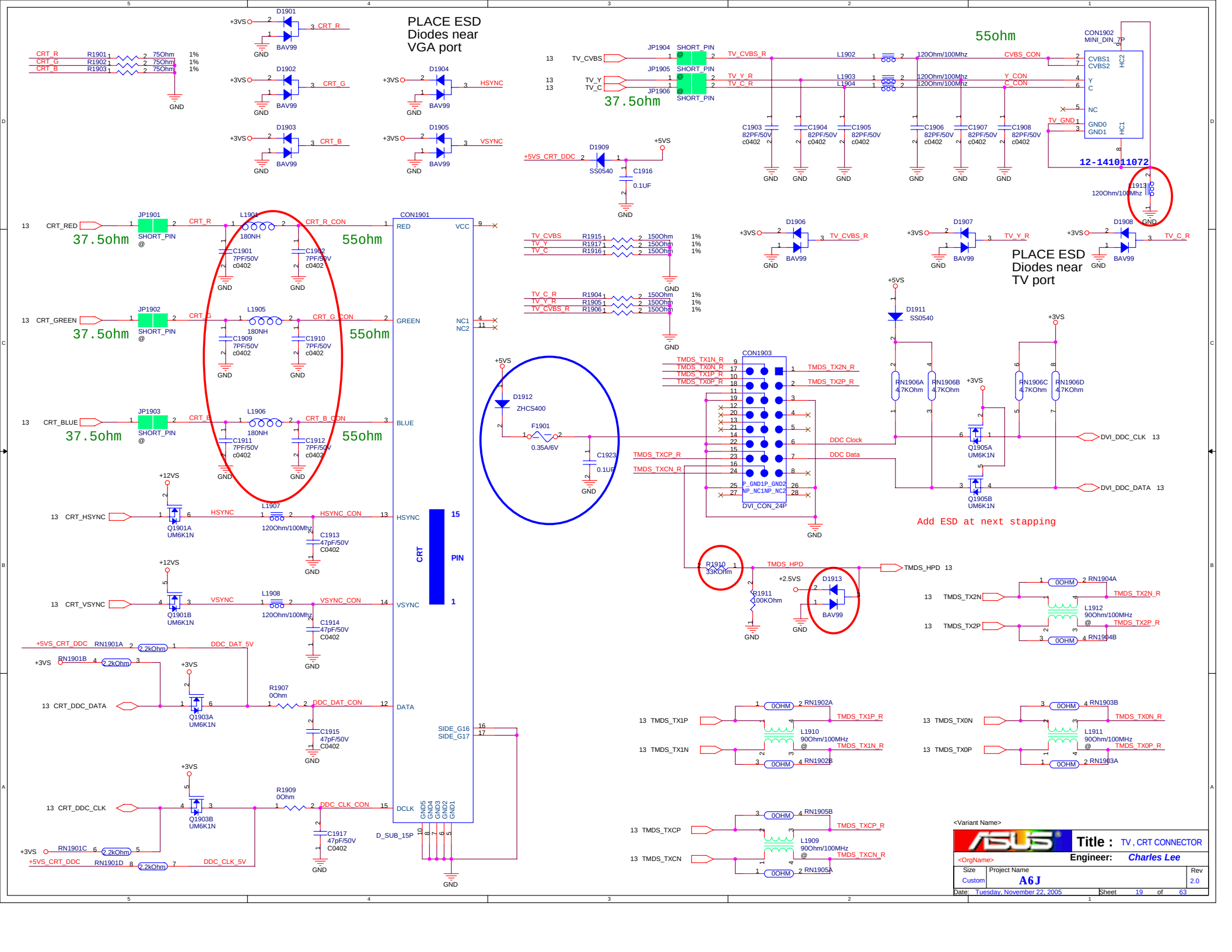
For EMI

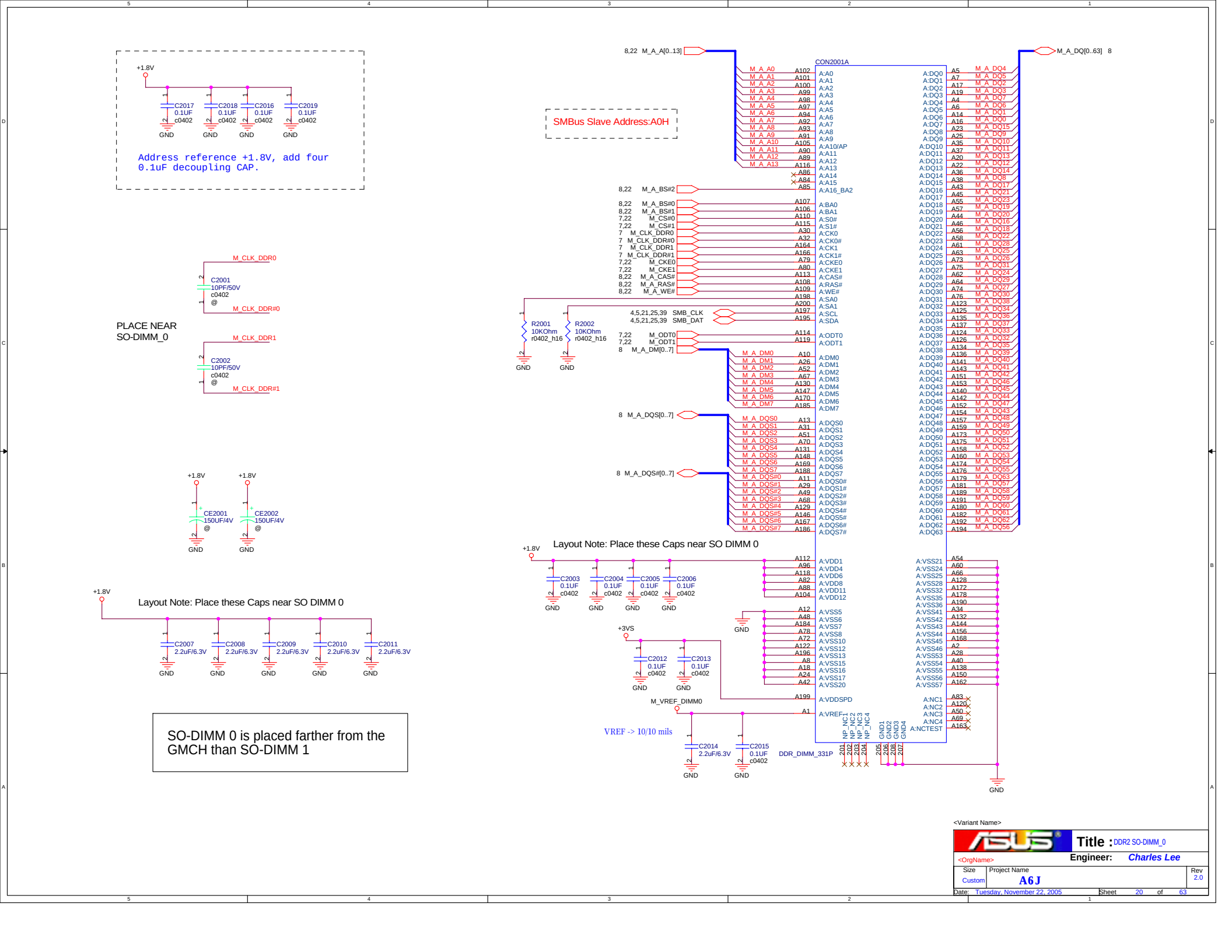


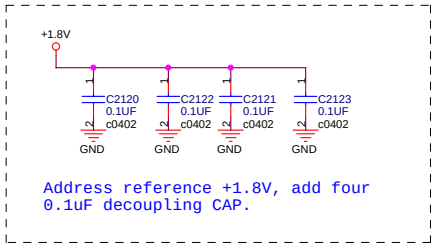
A6J doesn't support USB WLAN function!

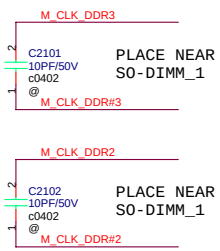
<Variant Name>

<OrgName>	Title : LVDS & INVERTER	
	Engineer: Charles Lee	
Size: Custom	Project Name: A6J	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 18 of 63	

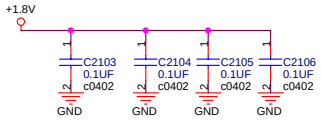

PLACE ESD
Diodes near
VGA port
PLACE ESD
Diodes near
TV port
55ohm
37.5ohm
CON1902
MINI_DIN_7P
12-141011072
CON1901
CON1903
DVI_CON_24P
CRT
PIN
D_SUB_15P
Add ESD at next stapping
Title : TV , CRT CONNECTOR
Engineer: Charles Lee
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 19 of 63


+1.8V
C2017 0.1UF c0402
C2018 0.1UF c0402
C2016 0.1UF c0402
C2019 0.1UF c0402
GND
Address reference +1.8V, add four 0.1uF decoupling CAP.
M_CLK_DDR0
C2001 10PF/50V c0402 @
M_CLK_DDR#0
PLACE NEAR SO-DIMM_0
M_CLK_DDR1
C2002 10PF/50V c0402 @
M_CLK_DDR#1
+1.8V
CE2001 150UF/4V @
CE2002 150UF/4V @
Layout Note: Place these Caps near SO DIMM 0
C2007 2.2uF/6.3V
C2008 2.2uF/6.3V
C2009 2.2uF/6.3V
C2010 2.2uF/6.3V
C2011 2.2uF/6.3V
SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1
8,22 M_A_A[0..13]
SMBus Slave Address:A0H
CON2001A
M_A_A0 A102 A:A0
M_A_A1 A101 A:A1
M_A_A2 A100 A:A2
M_A_A3 A99 A:A3
M_A_A4 A98 A:A4
M_A_A5 A97 A:A5
M_A_A6 A94 A:A6
M_A_A7 A92 A:A7
M_A_A8 A93 A:A8
M_A_A9 A91 A:A9
M_A_A10 A105 A:A10/AP
M_A_A11 A90 A:A11
M_A_A12 A89 A:A12
M_A_A13 A116 A:A13
A86 A:A14
A84 A:A15
8,22 M_A_BS#2 A85 A:A16_BA2
8,22 M_A_BS#0 A107 A:BA0
8,22 M_A_BS#1 A106 A:BA1
7,22 M_CS#0 A110 A:S0#
7,22 M_CS#1 A115 A:S1#
7 M_CLK_DDR0 A30 A:CK0
7 M_CLK_DDR#0 A32 A:CK0#
7 M_CLK_DDR1 A164 A:CK1
7 M_CLK_DDR#1 A166 A:CK1#
7,22 M_CKE0 A79 A:CKE0
7,22 M_CKE1 A80 A:CKE1
8,22 M_A_CAS# A113 A:CAS#
8,22 M_A_RAS# A108 A:RAS#
8,22 M_A_WE# A109 A:WE#
A198 A:SA0
A200 A:SA1
4,5,21,25,39 SMB_CLK A197 A:SCL
4,5,21,25,39 SMB_DAT A195 A:SDA
R2001 10KOhm r0402_h16
R2002 10KOhm r0402_h16
GND
7,22 M_ODT0 A114 A:ODT0
7,22 M_ODT1 A119 A:ODT1
8 M_A_DM[0..7]
M_A_DM0 A10 A:DM0
M_A_DM1 A26 A:DM1
M_A_DM2 A52 A:DM2
M_A_DM3 A67 A:DM3
M_A_DM4 A130 A:DM4
M_A_DM5 A147 A:DM5
M_A_DM6 A170 A:DM6
M_A_DM7 A185 A:DM7
8 M_A_DQS[0..7]
M_A_DQS0 A13 A:DQS0
M_A_DQS1 A31 A:DQS1
M_A_DQS2 A51 A:DQS2
M_A_DQS3 A70 A:DQS3
M_A_DQS4 A131 A:DQS4
M_A_DQS5 A148 A:DQS5
M_A_DQS6 A169 A:DQS6
M_A_DQS7 A188 A:DQS7
8 M_A_DQS#[0..7]
M_A_DQS#0 A11 A:DQS0#
M_A_DQS#1 A29 A:DQS1#
M_A_DQS#2 A49 A:DQS2#
M_A_DQS#3 A68 A:DQS3#
M_A_DQS#4 A129 A:DQS4#
M_A_DQS#5 A146 A:DQS5#
M_A_DQS#6 A167 A:DQS6#
M_A_DQS#7 A186 A:DQS7#
M_A_DQ[0..63] 8
A:DQ0 A5 M_A_DQ4
A:DQ1 A7 M_A_DQ5
A:DQ2 A17 M_A_DQ2
A:DQ3 A19 M_A_DQ3
A:DQ4 A4 M_A_DQ7
A:DQ5 A6 M_A_DQ6
A:DQ6 A14 M_A_DQ1
A:DQ7 A16 M_A_DQ0
A:DQ8 A23 M_A_DQ15
A:DQ9 A25 M_A_DQ9
A:DQ10 A35 M_A_DQ10
A:DQ11 A37 M_A_DQ11
A:DQ12 A20 M_A_DQ13
A:DQ13 A22 M_A_DQ12
A:DQ14 A36 M_A_DQ14
A:DQ15 A38 M_A_DQ8
A:DQ16 A43 M_A_DQ17
A:DQ17 A45 M_A_DQ21
A:DQ18 A55 M_A_DQ23
A:DQ19 A57 M_A_DQ19
A:DQ20 A44 M_A_DQ20
A:DQ21 A46 M_A_DQ16
A:DQ22 A56 M_A_DQ18
A:DQ23 A58 M_A_DQ22
A:DQ24 A61 M_A_DQ28
A:DQ25 A63 M_A_DQ25
A:DQ26 A73 M_A_DQ26
A:DQ27 A75 M_A_DQ31
A:DQ28 A62 M_A_DQ24
A:DQ29 A64 M_A_DQ29
A:DQ30 A74 M_A_DQ27
A:DQ31 A76 M_A_DQ30
A:DQ32 A123 M_A_DQ38
A:DQ33 A125 M_A_DQ34
A:DQ34 A135 M_A_DQ36
A:DQ35 A137 M_A_DQ37
A:DQ36 A124 M_A_DQ33
A:DQ37 A126 M_A_DQ32
A:DQ38 A134 M_A_DQ35
A:DQ39 A136 M_A_DQ39
A:DQ40 A141 M_A_DQ40
A:DQ41 A143 M_A_DQ41
A:DQ42 A151 M_A_DQ42
A:DQ43 A153 M_A_DQ46
A:DQ44 A140 M_A_DQ45
A:DQ45 A142 M_A_DQ44
A:DQ46 A152 M_A_DQ47
A:DQ47 A154 M_A_DQ43
A:DQ48 A157 M_A_DQ48
A:DQ49 A159 M_A_DQ49
A:DQ50 A173 M_A_DQ50
A:DQ51 A175 M_A_DQ51
A:DQ52 A158 M_A_DQ52
A:DQ53 A160 M_A_DQ53
A:DQ54 A174 M_A_DQ54
A:DQ55 A176 M_A_DQ55
A:DQ56 A179 M_A_DQ63
A:DQ57 A181 M_A_DQ57
A:DQ58 A189 M_A_DQ58
A:DQ59 A191 M_A_DQ59
A:DQ60 A180 M_A_DQ60
A:DQ61 A182 M_A_DQ61
A:DQ62 A192 M_A_DQ62
A:DQ63 A194 M_A_DQ56
+1.8V
Layout Note: Place these Caps near SO DIMM 0
C2003 0.1UF c0402
C2004 0.1UF c0402
C2005 0.1UF c0402
C2006 0.1UF c0402
A112 A:VDD1
A96 A:VDD4
A118 A:VDD6
A82 A:VDD8
A88 A:VDD11
A104 A:VDD12
A12 A:VSS5
A48 A:VSS6
A184 A:VSS7
A78 A:VSS8
A72 A:VSS10
A122 A:VSS12
A196 A:VSS13
A8 A:VSS15
A18 A:VSS16
A24 A:VSS17
A42 A:VSS20
+3VS
C2012 0.1UF c0402
C2013 0.1UF c0402
M_VREF_DIMM0
A199 A:VDDSPD
A1 A:VREF
VREF -> 10/10 mils
C2014 2.2uF/6.3V
C2015 0.1UF c0402
DDR_DIMM_331P
NP_NC1 201
NP_NC2 202
NP_NC3 203
NP_NC4 204
GND1 205
GND2 206
GND3 208
GND4 207
A:NCTEST
A:NC1 A83
A:NC2 A120
A:NC3 A50
A:NC4 A69
A163
A:VSS21 A54
A:VSS24 A60
A:VSS25 A66
A:VSS28 A128
A:VSS32 A172
A:VSS35 A178
A:VSS36 A190
A:VSS41 A34
A:VSS42 A132
A:VSS43 A144
A:VSS44 A156
A:VSS45 A168
A:VSS46 A2
A:VSS53 A28
A:VSS54 A40
A:VSS55 A138
A:VSS56 A150
A:VSS57 A162
<Variant Name>
Title : DDR2 SO-DIMM_0
<OrgName>
Engineer: Charles Lee
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 20 of 63

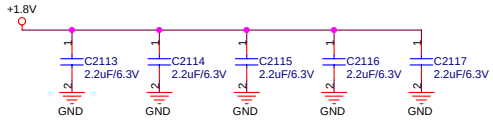


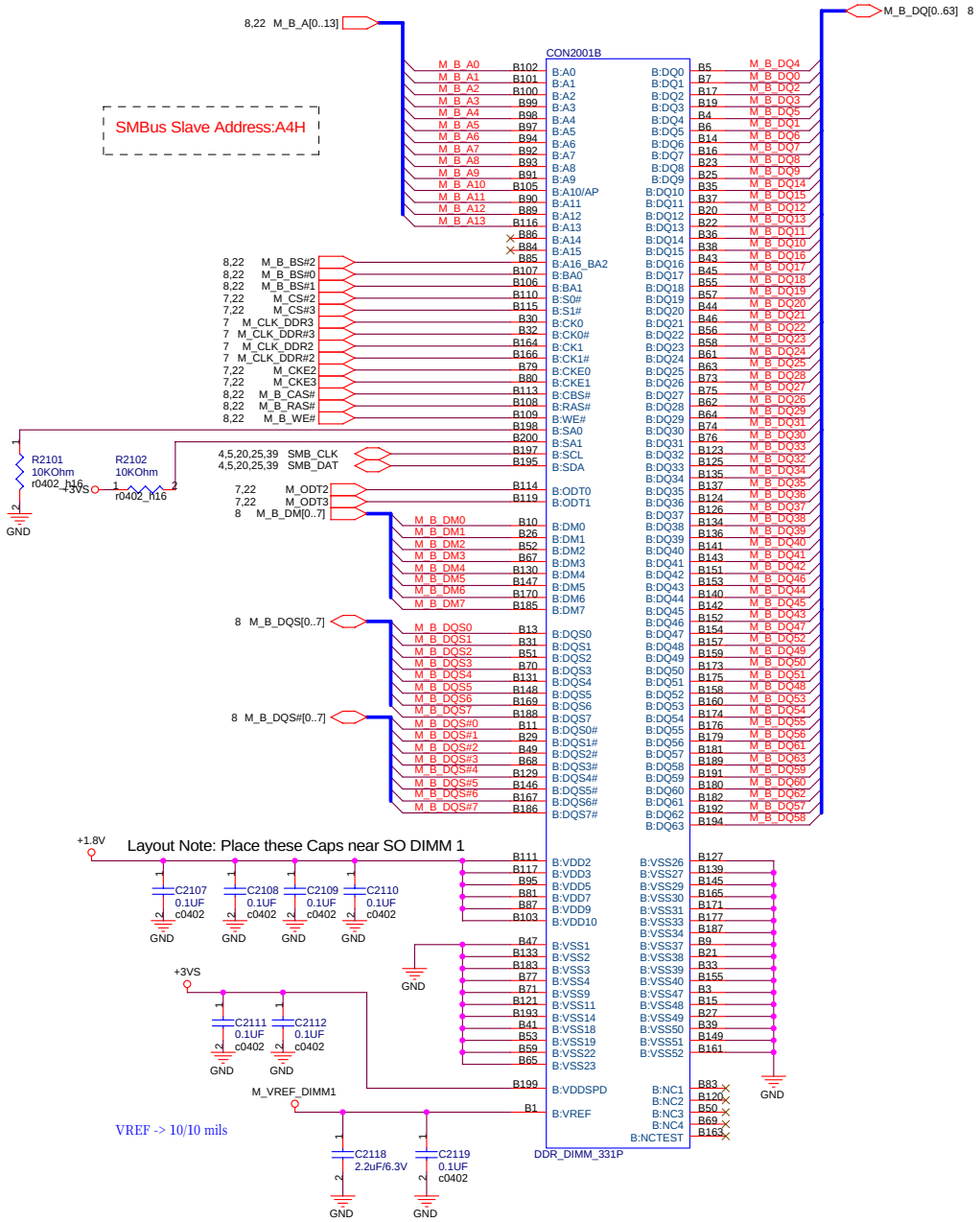


Layout Note: Place these High-Freq decoupling Caps near the GMCH



Layout Note: Place these CAPs near the GMCH



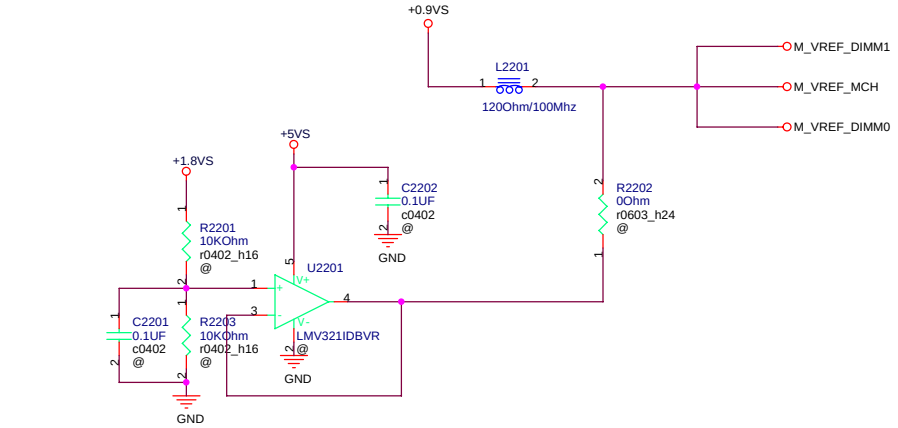


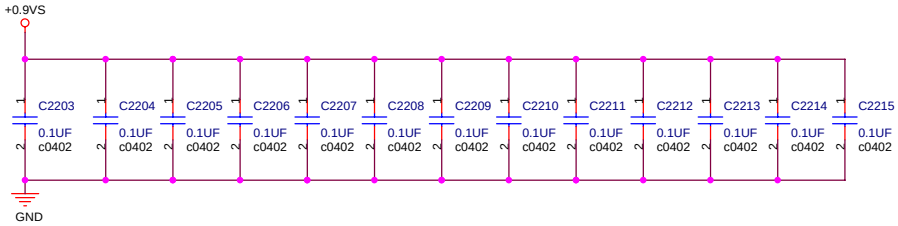
<variant_name>

Title : DDR2 SO-DIMM_1
<OrgName>
Engineer: Charles Lee

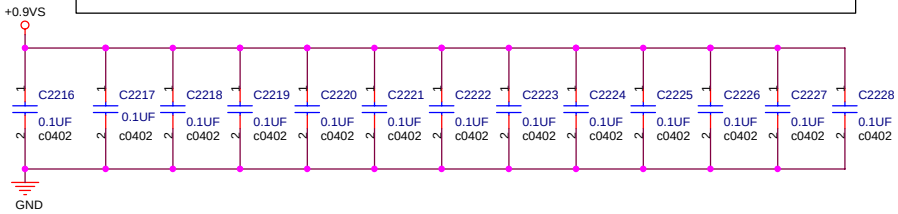
Size	Project Name	Rev
Custom	A6J	2.0

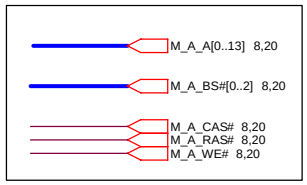
Date: Tuesday, November 22, 2005 Sheet 21 of 63

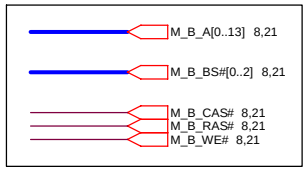


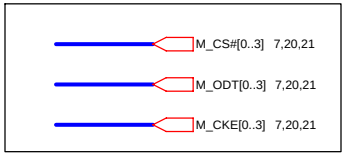


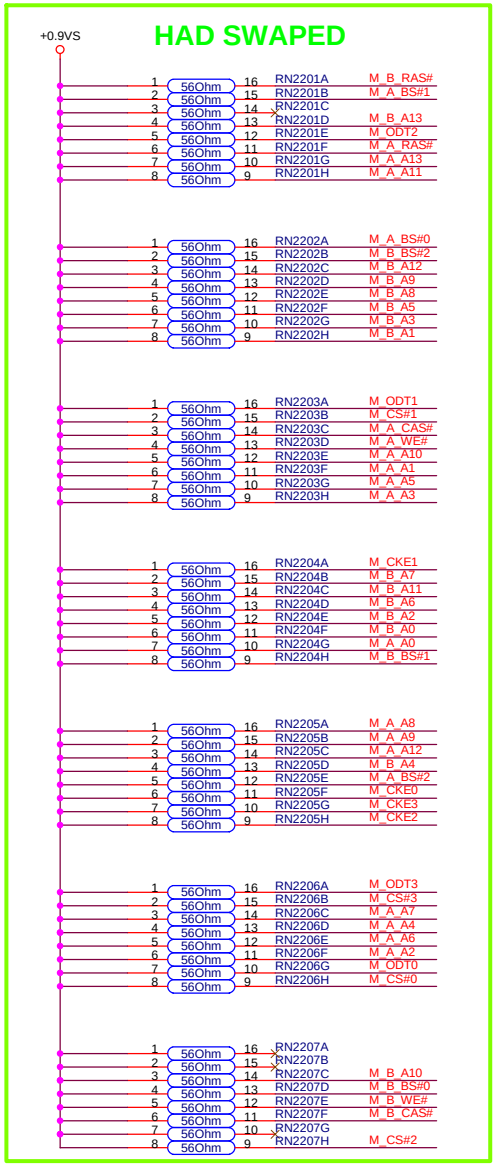
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS











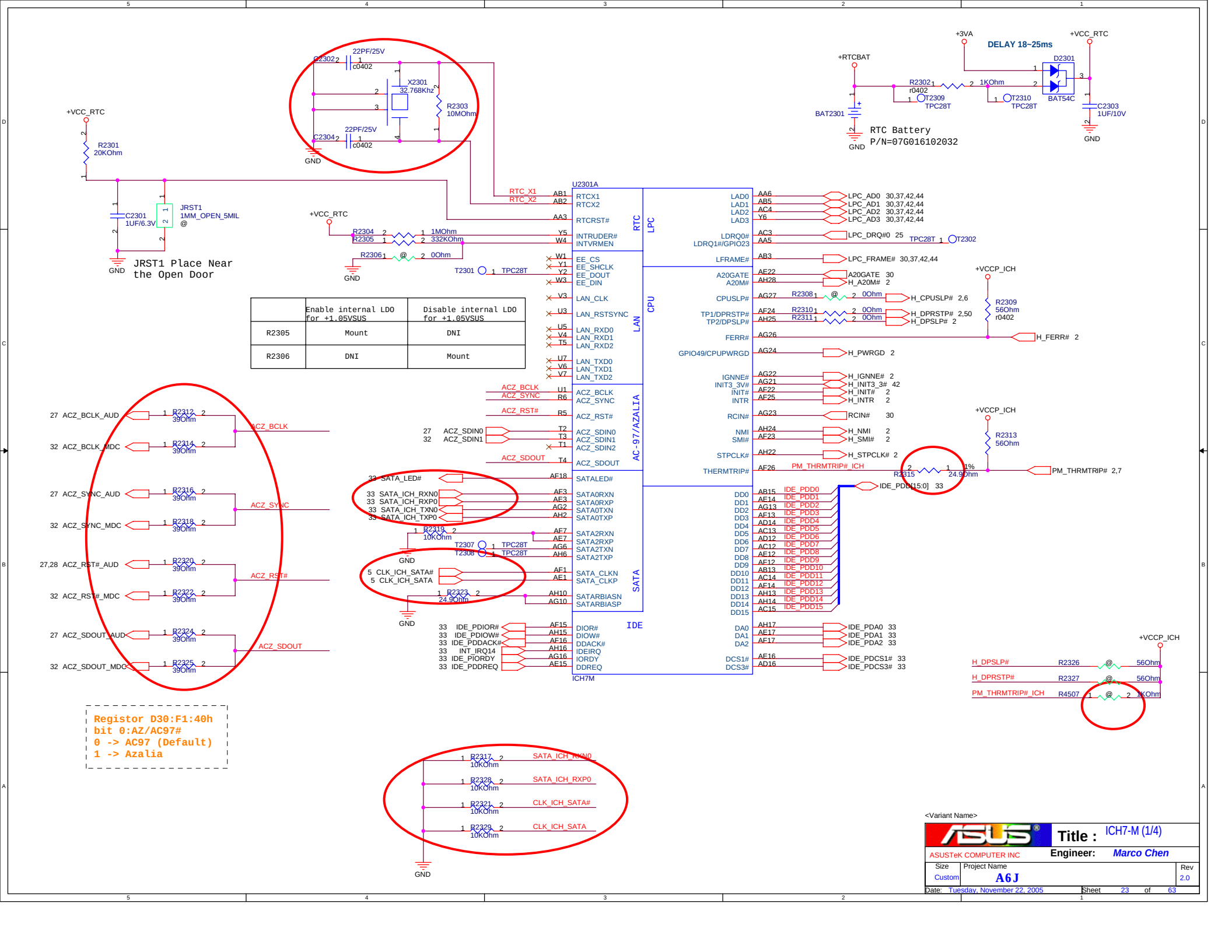
<Variant Name>

Title : DDR2 TERM

ASUSTeK COMPUTER INC Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 22 of 63



	Enable internal LDO for +1.05VSUS	Disable internal LDO for +1.05VSUS
R2305	Mount	DNI
R2306	DNI	Mount

<variant_name>

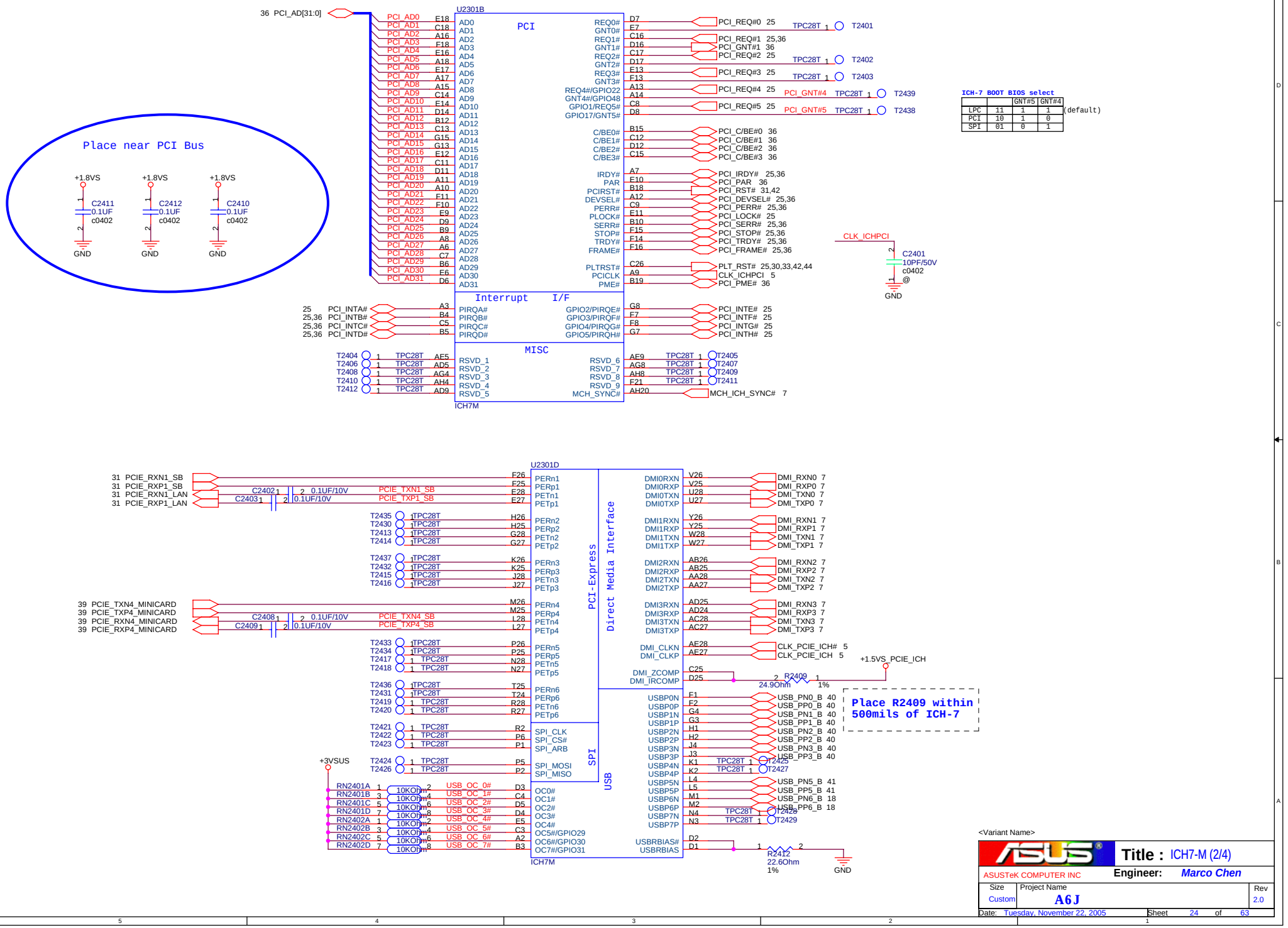
Title : ICH7-M (1/4)

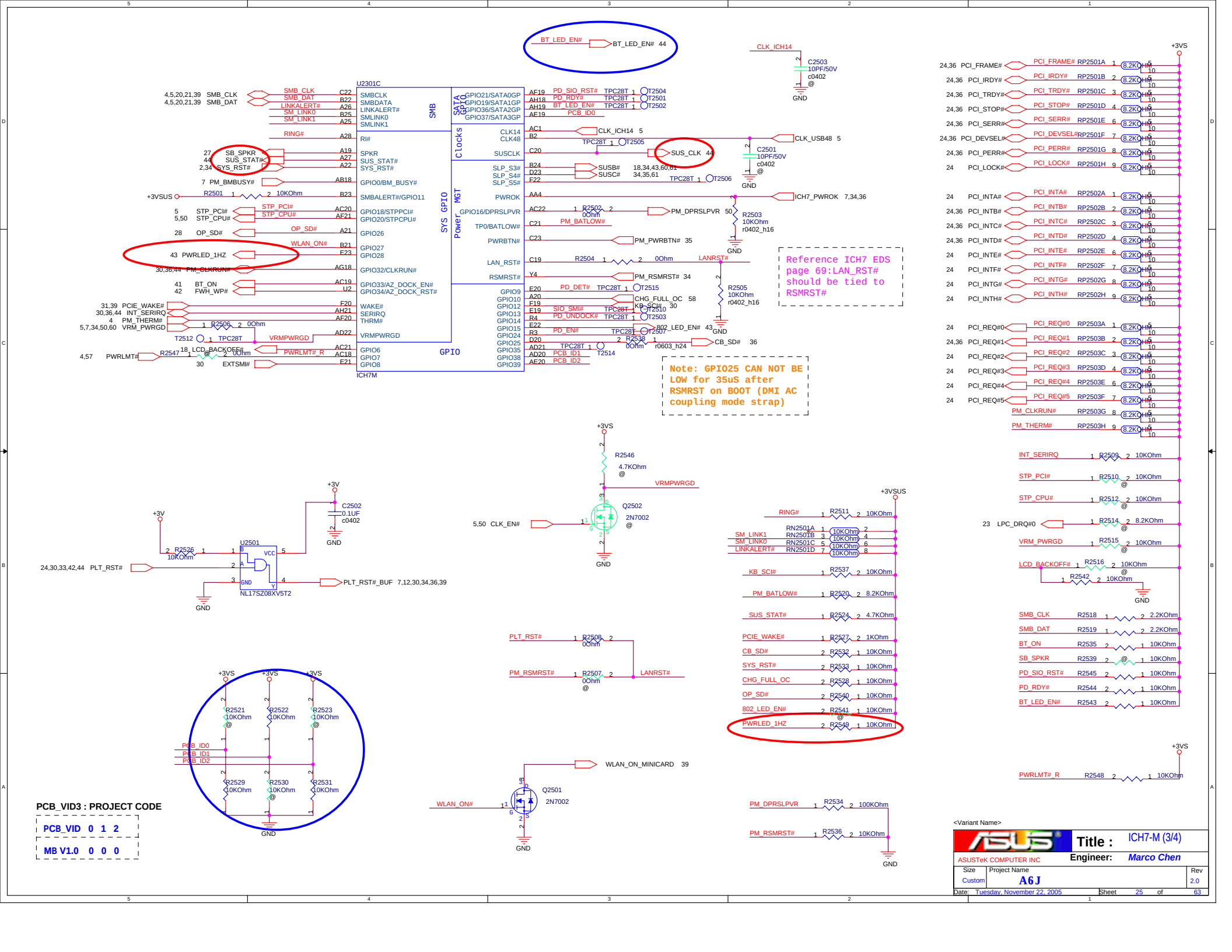
ASUSTeK COMPUTER INC

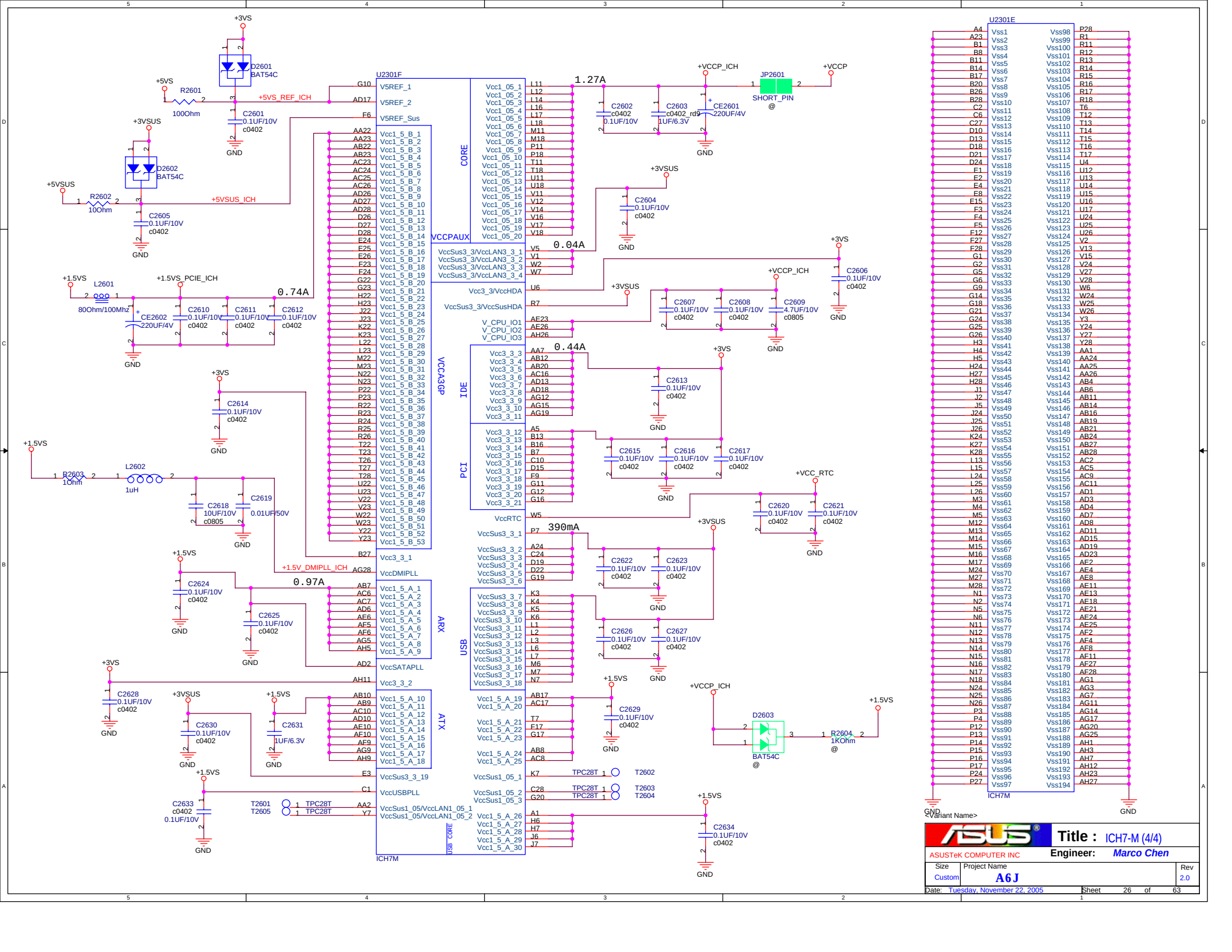
Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6J	2.0

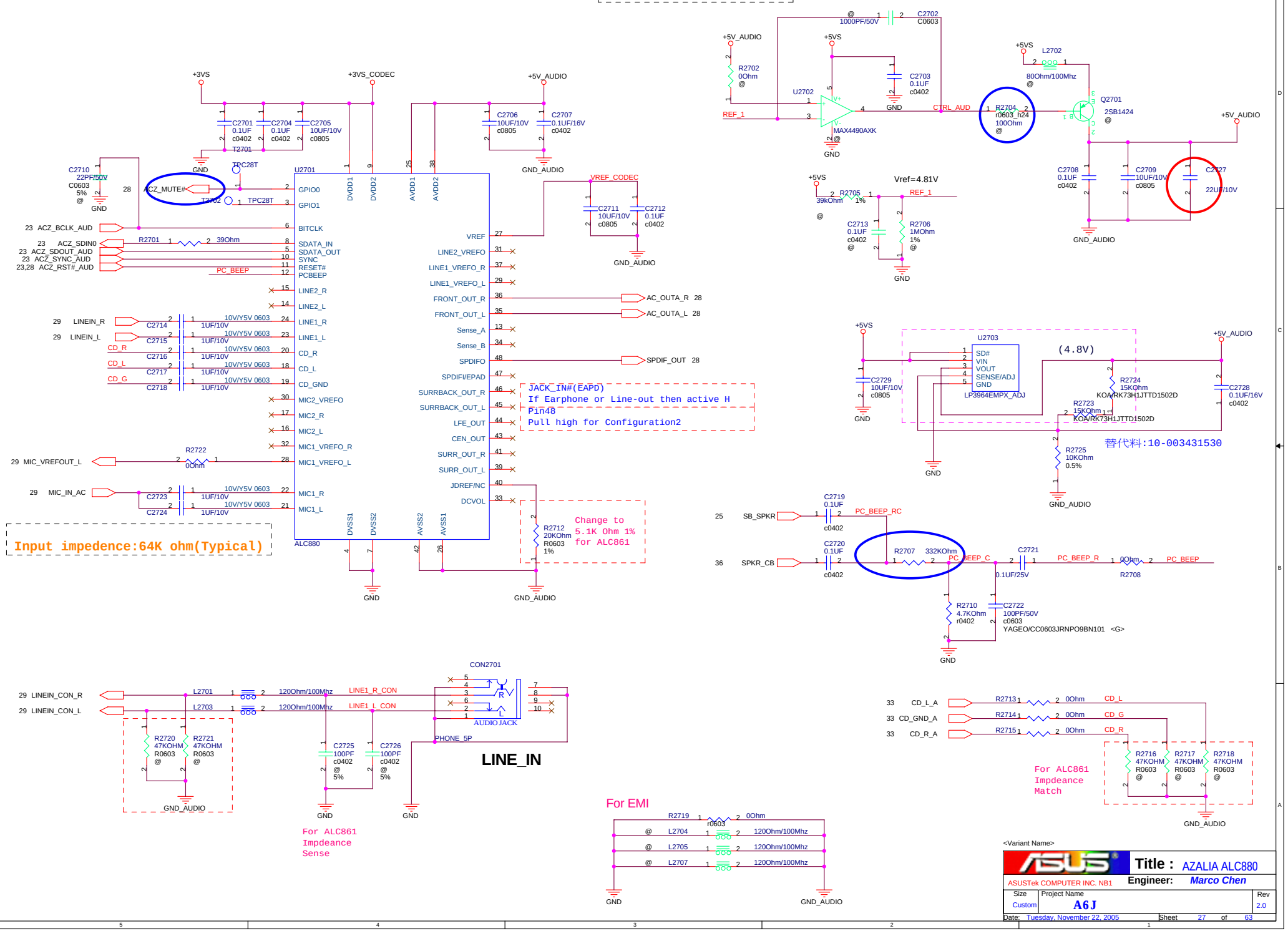
Date: Tuesday, November 22, 2005 Sheet 23 of 63


Place near PCI Bus
+1.8VS
C2411 0.1UF c0402
C2412 0.1UF c0402
C2410 0.1UF c0402
GND
36 PCI_AD[31:0]
U2301B
PCI
PCI_AD0 E18
PCI_AD1 C18
PCI_AD2 A16
PCI_AD3 F18
PCI_AD4 E16
PCI_AD5 A18
PCI_AD6 E17
PCI_AD7 A17
PCI_AD8 A15
PCI_AD9 C14
PCI_AD10 E14
PCI_AD11 D14
PCI_AD12 B12
PCI_AD13 C13
PCI_AD14 G15
PCI_AD15 G13
PCI_AD16 E12
PCI_AD17 C11
PCI_AD18 D11
PCI_AD19 A11
PCI_AD20 A10
PCI_AD21 F11
PCI_AD22 F10
PCI_AD23 E9
PCI_AD24 D9
PCI_AD25 B9
PCI_AD26 A8
PCI_AD27 A6
PCI_AD28 C7
PCI_AD29 B6
PCI_AD30 E6
PCI_AD31 D6
REQ0# D7
GNT0# E7
REQ1# C16
GNT1# D16
REQ2# C17
GNT2# D17
REQ3# E13
GNT3# F13
REQ4#/GPIO22 A13
GNT4#/GPIO48 A14
GPIO1/REQ5# C8
GPIO17/GNT5# D8
PCI_REQ#0 25
PCI_REQ#1 25,36
PCI_GNT#1 36
PCI_REQ#2 25
PCI_REQ#3 25
PCI_REQ#4 25
PCI_GNT#4
PCI_REQ#5 25
PCI_GNT#5
TPC28T 1 T2401
TPC28T 1 T2402
TPC28T 1 T2403
TPC28T 1 T2439
TPC28T 1 T2438
C/BE0# B15
C/BE1# C12
C/BE2# D12
C/BE3# C15
PCI_C/BE#0 36
PCI_C/BE#1 36
PCI_C/BE#2 36
PCI_C/BE#3 36
IRDY# A7
PAR E10
PCIRST# B18
DEVSEL# A12
PERR# C9
PLOCK# E11
SERR# B10
STOP# F15
TRDY# F14
FRAME# F16
PCI_IRDY# 25,36
PCI_PAR 36
PCI_RST# 31,42
PCI_DEVSEL# 25,36
PCI_PERR# 25,36
PCI_LOCK# 25
PCI_SERR# 25,36
PCI_STOP# 25,36
PCI_TRDY# 25,36
PCI_FRAME# 25,36
PLTRST# C26
PCICLK A9
PME# B19
PLT_RST# 25,30,33,42,44
CLK_ICHPCI 5
PCI_PME# 36
Interrupt I/F
25 PCI_INTA# A3
25,36 PCI_INTB# B4
25,36 PCI_INTC# C5
25,36 PCI_INTD# B5
PIRQA# PIRQB# PIRQC# PIRQD#
GPIO2/PIRQE# G8
GPIO3/PIRQF# F7
GPIO4/PIRQG# F8
GPIO5/PIRQH# G7
PCI_INTE# 25
PCI_INTF# 25
PCI_INTG# 25
PCI_INTH# 25
MISC
T2404 T2406 T2408 T2410 T2412 TPC28T AE5 AD5 AG4 AH4 AD9
RSVD_1 RSVD_2 RSVD_3 RSVD_4 RSVD_5
RSVD_6 RSVD_7 RSVD_8 RSVD_9 MCH_SYNC#
AE9 AG8 AH8 F21 AH20
TPC28T T2405 T2407 T2409 T2411
MCH_ICH_SYNC# 7
ICH7M
CLK_ICHPCI
C2401 10PF/50V c0402 @
GND
ICH7-M BOOT BIOS select
GNT#5 GNT#4
LPC 11 1 1 (default)
PCI 10 1 0
SPI 01 0 1
U2301D
PCI-Express
Direct Media Interface
SPI
USB
31 PCIE_RXN1_SB
31 PCIE_RXP1_SB
31 PCIE_RXN1_LAN
31 PCIE_RXP1_LAN
C2402 0.1UF/10V
C2403 0.1UF/10V
PCIE_TXN1_SB
PCIE_TXP1_SB
PERn1 F26
PERp1 F25
PETn1 E28
PETp1 E27
PERn2 H26
PERp2 H25
PETn2 G28
PETp2 G27
PERn3 K26
PERp3 K25
PETn3 J28
PETp3 J27
PERn4 M26
PERp4 M25
PETn4 L28
PETp4 L27
PERn5 P26
PERp5 P25
PETn5 N28
PETp5 N27
PERn6 T25
PERp6 T24
PETn6 R28
PETp6 R27
DMI0RXN V26
DMI0RXP V25
DMI0TXN U28
DMI0TXP U27
DMI1RXN Y26
DMI1RXP Y25
DMI1TXN W28
DMI1TXP W27
DMI2RXN AB26
DMI2RXP AB25
DMI2TXN AA28
DMI2TXP AA27
DMI3RXN AD25
DMI3RXP AD24
DMI3TXN AC28
DMI3TXP AC27
DMI_RXN0 7
DMI_RXP0 7
DMI_TXN0 7
DMI_TXP0 7
DMI_RXN1 7
DMI_RXP1 7
DMI_TXN1 7
DMI_TXP1 7
DMI_RXN2 7
DMI_RXP2 7
DMI_TXN2 7
DMI_TXP2 7
DMI_RXN3 7
DMI_RXP3 7
DMI_TXN3 7
DMI_TXP3 7
39 PCIE_TXN4_MINICARD
39 PCIE_TXP4_MINICARD
39 PCIE_RXN4_MINICARD
39 PCIE_RXP4_MINICARD
C2408 0.1UF/10V
C2409 0.1UF/10V
PCIE_TXN4_SB
PCIE_TXP4_SB
DMI_CLKN AE28
DMI_CLKP AE27
CLK_PCIE_ICH# 5
CLK_PCIE_ICH 5
DMI_ZCOMP C25
DMI_IRCOMP D25
+1.5VS_PCIE_ICH
R2409 24.9Ohm 1%
Place R2409 within 500mils of ICH-7
SPI_CLK
SPI_CS#
SPI_ARB
SPI_MOSI
SPI_MISO
+3VSUS
USBP0N F1
USBP0P F2
USBP1N G4
USBP1P G3
USBP2N H1
USBP2P H2
USBP3N J4
USBP3P J3
USBP4N K1
USBP4P K2
USBP5N L4
USBP5P L5
USBP6N M1
USBP6P M2
USBP7N N4
USBP7P N3
USB_PN0_B 40
USB_PP0_B 40
USB_PN1_B 40
USB_PP1_B 40
USB_PN2_B 40
USB_PP2_B 40
USB_PN3_B 40
USB_PP3_B 40
USB_PN5_B 41
USB_PP5_B 41
USB_PN6_B 18
USB_PP6_B 18
TPC28T T2425
TPC28T T2427
TPC28T T2428
TPC28T T2429
RN2401A RN2401B RN2401C RN2401D RN2402A RN2402B RN2402C RN2402D 10KOhm
USB_OC_0# USB_OC_1# USB_OC_2# USB_OC_3# USB_OC_4# USB_OC_5# USB_OC_6# USB_OC_7#
OC0# D3
OC1# C4
OC2# D5
OC3# D4
OC4# E5
OC5#/GPIO29 C3
OC6#/GPIO30 A2
OC7#/GPIO31 B3
USBRBIAS# D2
USBRBIAS D1
R2412 22.6Ohm 1%
GND
ICH7M
<Variant Name>
Title : ICH7-M (2/4)
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 24 of 63


U2301C
ICH7M
SMB
SATA GPIO
Clocks
Power MGT
SYS GPIO
GPIO
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
SMBALERT#/GPIO11
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39
BT_LED_EN#
CLK_ICH14
CLK_USB48
SUS_CLK
SUSB#
SUSC#
PM_DPRSLPVR
PM_BATLOW#
PM_PWRBTN#
LANRST#
PM_RSMRST#
SIO_SMI#
PD_UNDOCK#
802_LED_EN#
CB_SD#
PCB_ID1
PCB_ID2
ICH7_PWROK
Reference ICH7 EDS page 69:LAN_RST# should be tied to RSMRST#
Note: GPIO25 CAN NOT BE LOW for 35uS after RSMRST on BOOT (DMI AC coupling mode strap)
PCB_VID3 : PROJECT CODE
PCB_VID 0 1 2
MB V1.0 0 0 0
<Variant Name>
Title : ICH7-M (3/4)
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 25 of 63

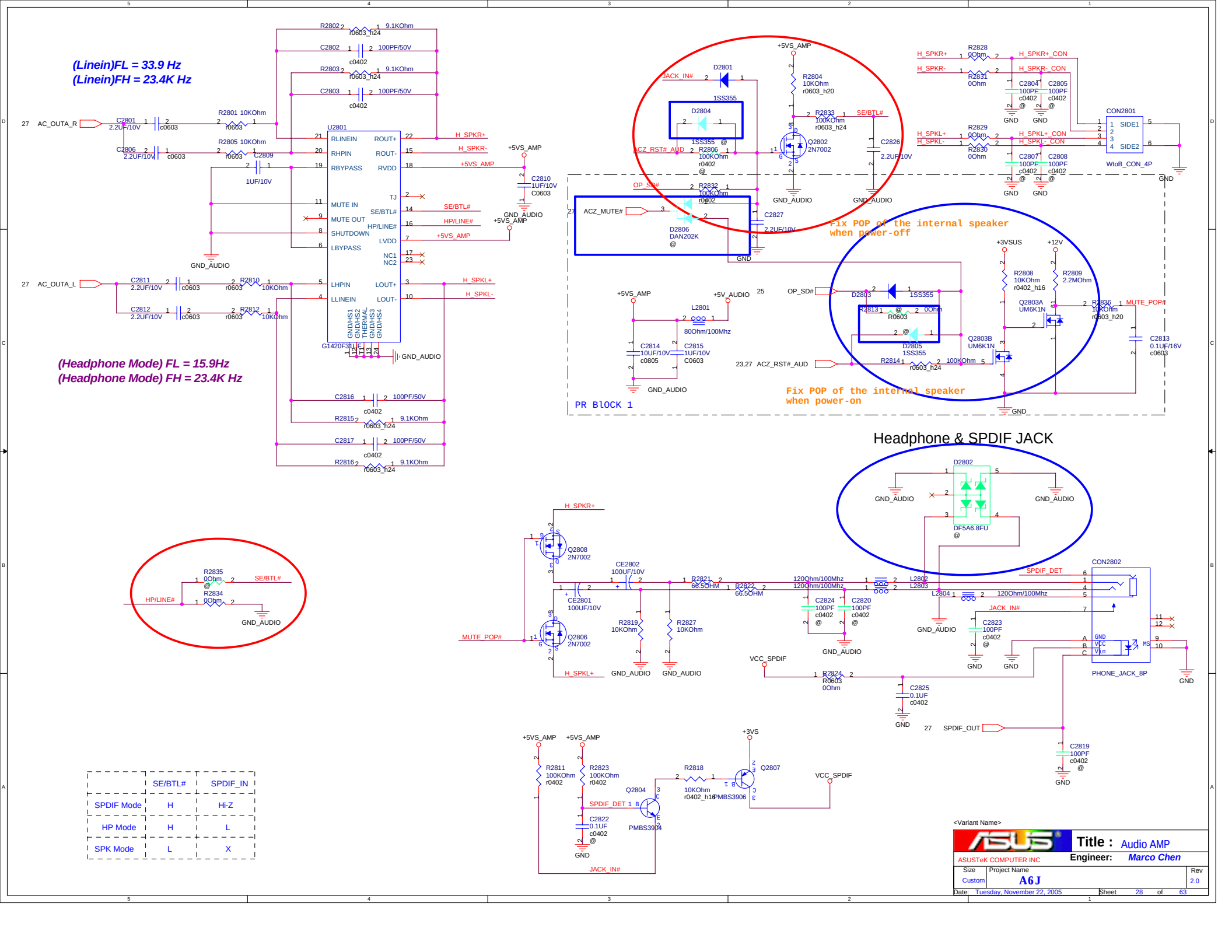

U2301E
U2301F
ICH7M
Title : ICH7-M (4/4)
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size: Custom
Project Name: A6J
Rev: 2.0
Date: Tuesday, November 22, 2005
Sheet 26 of 63
<Variant Name>
+3VS
+5VS
+5VSUS
+1.5VS
+VCCP_ICH
+VCCP
+3VSUS
+VCC_RTC
+5VS_REF_ICH
+5VSUS_ICH
+1.5VS_PCIE_ICH
+1.5V_DMIPLL_ICH
1.27A
0.04A
0.44A
0.74A
0.97A
390mA
CORE
VCCPAUX
VCCA3GP
IDE
PCI
USB
ARX
ATX
USB CORE

Place U2802near U2801



<variant_name>

ASUSTek COMPUTER INC. NB1	Title : AZALIA ALC880	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6J	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 27 of 63	



	SE/BTL#	SPDIF_IN
SPDIF Mode	H	Hi-Z
HP Mode	H	L
SPK Mode	L	X

<Variant Name>

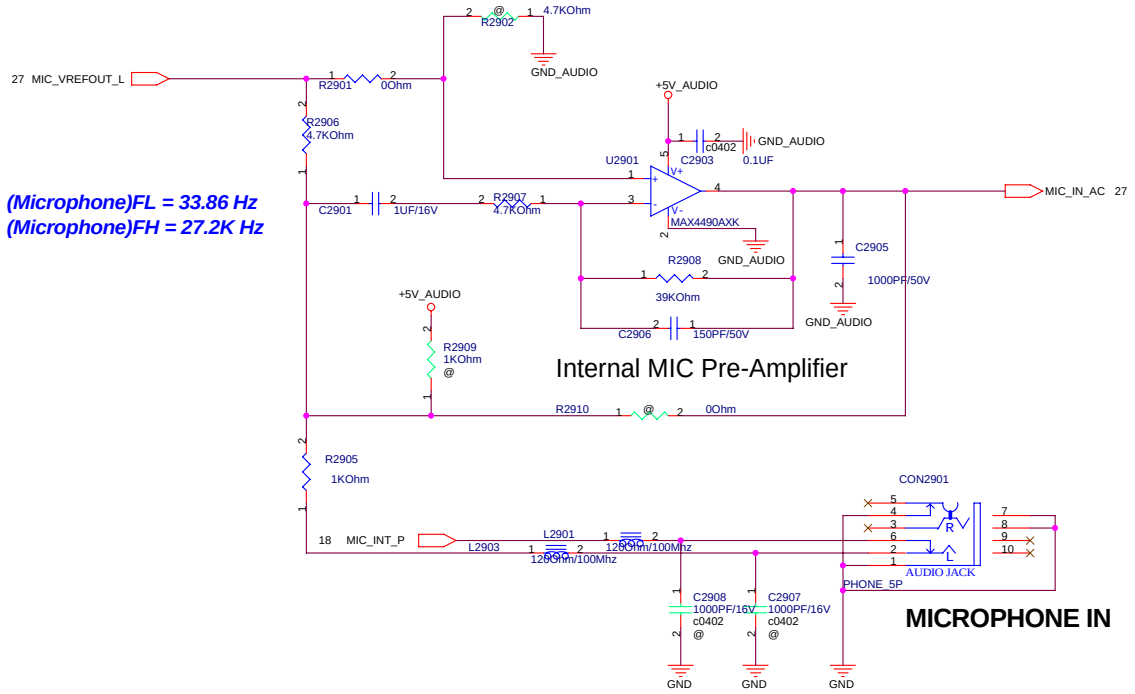
ASUSTeK COMPUTER INC

Title : Audio AMP

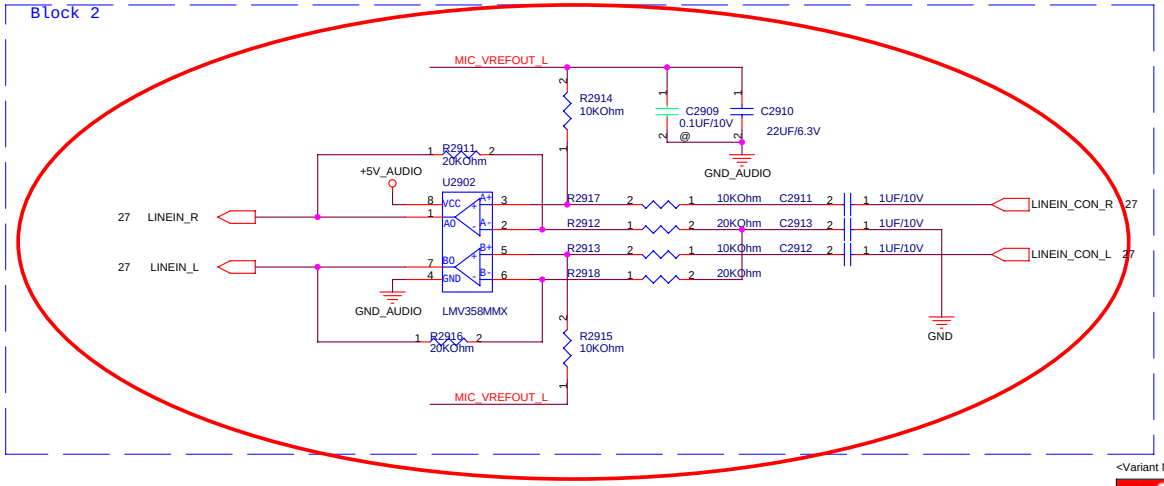
Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 28 of 63

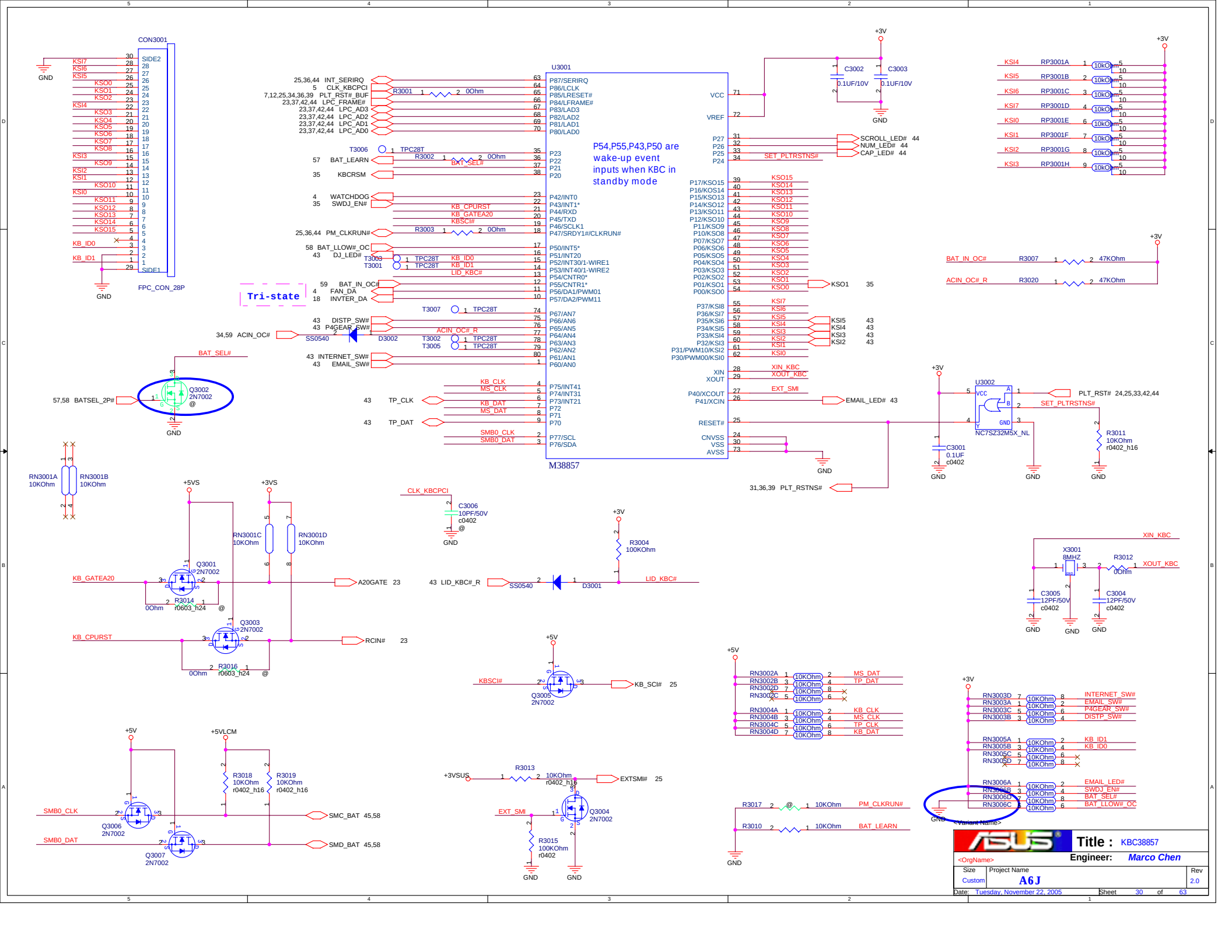


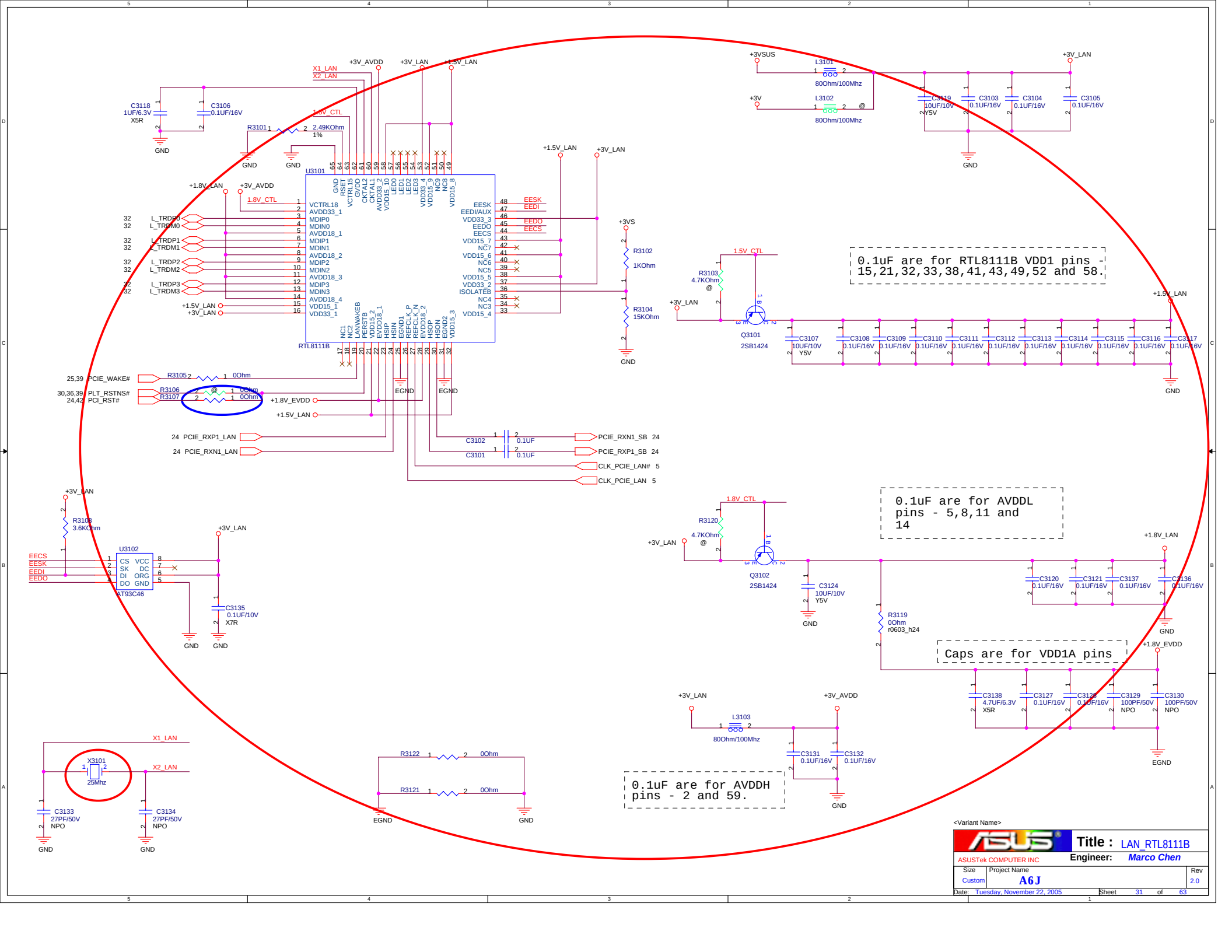
(Microphone)FL = 33.86 Hz
(Microphone)FH = 27.2K Hz



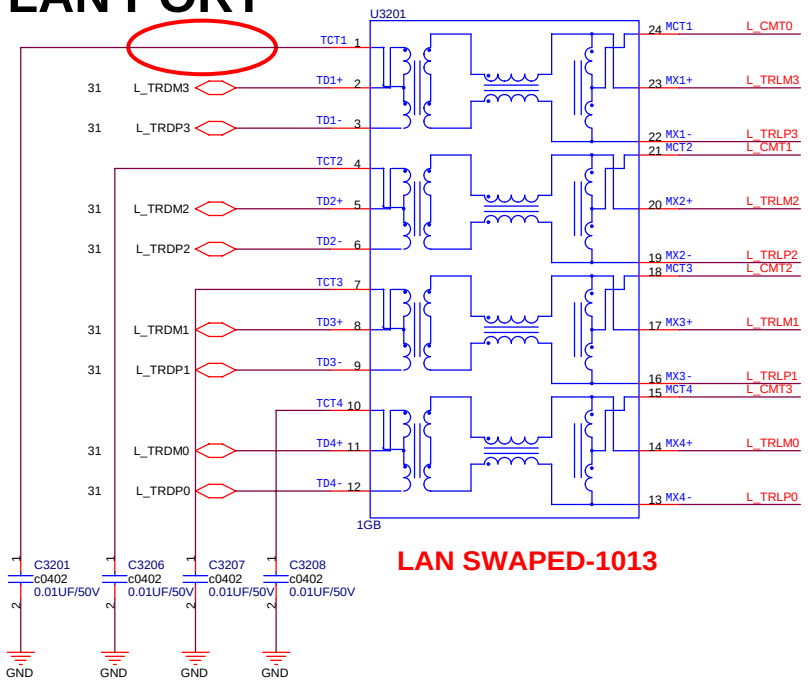
<Variant Name>

ASUSTeK COMPUTER INC	Title : MICROPHONE	
	Engineer: *Marco Chen*	
Size: Custom	Project Name: A6J	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 29 of 63	

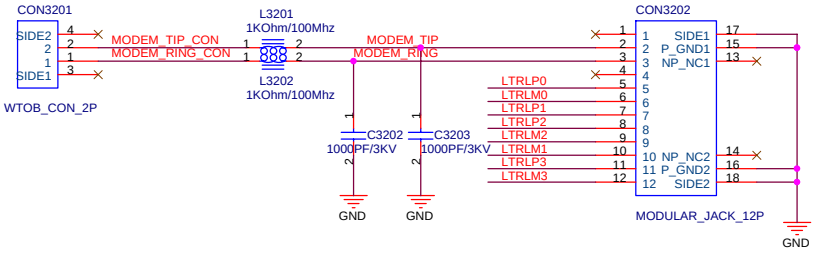

CON3001
FPC_CON_28P
U3001
M38857
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
Tri-state
Q3002 2N7002
Q3001 2N7002
Q3003 2N7002
Q3005 2N7002
Q3004 2N7002
Q3006 2N7002
Q3007 2N7002
RN3001A 10KOhm
RN3001B 10KOhm
RN3001C 10KOhm
RN3001D 10KOhm
C3002 0.1UF/10V
C3003 0.1UF/10V
C3001 0.1UF c0402
C3004 12PF/50V c0402
C3005 12PF/50V c0402
C3006 10PF/50V c0402
X3001 8MHZ
NC7SZ32M5X_NL
R3001 0Ohm
R3002 0Ohm
R3003 0Ohm
R3004 100KOhm
R3011 10KOhm r0402_h16
R3012 0Ohm
R3013 10KOhm r0402_h16
R3014 0Ohm r0603_h24
R3015 100KOhm r0402
R3016 0Ohm r0603_h24
R3017 10KOhm
R3018 10KOhm r0402_h16
R3019 10KOhm r0402_h16
R3020 47KOhm
R3007 47KOhm
SS0540
D3001
D3002
T3001 TPC28T
T3002 TPC28T
T3003 TPC28T
T3005 TPC28T
T3006 TPC28T
T3007 TPC28T
RP3001A 10KOhm
RP3001B 10KOhm
RP3001C 10KOhm
RP3001D 10KOhm
RP3001E 10KOhm
RP3001F 10KOhm
RP3001G 10KOhm
RP3001H 10KOhm
RN3002A 10KOhm
RN3002B 10KOhm
RN3002C 10KOhm
RN3002D 10KOhm
RN3003A 10KOhm
RN3003B 10KOhm
RN3003C 10KOhm
RN3003D 10KOhm
RN3004A 10KOhm
RN3004B 10KOhm
RN3004C 10KOhm
RN3004D 10KOhm
RN3005A 10KOhm
RN3005B 10KOhm
RN3005C 10KOhm
RN3005D 10KOhm
RN3006A 10KOhm
RN3006B 10KOhm
RN3006C 10KOhm
RN3006D 10KOhm
+3V
+5V
+3VS
+5VS
+5VLCM
+3VSUS
GND
BAT_SEL#
CLK_KBCPCI
XIN_KBC
XOUT_KBC
KB_GATEA20
KB_CPURST
KBSCI#
LID_KBC#
EXTSMI# 25
KB_SCI# 25
A20GATE 23
RCIN# 23
SMC_BAT 45,58
SMD_BAT 45,58
SMB0_CLK
SMB0_DAT
ACIN_OC#_R
EXT_SMI
PM_CLKRUN#
BAT_LEARN
PLT_RST# 24,25,33,42,44
SET_PLTRSTNS#
EMAIL_LED# 43
PLT_RSTNS# 31,36,39
SCROLL_LED# 44
NUM_LED# 44
CAP_LED# 44
Title : KBC38857
Engineer: Marco Chen
<OrgName>
Project Name A6J
Size Custom
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 30 of 63

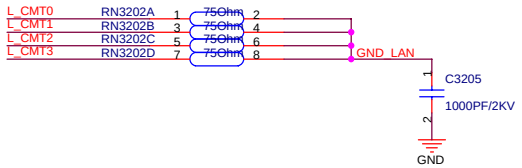

U3101
RTL8111B
U3102
AT93C46
Q3101
2SB1424
Q3102
2SB1424
X3101
25Mhz
L3101
L3102
L3103
80Ohm/100Mhz
0.1uF are for RTL8111B VDD1 pins - 15,21,32,33,38,41,43,49,52 and 58.
0.1uF are for AVDDL pins - 5,8,11 and 14
Caps are for VDD1A pins
0.1uF are for AVDDH pins - 2 and 59.
Title : LAN_RTL8111B
ASUSTek COMPUTER INC
Engineer: Marco Chen
Project Name A6J
Size Custom
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 31 of 63
<Variant Name>

LAN PORT

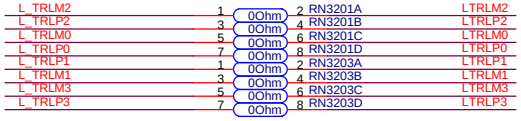


LAN SWAPED-1013

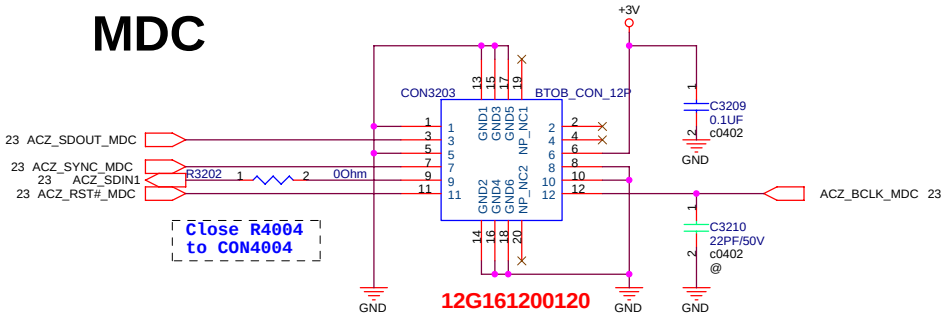




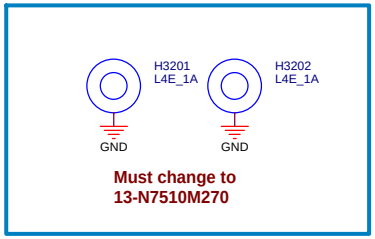
FOR EMI



MDC



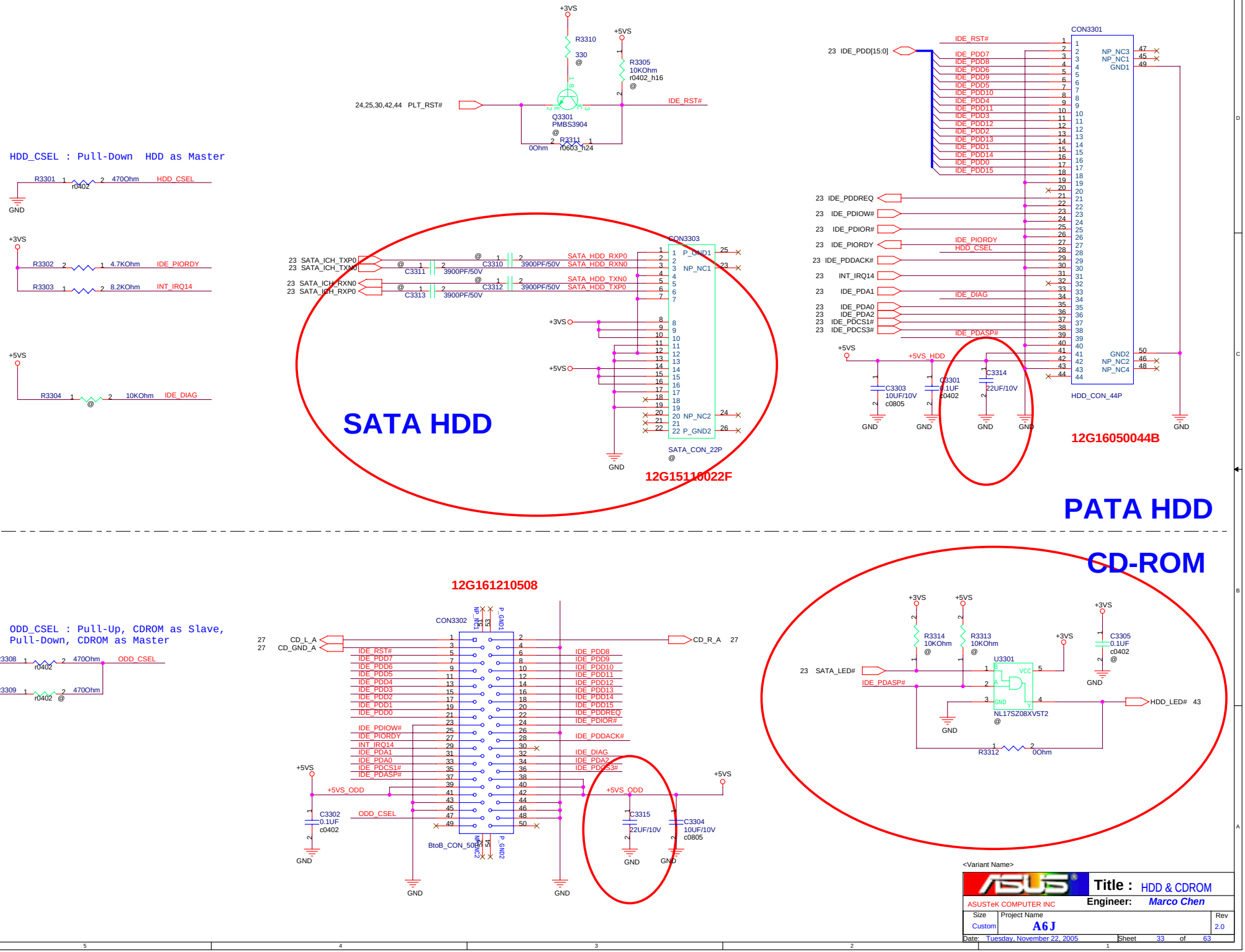
12G161200120

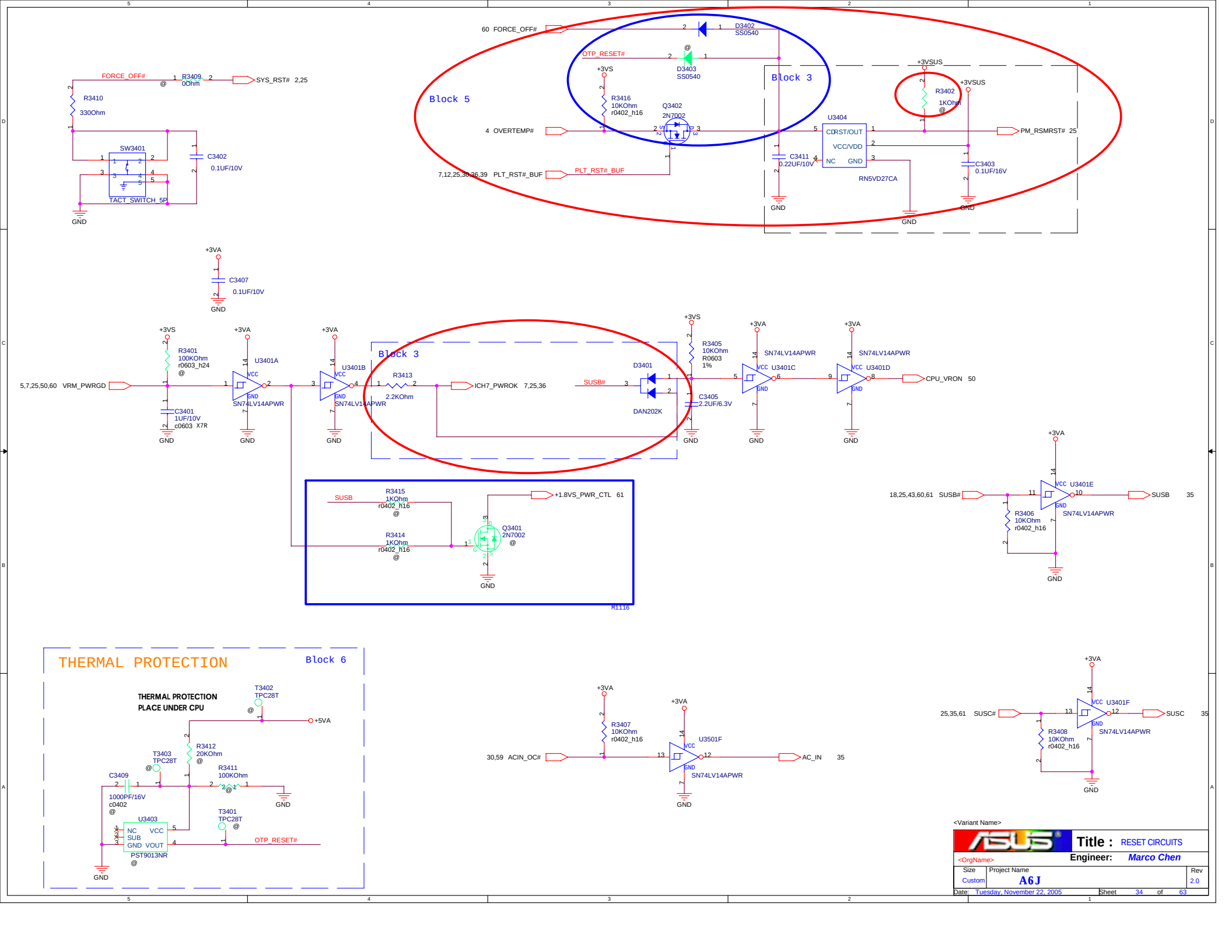


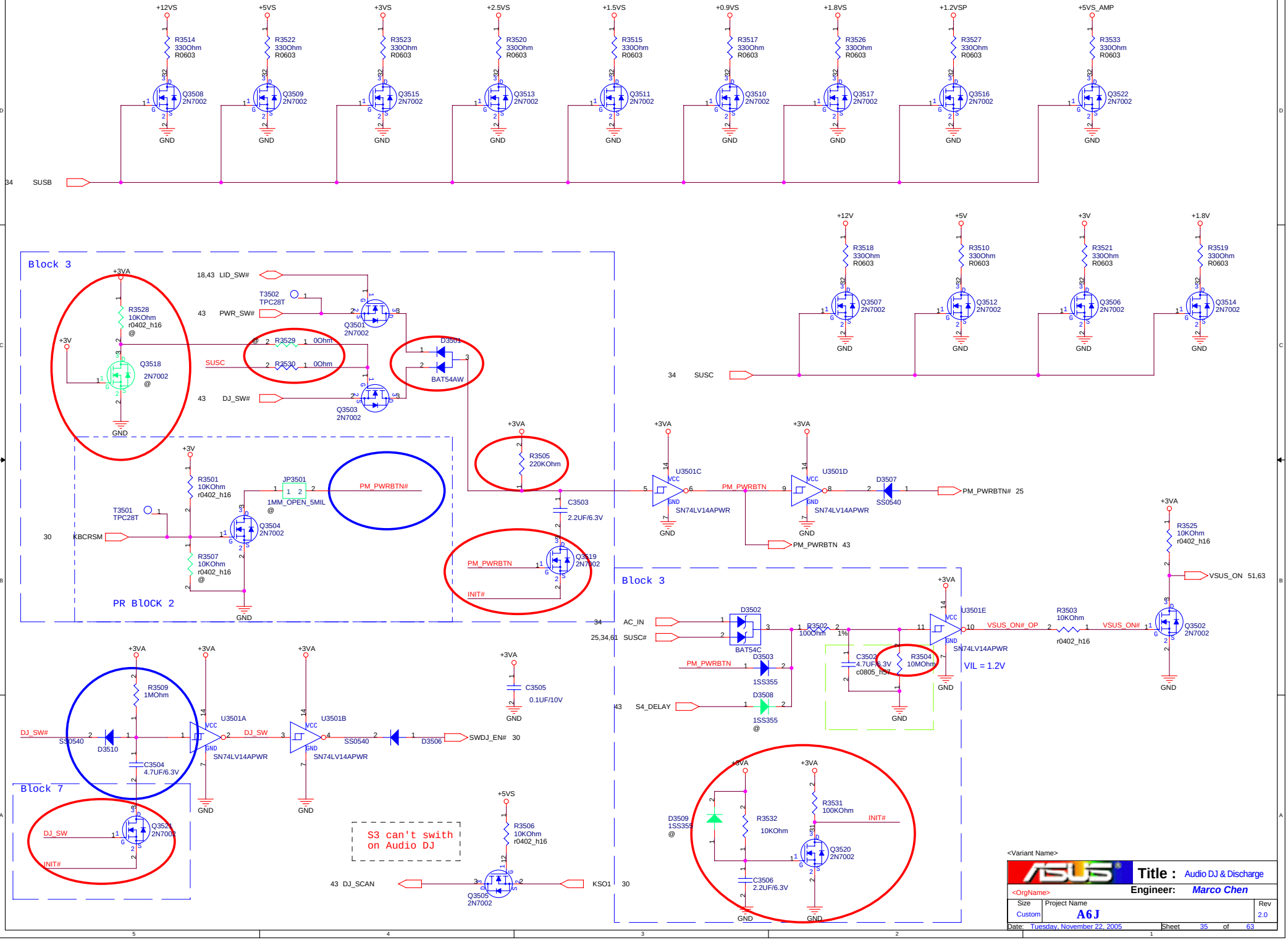
Must change to 13-N7510M270

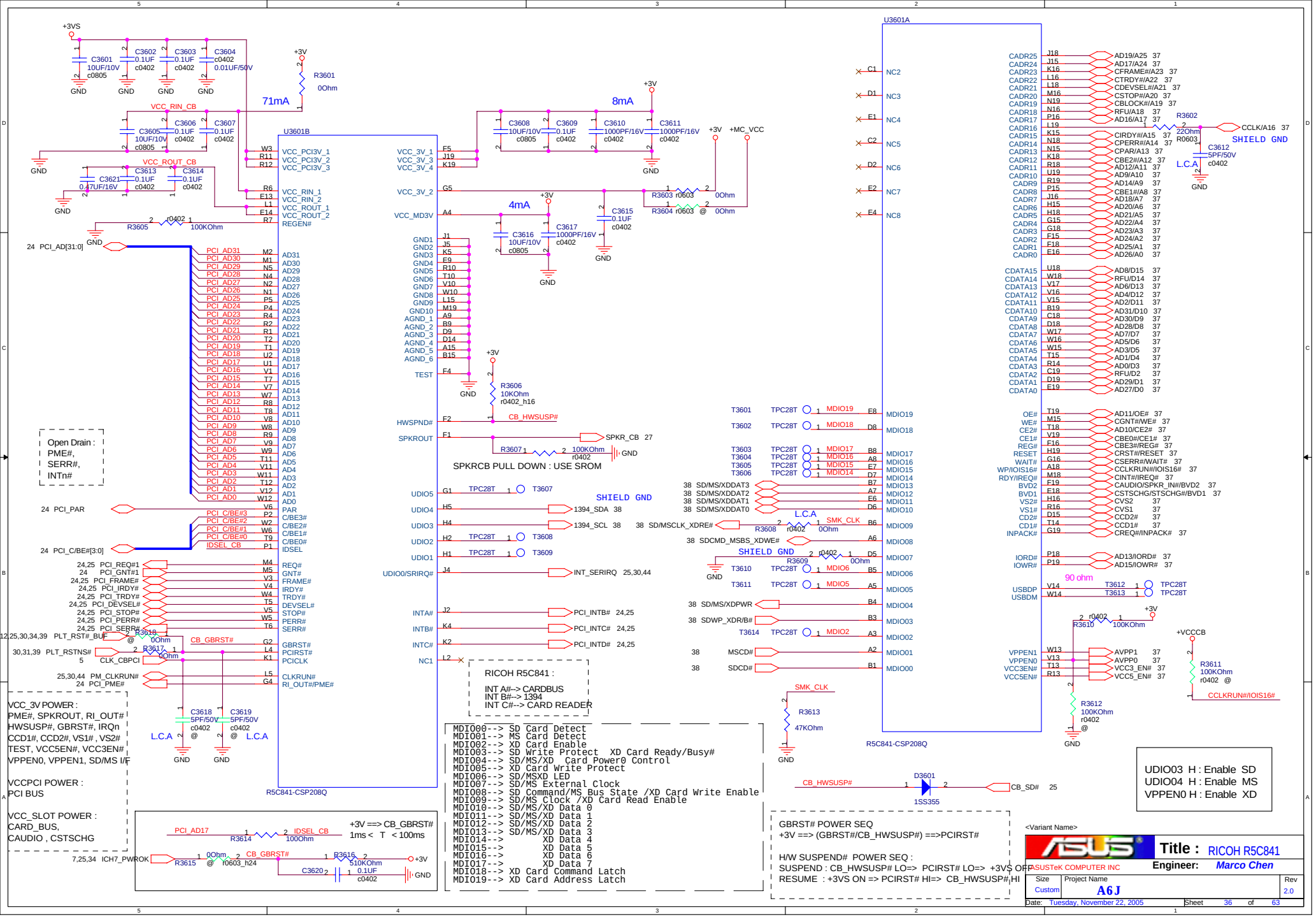
<Variant Name>

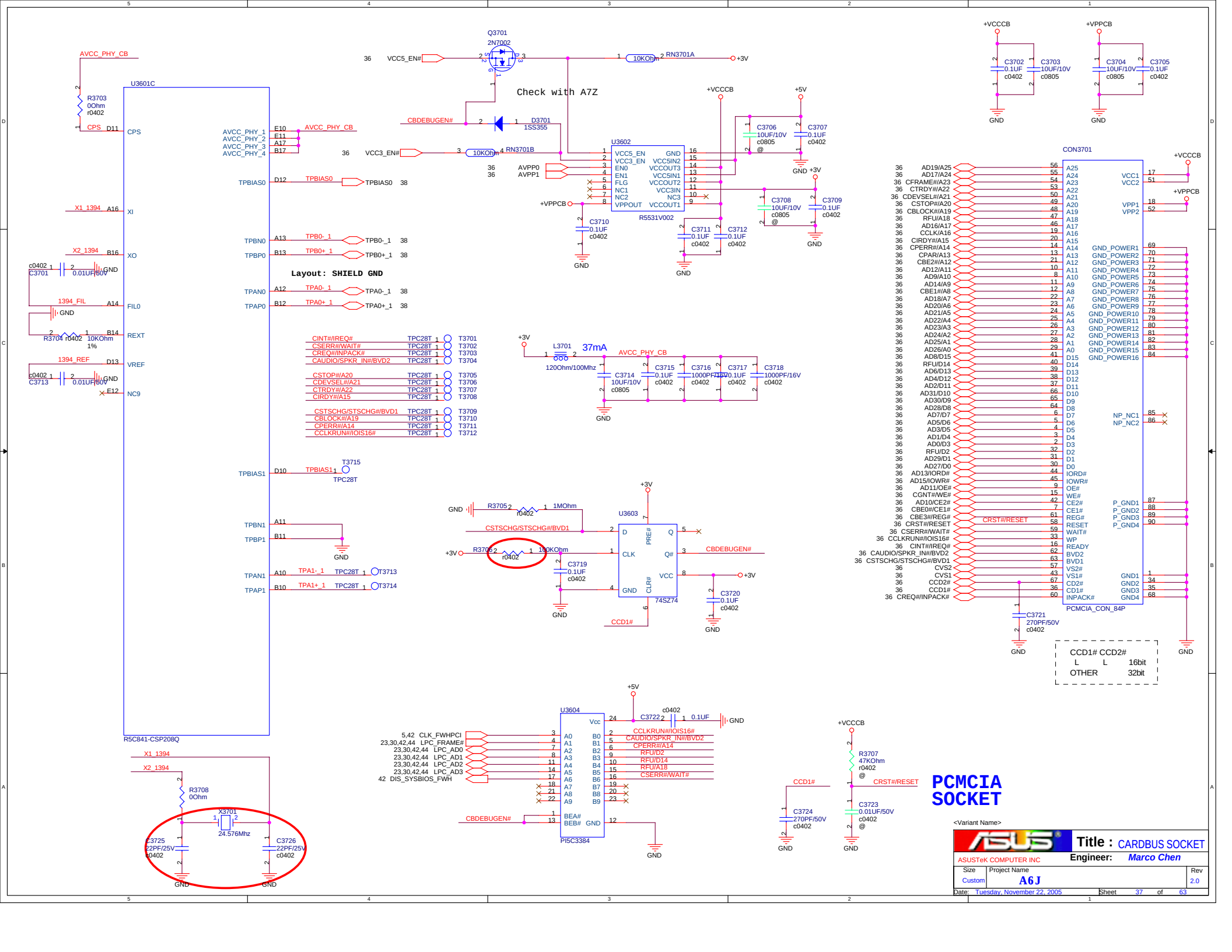
ASUSTeK COMPUTER INC	Title : RJ11+45,MDC	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6J	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 32 of 63	

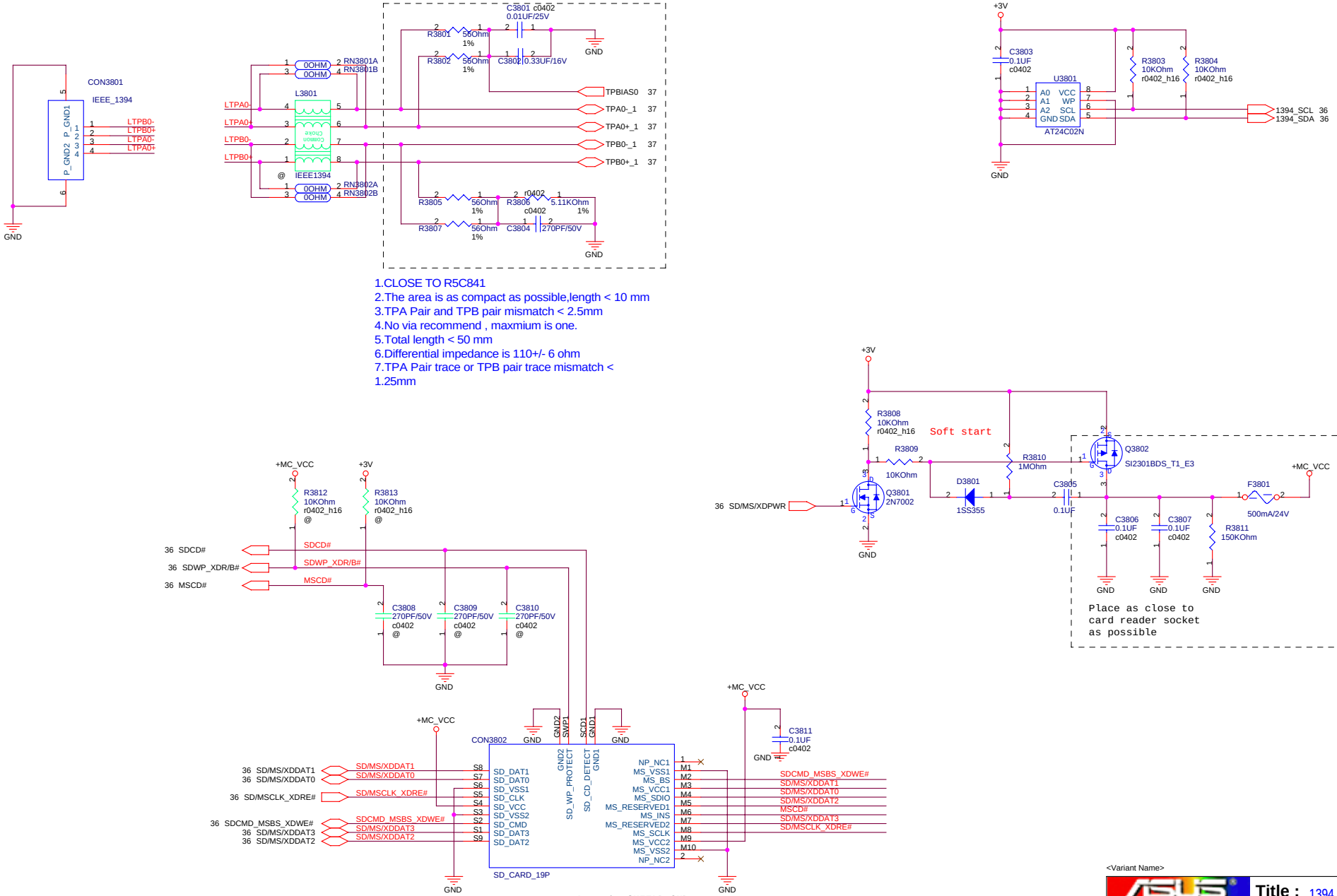

HDD_CSEL : Pull-Down HDD as Master
R3301 r0402 470Ohm HDD_CSEL
R3302 4.7KOhm IDE_PIORDY
R3303 8.2KOhm INT_IRQ14
R3304 @ 10KOhm IDE_DIAG
+3VS
+5VS
GND
R3310 330 @
R3305 10KOhm r0402_h16 @
24,25,30,42,44 PLT_RST#
IDE_RST#
Q3301 PMBS3904 @
R3311 0Ohm r0603_h24
SATA HDD
CON3303
SATA_CON_22P @
SATA_ICH_TXP0
SATA_ICH_TXN0
SATA_ICH_RXN0
SATA_ICH_RXP0
C3310 C3311 C3312 C3313 3900PF/50V
SATA_HDD_RXP0
SATA_HDD_RXN0
SATA_HDD_TXN0
SATA_HDD_TXP0
P_GND1
NP_NC1
NP_NC2
P_GND2
12G15110022F
PATA HDD
CON3301
HDD_CON_44P
IDE_PDD[15:0]
IDE_PDDREQ
IDE_PDIOW#
IDE_PDIOR#
IDE_PIORDY
IDE_PDDACK#
INT_IRQ14
IDE_PDA1
IDE_PDA0
IDE_PDA2
IDE_PDCS1#
IDE_PDCS3#
IDE_PDASP#
IDE_DIAG
+5VS_HDD
C3303 10UF/10V c0805
C3301 0.1UF c0402
C3314 22UF/10V
NP_NC3
NP_NC4
GND1
GND2
12G16050044B
CD-ROM
ODD_CSEL : Pull-Up, CDROM as Slave, Pull-Down, CDROM as Master
R3308 r0402 470Ohm ODD_CSEL
R3309 r0402 @ 470Ohm
12G161210508
CON3302
BtoB_CON_50P
CD_L_A
CD_GND_A
CD_R_A
IDE_RST#
IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
IDE_PDDREQ
IDE_PDIOR#
IDE_PDIOW#
IDE_PDDACK#
IDE_PDASP#
+5VS_ODD
C3302 0.1UF c0402
C3315 22UF/10V
C3304 10UF/10V c0805
R3314 10KOhm @
R3313 10KOhm @
C3305 0.1UF c0402 @
U3301
NL17SZ08XV5T2 @
SATA_LED#
HDD_LED#
R3312 0Ohm
<Variant Name>
Title : HDD & CDROM
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 33 of 63

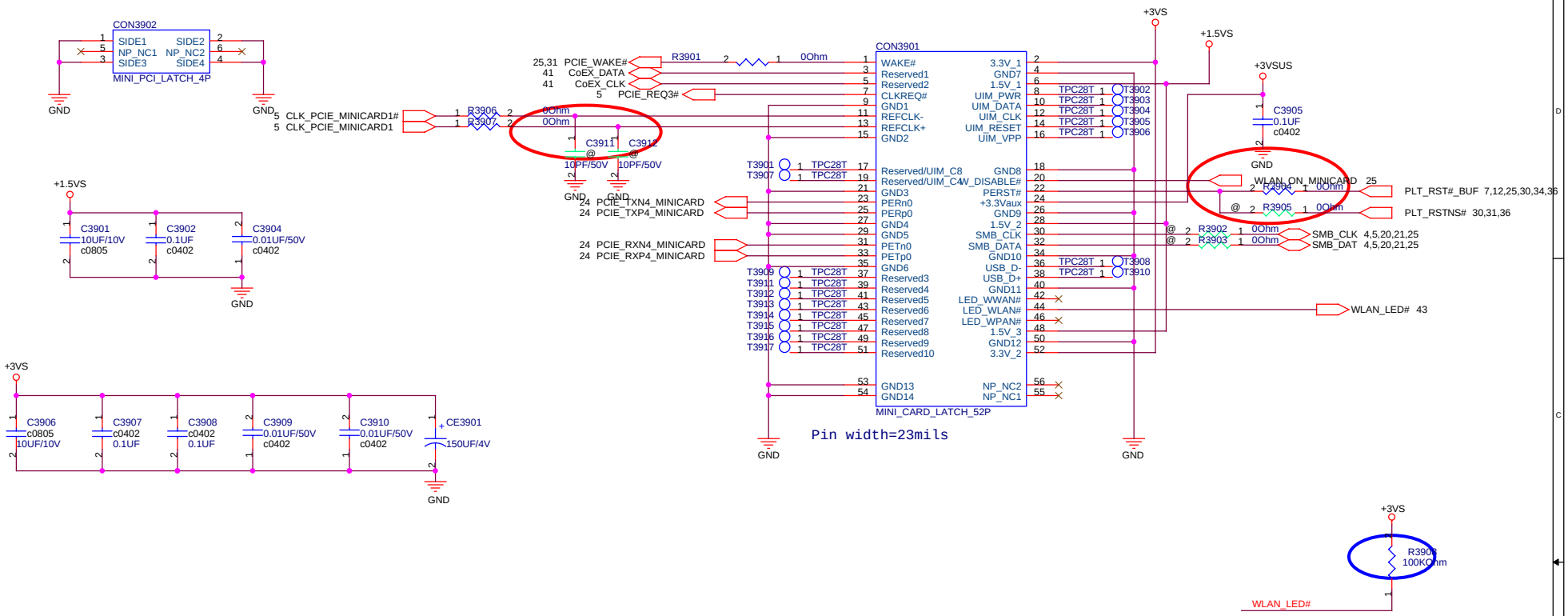

FORCE_OFF#
R3409
0Ohm
SYS_RST# 2,25
R3410
330Ohm
SW3401
TACT_SWITCH_5P
C3402
0.1UF/10V
GND
60 FORCE_OFF#
D3402
SS0540
OTP_RESET#
D3403
SS0540
Block 5
Block 3
+3VS
R3416
10KOhm
r0402_h16
Q3402
2N7002
4 OVERTEMP#
7,12,25,36,39 PLT_RST#_BUF
PLT_RST#_BUF
+3VSUS
R3402
1KOhm
U3404
CRST/OUT
VCC/VDD
NC GND
RN5VD27CA
C3411
0.22UF/10V
C3403
0.1UF/16V
PM_RSMRST# 25
+3VA
C3407
0.1UF/10V
R3401
100KOhm
r0603_h24
C3401
1UF/10V
c0603 X7R
U3401A
U3401B
SN74LV14APWR
5,7,25,50,60 VRM_PWRGD
R3413
2.2KOhm
ICH7_PWROK 7,25,36
SUSB#
D3401
DAN202K
R3405
10KOhm
R0603
1%
C3405
2.2UF/6.3V
U3401C
U3401D
CPU_VRON 50
R3415
1KOhm
r0402_h16
R3414
1KOhm
r0402_h16
Q3401
2N7002
+1.8VS_PWR_CTL 61
M1116
18,25,43,60,61 SUSB#
U3401E
R3406
10KOhm
r0402_h16
SUSB 35
THERMAL PROTECTION
Block 6
THERMAL PROTECTION
PLACE UNDER CPU
T3402
TPC28T
+5VA
R3412
20KOhm
T3403
TPC28T
R3411
100KOhm
C3409
1000PF/16V
c0402
U3403
NC
SUB
GND
VCC
VOUT
PST9013NR
T3401
TPC28T
OTP_RESET#
30,59 ACIN_OC#
R3407
10KOhm
r0402_h16
U3501F
AC_IN 35
25,35,61 SUSC#
U3401F
R3408
10KOhm
r0402_h16
SUSC 35
<Variant Name>
Title : RESET CIRCUITS
<OrgName>
Engineer: Marco Chen
Size
Custom
Project Name
A6J
Rev
2.0
Date: Tuesday, November 22, 2005
Sheet 34 of 63


+12VS
+5VS
+3VS
+2.5VS
+1.5VS
+0.9VS
+1.8VS
+1.2VSP
+5VS_AMP
R3514 330Ohm R0603
R3522 330Ohm R0603
R3523 330Ohm R0603
R3520 330Ohm R0603
R3515 330Ohm R0603
R3517 330Ohm R0603
R3526 330Ohm R0603
R3527 330Ohm R0603
R3533 330Ohm R0603
Q3508 2N7002
Q3509 2N7002
Q3515 2N7002
Q3513 2N7002
Q3511 2N7002
Q3510 2N7002
Q3517 2N7002
Q3516 2N7002
Q3522 2N7002
GND
34 SUSB
+12V
+5V
+3V
+1.8V
R3518 330Ohm R0603
R3510 330Ohm R0603
R3521 330Ohm R0603
R3519 330Ohm R0603
Q3507 2N7002
Q3512 2N7002
Q3506 2N7002
Q3514 2N7002
34 SUSC
Block 3
+3VA
+3V
18,43 LID_SW#
T3502 TPC28T
43 PWR_SW#
R3528 10KOhm r0402_h16 @
R3529 0Ohm
R3530 0Ohm
SUSC
43 DJ_SW#
Q3518 2N7002 @
Q3501 2N7002
Q3503 2N7002
D3501
BAT54AW
R3505 220KOhm
C3503 2.2UF/6.3V
PR BLOCK 2
R3501 10KOhm r0402_h16
JP3501
1MM_OPEN_5MIL @
PM_PWRBTN#
T3501 TPC28T
30 KBCRSM
Q3504 2N7002
R3507 10KOhm r0402_h16 @
Q3519 2N7002
PM_PWRBTN
INIT#
U3501C
U3501D
SN74LV14APWR
PM_PWRBTN
D3507 SS0540
PM_PWRBTN# 25
PM_PWRBTN 43
Block 3
34 AC_IN
25,34,61 SUSC#
D3502 BAT54C
D3503 1SS355
D3508 1SS355 @
43 S4_DELAY
R3502 100Ohm 1%
C3502 4.7UF/6.3V c0805_h57
R3504 10MOhm
VIL = 1.2V
U3501E
VSUS_ON# OP
R3503 10KOhm r0402_h16
VSUS_ON#
R3525 10KOhm r0402_h16
VSUS_ON 51,63
Q3502 2N7002
R3509 1MOhm
U3501A
U3501B
DJ_SW#
SS0540
D3510
DJ_SW
C3504 4.7UF/6.3V
C3505 0.1UF/10V
D3506
SWDJ_EN# 30
Block 7
Q3521 2N7002
INIT#
S3 can't swith on Audio DJ
+5VS
R3506 10KOhm r0402_h16
43 DJ_SCAN
Q3505 2N7002
KSO1 30
D3509 1SS355 @
R3532 10KOhm
R3531 100KOhm
Q3520 2N7002
C3506 2.2UF/6.3V
<Variant Name>
Title : Audio DJ & Discharge
<OrgName>
Engineer: Marco Chen
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 35 of 63


U3601B
R5C841-CSP208Q
U3601A
R5C841-CSP208Q
71mA
8mA
4mA
SHIELD GND
L.C.A
SPKRCB PULL DOWN : USE SROM
Open Drain : PME#, SERR#, INTn#
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
VCC_3V POWER : PME#, SPKROUT, RI_OUT# HWSUSP#, GBRST#, IRQn CCD1#, CCD2#, VS1# , VS2# TEST, VCC5EN#, VCC3EN# VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER : PCI BUS
VCC_SLOT POWER : CARD_BUS, CAUDIO , CSTSCHG
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
+3V ==> CB_GBRST# 1ms < T < 100ms
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP#,HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
Title : RICOH R5C841
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 36 of 63

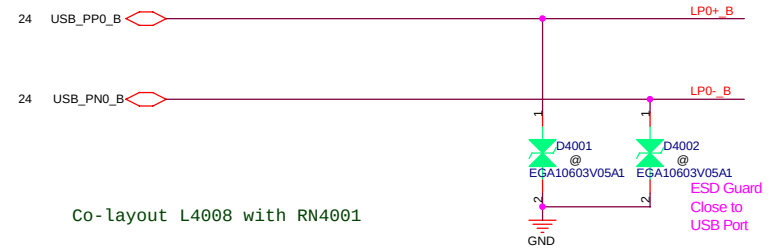

U3601C
R5C841-CSP208Q
Layout: SHIELD GND
Check with A7Z
Q3701
2N7002
D3701
1SS355
U3602
R5531V002
U3603
74SZ74
U3604
PI5C3384
CON3701
PCMCIA_CON_84P
PCMCIA SOCKET
CCD1# CCD2#
L L 16bit
OTHER 32bit
Title : CARDBUS SOCKET
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Project Name A6J
Date: Tuesday, November 22, 2005
Sheet 37 of 63


CON3801
IEEE_1394
P_GND1
P_GND2
LTPB0-
LTPB0+
LTPA0-
LTPA0+
GND
C3801 c0402
0.01UF/25V
R3801 56Ohm 1%
R3802 56Ohm 1%
C3802 0.33UF/16V
RN3801A 0OHM
RN3801B 0OHM
L3801
IEEE1394
RN3802A 0OHM
RN3802B 0OHM
TPBIAS0 37
TPA0-_1 37
TPA0+_1 37
TPB0-_1 37
TPB0+_1 37
R3805 56Ohm 1%
R3806 r0402 c0402 5.11KOhm 1%
R3807 56Ohm 1%
C3804 270PF/50V
+3V
C3803 0.1UF c0402
U3801
A0 A1 A2 GND VCC WP SCL SDA
AT24C02N
R3803 10KOhm r0402_h16
R3804 10KOhm r0402_h16
1394_SCL 36
1394_SDA 36
1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm
+MC_VCC
R3812 10KOhm r0402_h16 @
R3813 10KOhm r0402_h16 @
36 SDCD#
36 SDWP_XDR/B#
36 MSCD#
C3808 270PF/50V c0402 @
C3809 270PF/50V c0402 @
C3810 270PF/50V c0402 @
CON3802
SD_CARD_19P
GND2
SWP1
SCD1
GND1
SD_WP_PROTECT
SD_CD_DETECT
36 SD/MS/XDDAT1
36 SD/MS/XDDAT0
36 SD/MSCLK_XDRE#
36 SDCMD_MSBS_XDWE#
36 SD/MS/XDDAT3
36 SD/MS/XDDAT2
SD_DAT1
SD_DAT0
SD_VSS1
SD_CLK
SD_VCC
SD_VSS2
SD_CMD
SD_DAT3
SD_DAT2
NP_NC1
MS_VSS1
MS_BS
MS_VCC1
MS_SDIO
MS_RESERVED1
MS_INS
MS_RESERVED2
MS_SCLK
MS_VCC2
MS_VSS2
NP_NC2
C3811 0.1UF c0402
Layout: SHIELD GND
+3V
R3808 10KOhm r0402_h16
Soft start
R3809 10KOhm
R3810 1MOhm
Q3801 2N7002
D3801 1SS355
C3805 0.1UF
Q3802 SI2301BDS_T1_E3
F3801 500mA/24V
C3806 0.1UF c0402
C3807 0.1UF c0402
R3811 150KOhm
36 SD/MS/XDPWR
Place as close to card reader socket as possible
<Variant Name>
Title : 1394 & 3 IN 1 CON
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 38 of 63

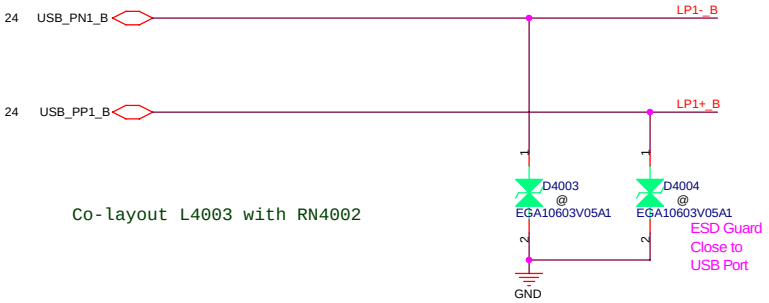


<Variant Name>

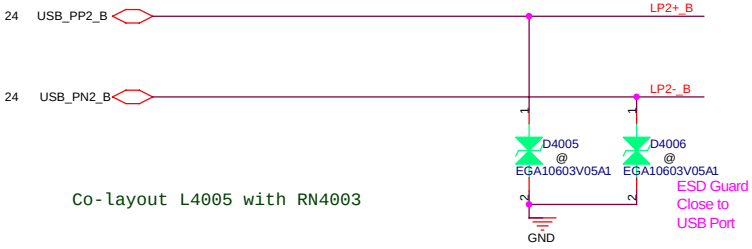
ASUSTeK COMPUTER INC	Title : MINICARD (Golan)	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6J	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 39 of 63	



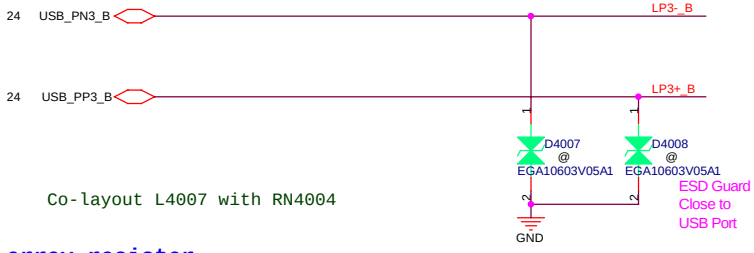
Co-layout L4008 with RN4001



Co-layout L4003 with RN4002

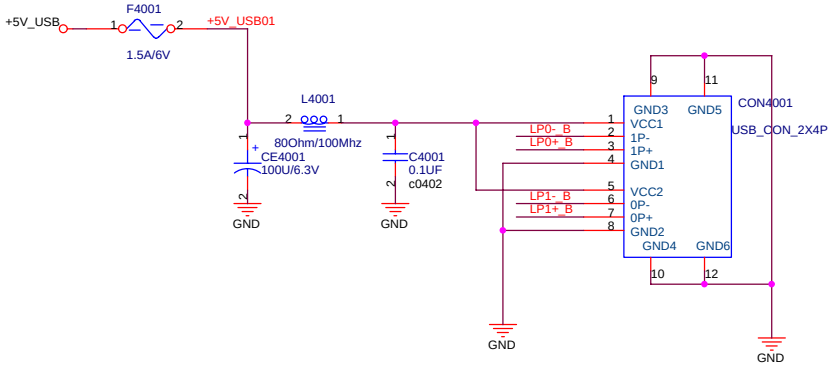


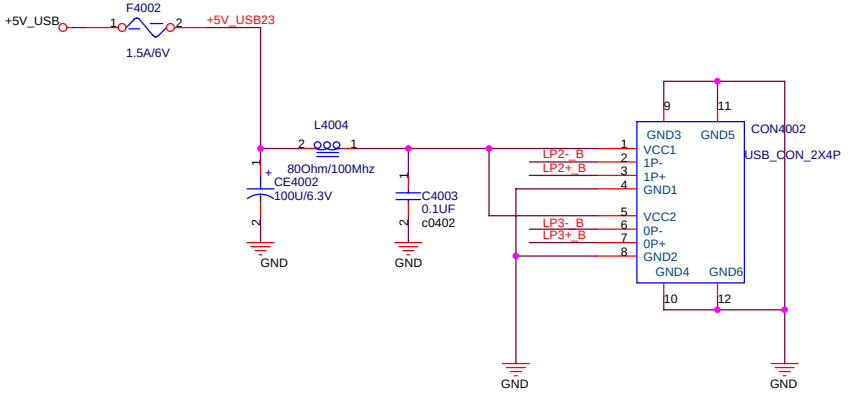
Co-layout L4005 with RN4003

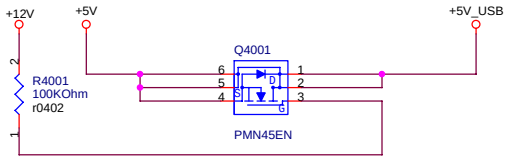


Co-layout L4007 with RN4004

4P2R array resister
co-layout with comman choke







<Variant Name>

ASUSTeK COMPUTER INC

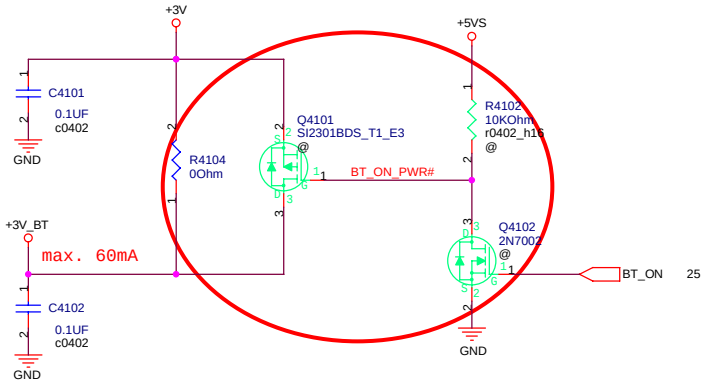
Title : USB CONN X 4

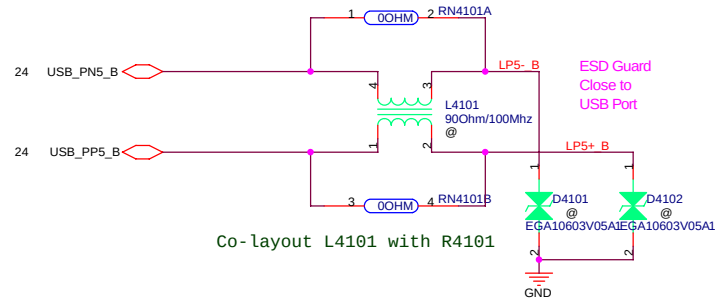
Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 40 of 63

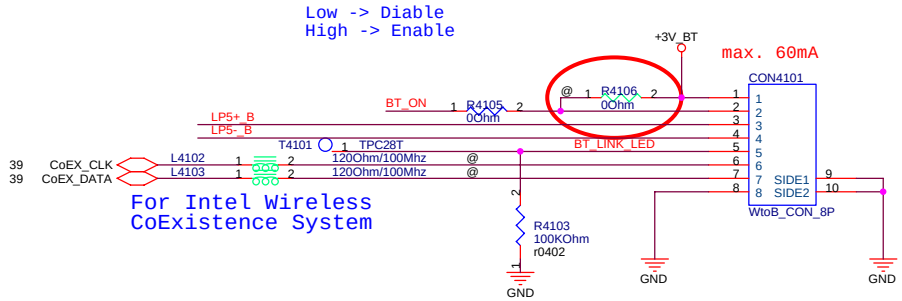
BT ON/OFF Control





Co-layout L4101 with R4101

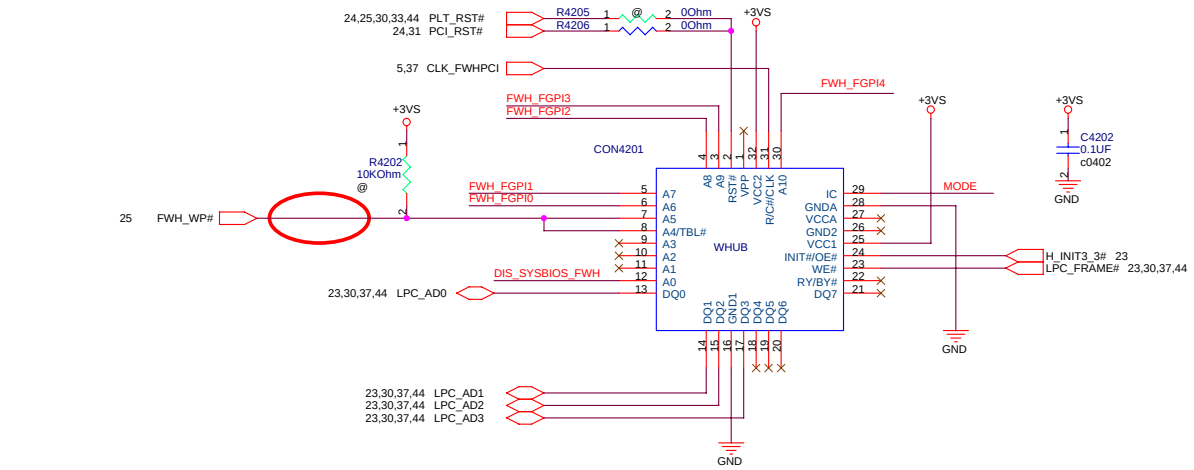
Bluetooth Module

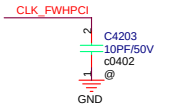


For Intel Wireless
CoExistence System

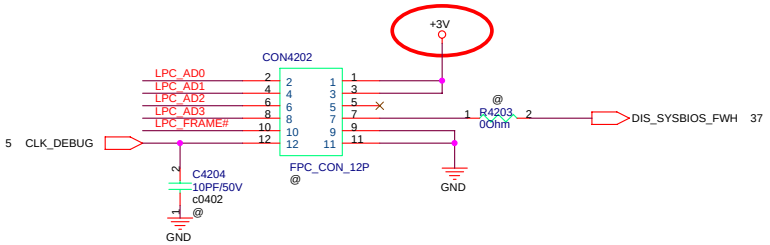
<Variant Name>

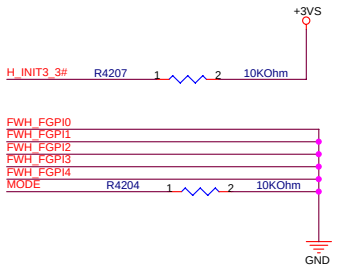
ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: *Marco Chen*	
Size: Custom	Project Name: A6J	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 41 of 63	





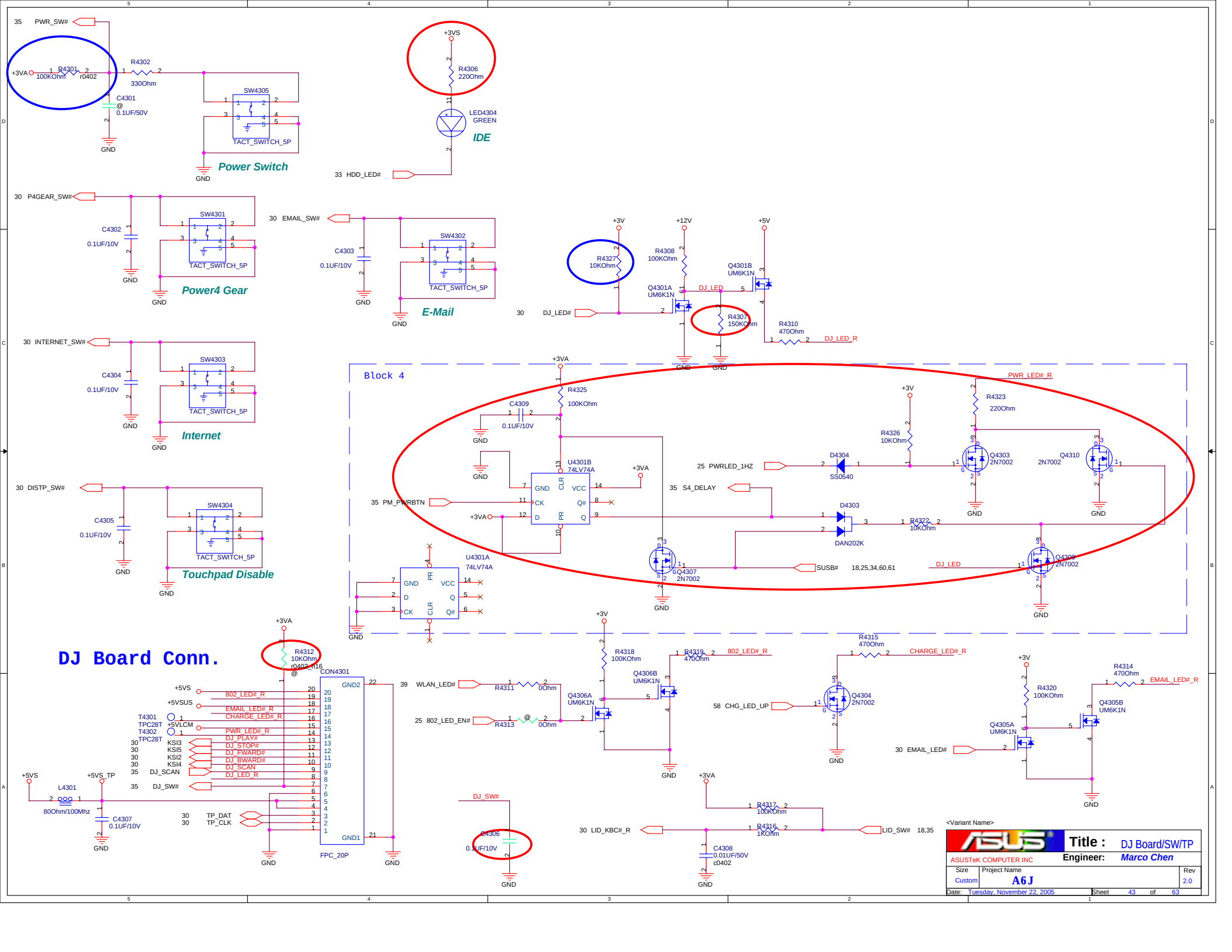
PLCC32 Socket Part Number : 12-043000323
SST FWH/LPC Part Number : 05G00101712L(燒)

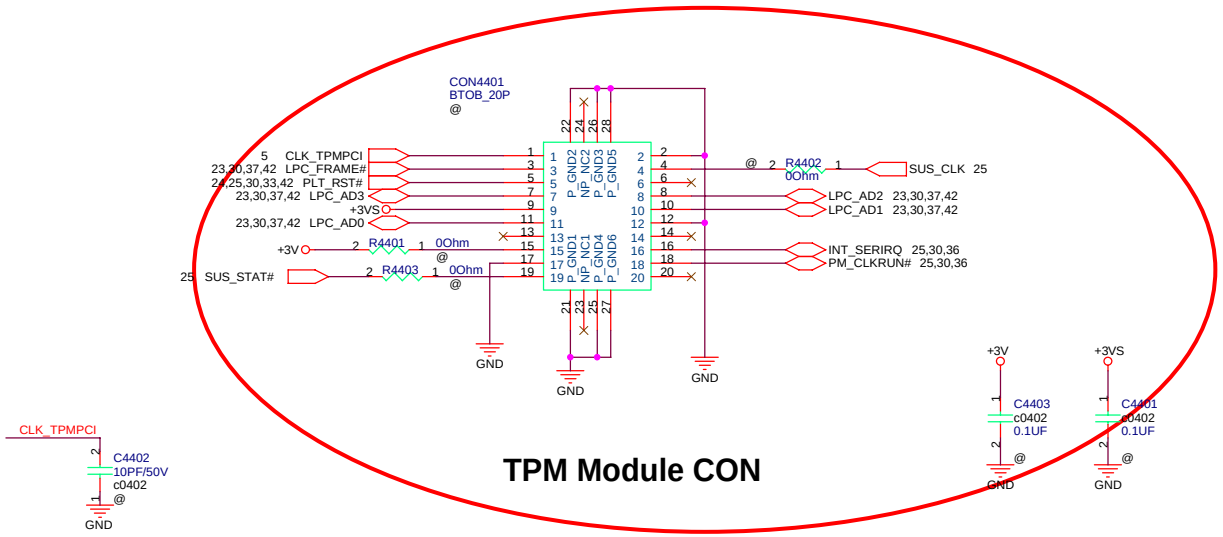


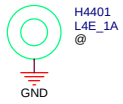


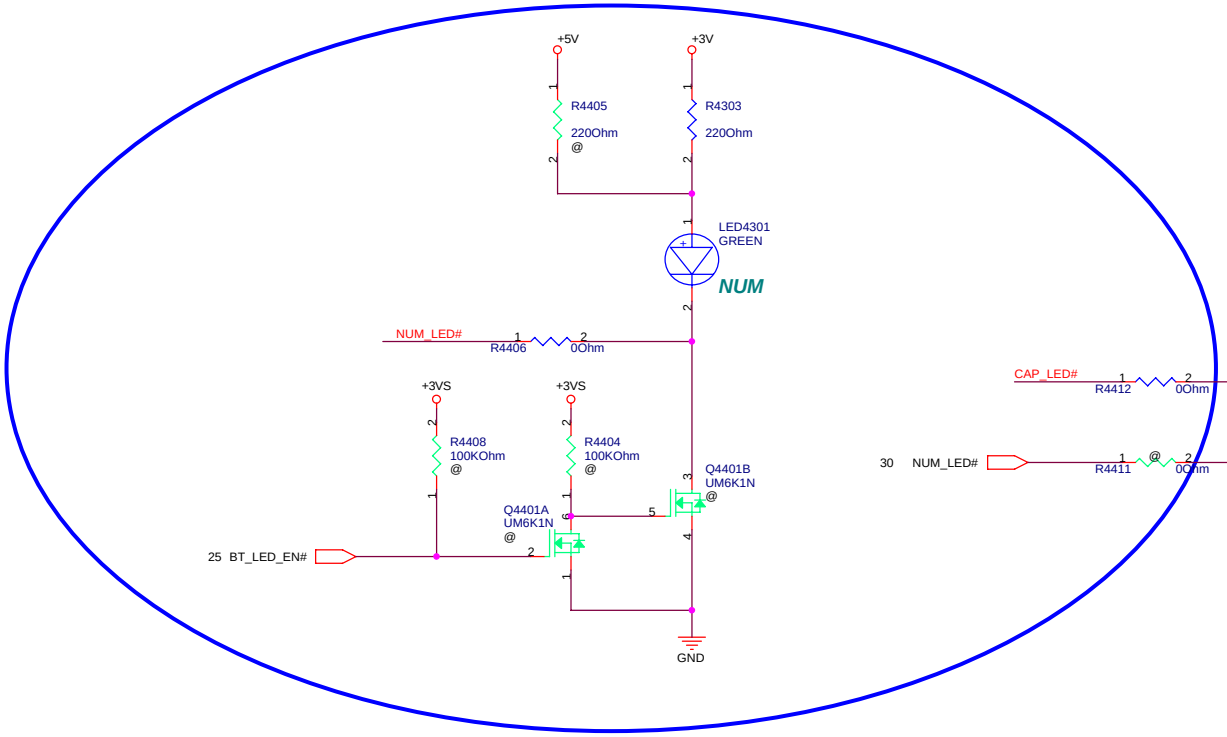
<Variant Name>

ASUSTeK COMPUTER INC	Title : Startup Circuit	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6J	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 42 of 63	


35 PWR_SW#
+3VA
R4301 100KOhm r0402
R4302 330Ohm
C4301 @ 0.1UF/50V
SW4305
TACT_SWITCH_5P
GND
Power Switch
+3VS
R4306 220Ohm
LED4304 GREEN
IDE
33 HDD_LED#
30 P4GEAR_SW#
C4302 0.1UF/10V
SW4301
TACT_SWITCH_5P
Power4 Gear
30 EMAIL_SW#
C4303 0.1UF/10V
SW4302
TACT_SWITCH_5P
E-Mail
30 INTERNET_SW#
C4304 0.1UF/10V
SW4303
TACT_SWITCH_5P
Internet
30 DISTP_SW#
C4305 0.1UF/10V
SW4304
TACT_SWITCH_5P
Touchpad Disable
+3V
+12V
+5V
R4327 10KOhm
R4308 100KOhm
Q4301A UM6K1N
Q4301B UM6K1N
DJ_LED
30 DJ_LED#
R4307 150KOhm
R4310 470Ohm
DJ_LED_R
Block 4
+3VA
R4325 100KOhm
C4309 0.1UF/10V
U4301B 74LV74A
U4301A 74LV74A
35 PM_PWRBTN
25 PWRLED_1HZ
35 S4_DELAY
D4304 SS0540
D4303 DAN202K
Q4307 2N7002
Q4303 2N7002
Q4310 2N7002
Q4308 2N7002
R4326 10KOhm
R4323 220Ohm
R4322 10KOhm
PWR_LED#_R
SUSB# 18,25,34,60,61
DJ_LED
DJ Board Conn.
R4312 10KOhm r0402_m16
CON4301
FPC_20P
+5VS
+5VSUS
+5VLCM
802_LED#_R
EMAIL_LED#_R
CHARGE_LED#_R
PWR_LED#_R
DJ_PLAY#
DJ_STOP#
DJ_FWARD#
DJ_BWARD#
DJ_SCAN
DJ_LED_R
DJ_SW#
T4301 TPC28T
T4302 TPC28T
KSI3
KSI5
KSI2
KSI4
L4301 80Ohm/100Mhz
+5VS_TP
C4307 0.1UF/10V
30 TP_DAT
30 TP_CLK
39 WLAN_LED#
R4311 0Ohm
25 802_LED_EN#
R4313 @ 0Ohm
R4318 100KOhm
R4319 470Ohm
802_LED#_R
Q4306A UM6K1N
Q4306B UM6K1N
58 CHG_LED_UP
R4315 470Ohm
CHARGE_LED#_R
Q4304 2N7002
30 EMAIL_LED#
R4320 100KOhm
R4314 470Ohm
EMAIL_LED#_R
Q4305A UM6K1N
Q4305B UM6K1N
30 LID_KBC#_R
R4317 100KOhm
R4316 1KOhm
LID_SW# 18,35
C4308 0.01UF/50V c0402
C4306 0.1UF/10V
<Variant Name>
Title : DJ Board/SW/TP
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 43 of 63



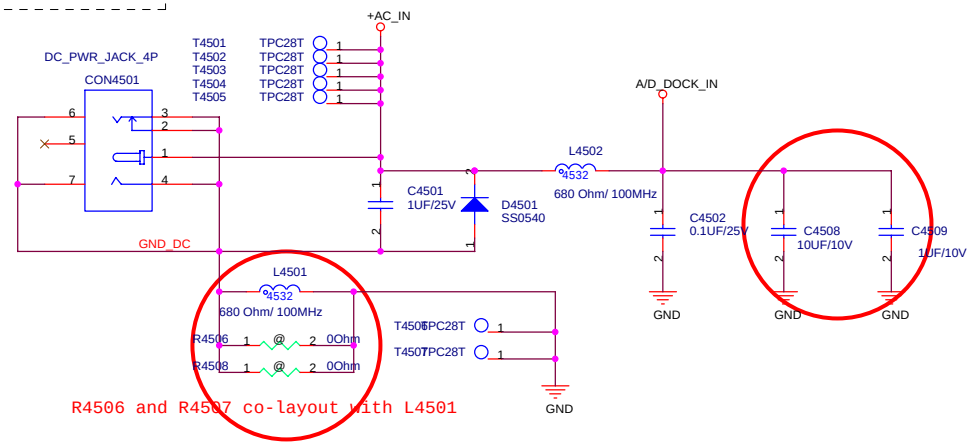


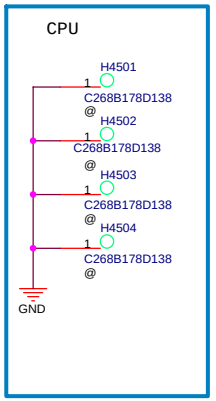


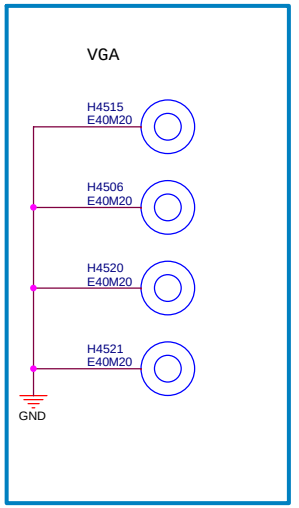
<Variant Name>

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6J	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 44 of 63	

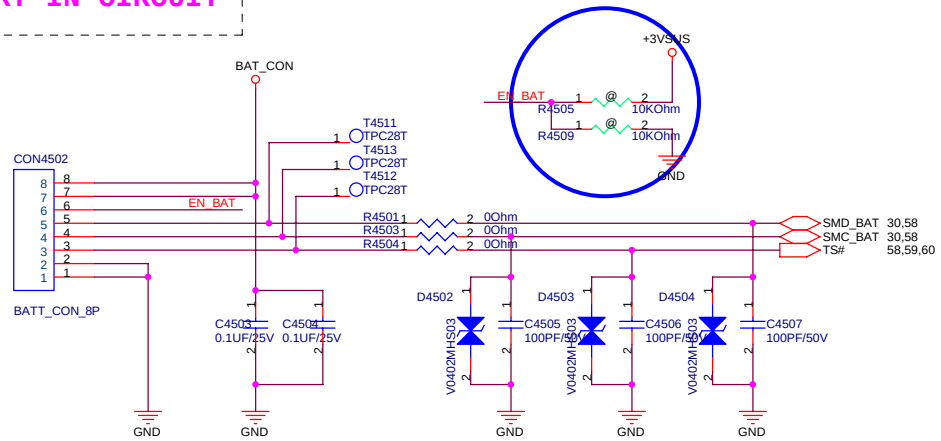
Adaptor IN Circuit

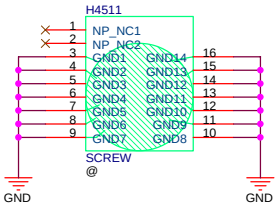


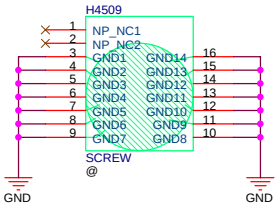


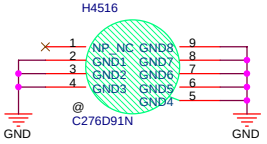


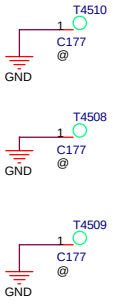
BATTERY IN CIRCUIT

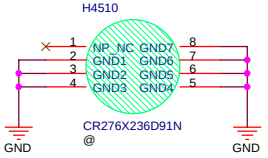


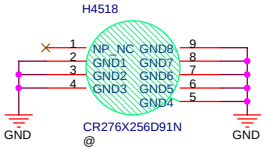


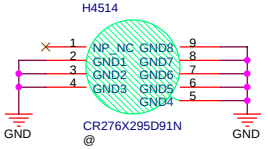


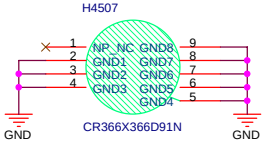


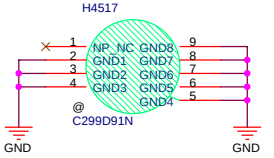


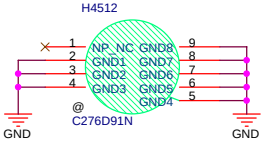


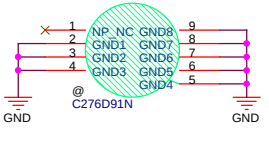


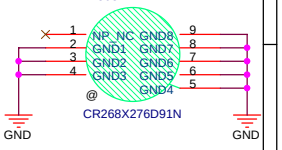












Host	SM-Bus Device	SM-Bus Address	Device
ICH7-M	Clock Generator	1101001x (D2)	ICS954310
ICH7-M	SO-DIMM 0	1010000x (A0)	DDR SOCKET1
ICH7-M	SO-DIMM 1	1010001x (A4)	DDR SOCKET2
ICH7-M	Thermal Sensor	0101110x (5C)	ADT7463 (Optinal)

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D

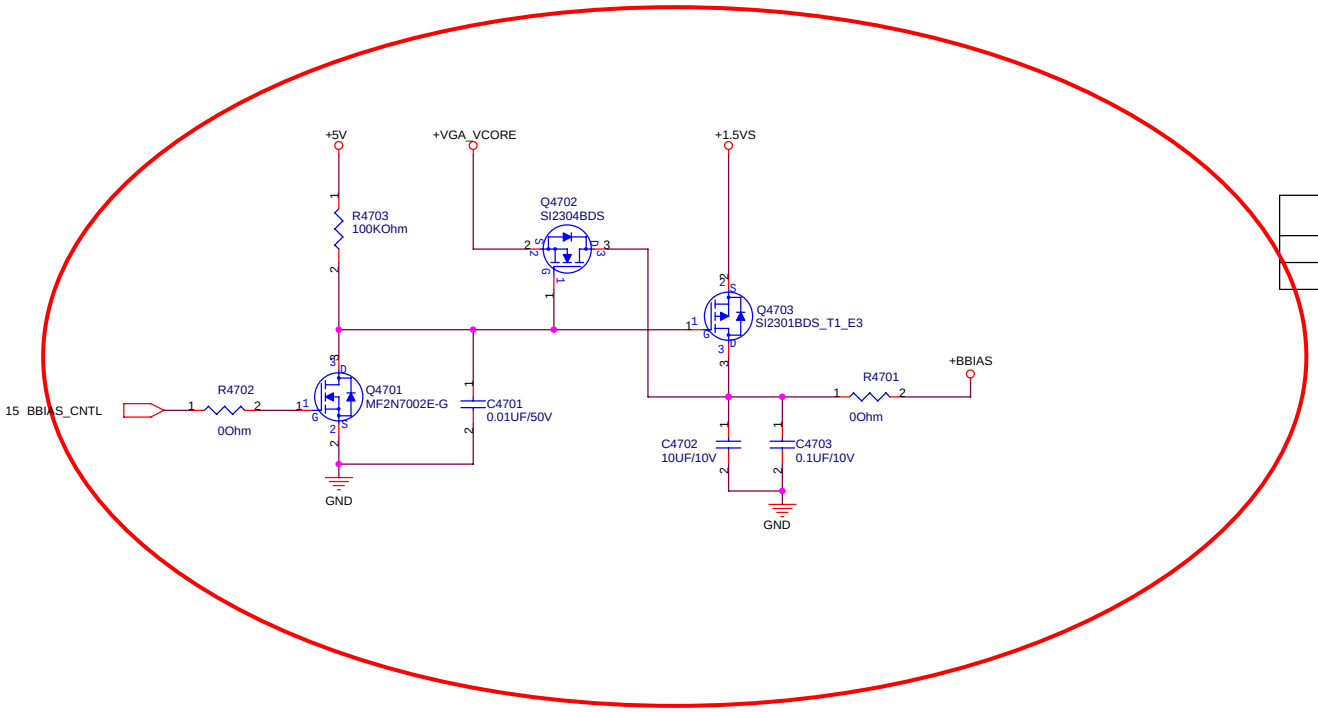
<Variant Name>

Title : SYSTEM

ASUSTeK COMPUTER INC Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 46 of 63



GENERICD_C	+BBP
0	1.1V
1	1.5V

GENERICD_C	-BBN
0	GND
1	-0.5V

<Variant Name>

Title : Back BIAS

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 47 of 63

R1.0 -> R1.1

1. Page2: Add test points T215 and T216 for H_ADS# and H_CPURST#

2. Page4: Modify FAN solution from DA to PWM and change R-C delay timing.

   A. Mount R416 and DNI R415

   B. Change C404 to 1uF

3. Page4: Connect +3VS_FAN(R419*3.3K ohm and R420*2.2K ohm 分壓 from +V5S_FAN) to U401.3 because FAN_DA level is 3V and FAN_PWM# is open-drain, change pull-up to +3VS and U401.3 level shift from 5V to 3V

4. Page4: Add pull-down resister R418*10M ohm to protect noise when power-on

5. Page5: Add (R579*33 ohm and C529*10pF) for TPM PCI 33MHz clock

6. Page5: Change R531 from 10 ohm to 22ohm to eliminate swing.

7. Page5: DNI R510 to disable ITP enable.

8. Page7: Delete R715 because it duplicate with R529.

9. Page9: Change L905 to P/N:09G012030000 and L905 to P/N:09G013120409 because +1.5VS_PCIE consume about 1.3A and +1.5VS_3GPLL consume 200mA only.

10. Page13: VGA_GPIO5 add pull-up 10K ohm to +3VS for ATI recommendation.

11. Page13: DNI R1320 and mount R1321 to change back light enable from DC level to PWM and meet VBIOS support.

12. Page13: Add R1343*0 ohm for reserving bead to ground.

13. Page15: Change L1504.2 to connect from +VGA_VCORE to +1.2VSP for ATI recommendation.

14. Page15: Change bead L1506 from 120Ohm/100Mhz to 30Ohm/100Mhz type.

15. Page19: Add bead L1913 between TV_GND and GND.

16. Page23: Change High Definition damping resisters*R2312, R2314, R2316, R2318, R2320, R2322, R2324, R2325 from 22 ohm to 39 ohm for reducing reflection.

17. Page29: Add Line-in solution, please commt Black 2.

18. Page31, 32: Change LAN chip from Marvell 88E8053 to Realtek RTL8111B.

19. Page34: Add Q3401 and R3414 to replace U3402B.

20. Page34,35: Modify reset circuits to meet Intel specification, please commt Black 3.

21. Page35,43 : DNI R4312 and change R3509 from 4.7M ohm to 2.2 M ohm to short SWDJ_EN# detected to 2secends for BIOS requirement and add INIT# solution(please comment Block 7).

22. Page37: Change R3706 from 10K ohm to 100K ohm to enlarge R-C delay time.

23. Page39: Reserve R3905 to PLT_RSTNS# Wire-Or with PLT_RST#_BUF.

24. Page41: Short CON4101.1 and CON4101.2 and delete R4105, R4104, and C4103 because no timing issue between power and enable signal.

25. Page42: Delete D4201 and DNI R4202 because no power loss issue exist.

26. Page43: Modify S4 strech circuits, please comment Block 4.

27. Page44: Add TPM connecter.

28. Page45: Add C4508, C4509, R4506 and R4507 for EMI requirment.

29. Page42: Change CON4202.1 and CON4202.3 power from +3VSUS to +3V.

30. Page18: Change L1806.2 power from AC_BAT_SYS to AC_BAT_SYS_CPU for EMI requirement.

31. Page7: Change from VRM_PWRGD to ICH7_PWROK to enable MCH_PWROK for Intel requirement(Mount R721 and DNI R722).

32. Page23,34: Change thermal-trip solution.

   A. Mount R2315 and DNI R4507

   B. Remove the circuits.(please comment Block 5)

   C. Mount thermal protection circuits.(please comment Block 6)

33. Page5, 23, 37: Change capacitor values for TXC recommendations(C513,C514 from 33pF to 27pF, C2302, C2304 from 12pF to 22pF ,Change X3701 to 07G010S22450*30 ppm and C3725 and C3726 to 22pf).

34. Page15, 47: Add Back Bias circuits for ATI recommendations.

35. Page5, 23, 33: Add SATA circuits for OEM requirement.

36. Page12: Remove R1205 for ATI recommendations.

37. Page39: Reserve R-C to tune waveform quanlity.(R3906,R3907,C3911,C3912)

38. Page41: Reserve R4104, R4105, R4106 to modify enable blue tooth solution.

R1.1 -> R2.0

1. Page4, 34: Add power limit solution and change thermal protection solution.

   A. Add R421*0 ohm and connect to H_PROCHOT_S#

   B. DNI R417*0 ohm

   C. Add R422*0 ohm and connect to OVERTEMP# that is wire-or with FORCE_OFF#.

   D. DNI OTP solution.

2. Page15: Add BBIAS_CNTL pull-down resister R1508*10K ohm to GND.

3. Page19: Modify parts (D1912 and F1901).

4. Page24: Add 3 pcs decoupling CAPs(C2410, C2411, C2412) to short return path because PCI Bus(IN1) reference +1.8VS(Vcc).

5. Page25, 44: Add BT_LED solution to co-layout with Scroll Lock for Epson requirement.

6. Page27: Change R2704 from 0 ohm to 150 ohm.

7. Page27: Change R2707 from 47K ohm to 332K ohm.

8. Page27, 28: Add MUTE_POP# solution for Epson requirements. Please comment PR BlOCK 1.

9. Page30: Add LID switch solution.

   A. Change BAT_SEL# push-pull resister from +3V to GND.

   B. DNI Q3002*2N7002.

10. Page31: Change LAN chip reset signal from PLT_RSTNS# to PCI_RST#. (Mount R3107 and DNI R3106).

11. Page35: Change KBCRSM solution to connect to PM_PWRBTN# directly, please comment PR BLOCK 2.

12. Page36: Change CARDBUS chip reset signal from PLT_RST#_BUF to PLT_RST#. (Mount R3618 and DNI R3617).

13. Page39: Add WLAN_LED# pull-high resister R3908*100K ohm to solve LED was lighted when miniCARD was un-plug in.

<Variant Name>

ASUSTeK COMPUTER INC	Title : History (1)	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6J	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 48 of 63	

14. Page40: Remove L4003, L4005, L4007, L4008 for EMI requirement.

15. Page43: Mount R4301*100K ohm to avoid PWR_SW# is floating.

16. Page43: Mount R4327*10K ohm to fix DJ_LED light soon issue when power on.

<Variant Name>

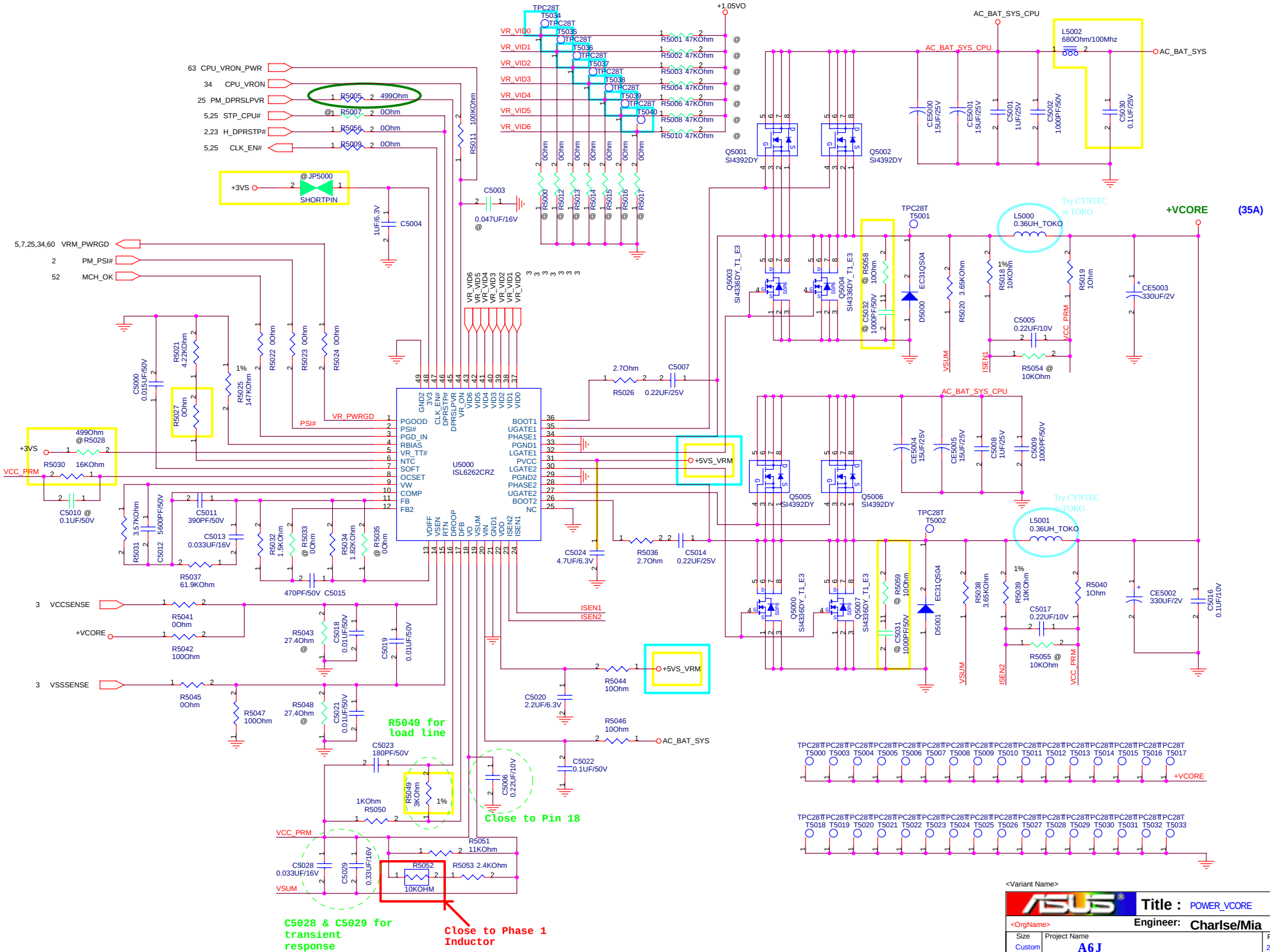
Title : History(2)

<OrgName>

Engineer: Marco Chen

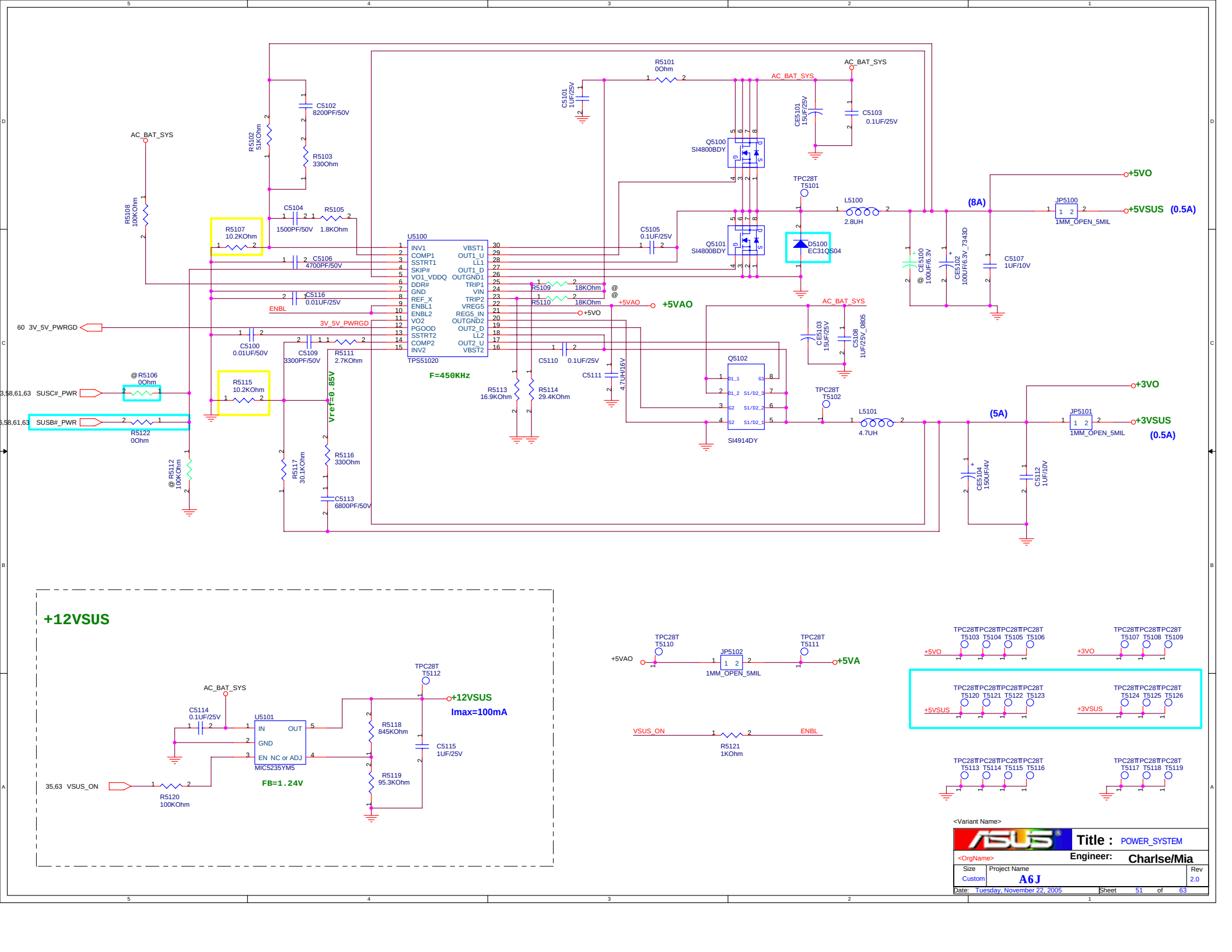
Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 49 of 63



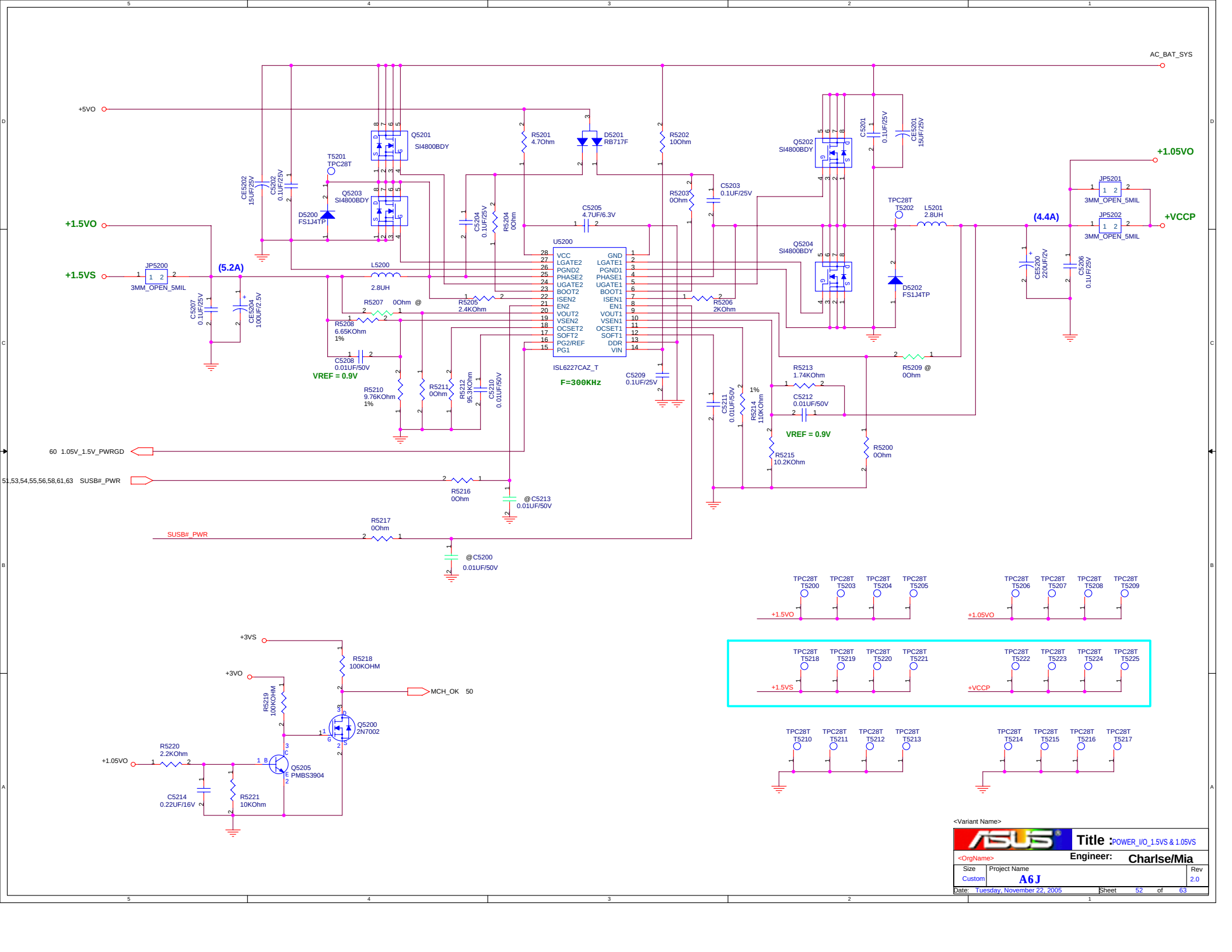
<Variant Name>

Title :	POWER_VCORE
<OrgName>	Engineer: Charlse/Mia
Size: Custom	Project Name: A6J
Rev: 2.0	
Date: Tuesday, November 22, 2005	Sheet 50 of 63



<Variant Name>

Title :	POWER_SYSTEM
<OrgName>	Engineer: Charlse/Mia
Size: Custom	Project Name: A6J
Rev: 2.0	
Date: Tuesday, November 22, 2005	Sheet 51 of 63



<Variant Name>

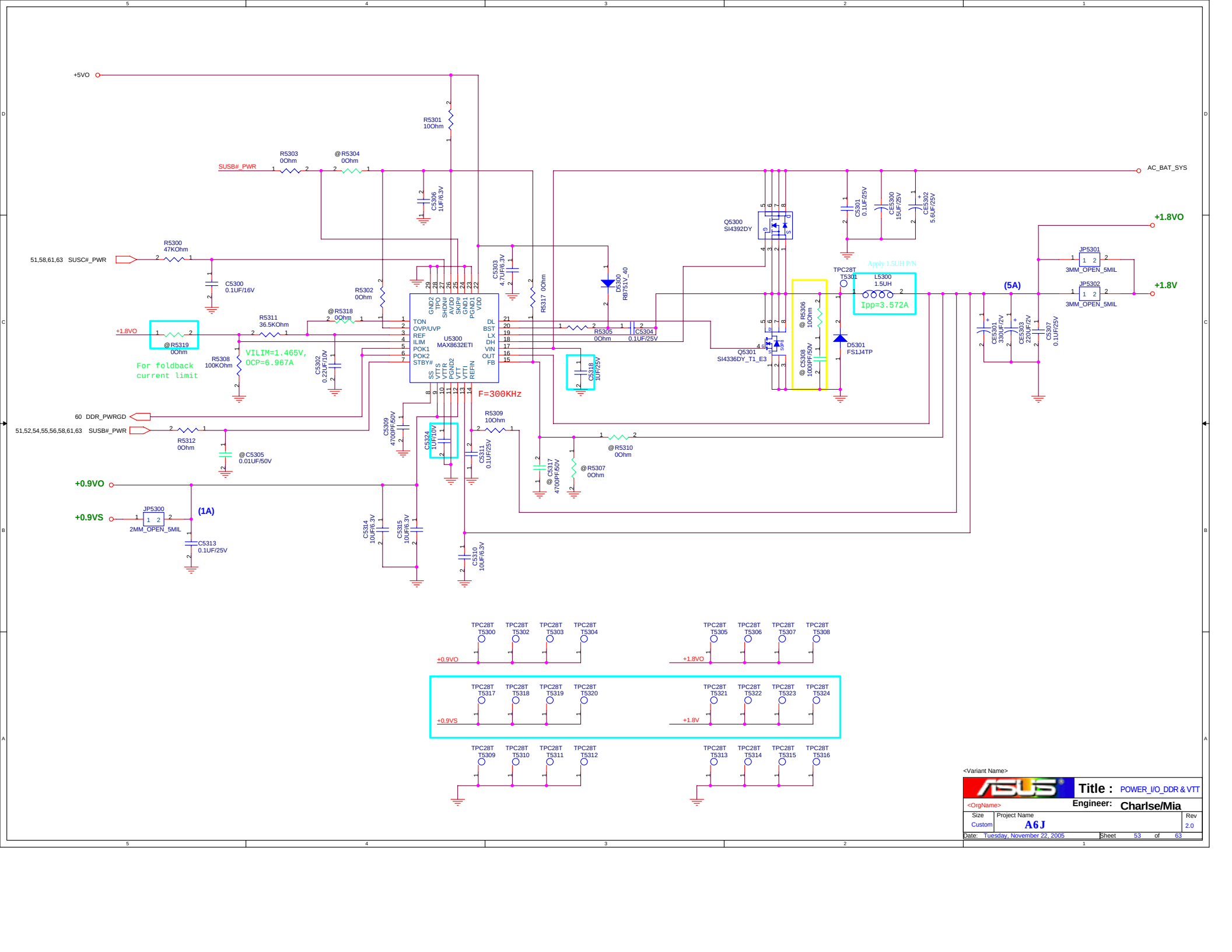
Title : POWER_I/O_1.5VS & 1.05VS

<OrgName>

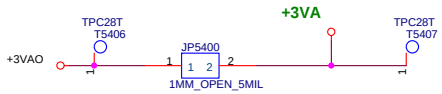
Engineer: Charlse/Mia

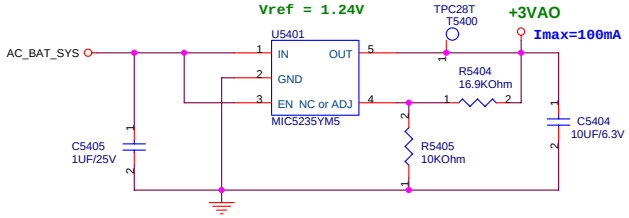
Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 52 of 63

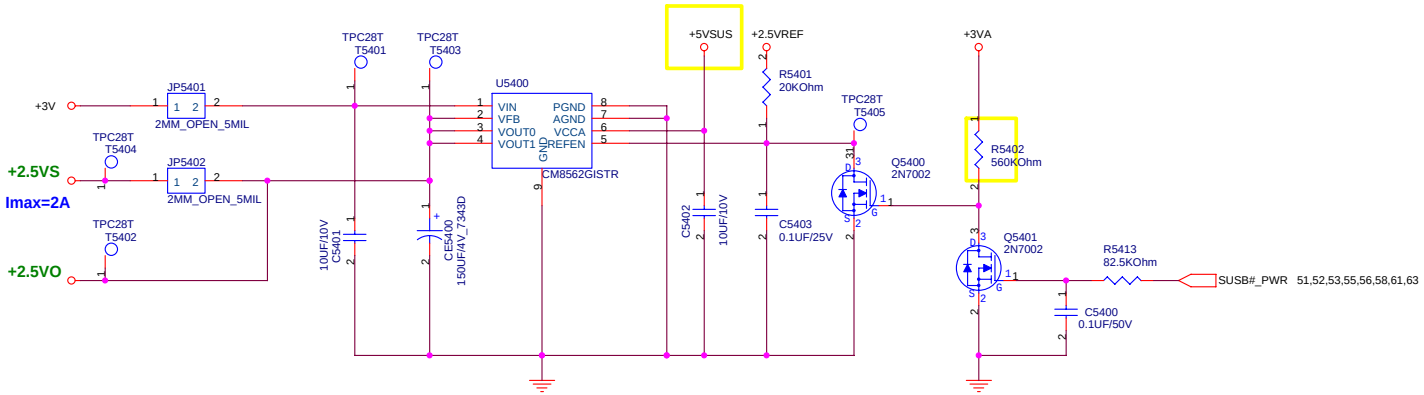

+5VO
R5301 10Ohm
R5303 0Ohm
@R5304 0Ohm
SUSB#_PWR
C5306 1UF/6.3V
AC_BAT_SYS
Q5300 SI4392DY
C5301 0.1UF/25V
CE5300 15UF/25V
CE5302 5.6UF/25V
+1.8VO
JP5301
3MM_OPEN_5MIL
+1.8V
JP5302
3MM_OPEN_5MIL
(5A)
R5300 47KOhm
51,58,61,63 SUSC#_PWR
C5300 0.1UF/16V
C5303 4.7UF/6.3V
R5317 0Ohm
D5300 RB751V_40
TPC28T T5301
L5300 1.5UH
Ipp=3.572A
Apply 1.5UH P/N
R5302 0Ohm
@R5318 0Ohm
R5311 36.5KOhm
+1.8VO
@R5319 0Ohm
R5308 100KOhm
VILIM=1.465V,
OCP=6.967A
For foldback current limit
C5302 0.22UF/10V
U5300 MAX8632ETI
TON
OVP/UVP
REF
ILIM
POK1
POK2
STBY#
GND2
TPO
SHDN#
AVDD
SKIP#
GND1
PGND1
VDD
DL
BST
LX
DH
VIN
OUT
FB
SS
VTTS
VTTR
PGND2
VTTI
REFIN
R5305 0Ohm
C5304 0.1UF/25V
C5318 10UF/25V
F=300KHz
R5306 10Ohm
@ C5308 1000PF/50V
Q5301 SI4336DY_T1_E3
D5301 FS1J4TP
CE5301 330UF/2V
CE5303 220UF/2V
C5307 0.1UF/25V
60 DDR_PWRGD
51,52,54,55,56,58,61,63 SUSB#_PWR
R5312 0Ohm
@C5305 0.01UF/50V
C5309 4700PF/50V
C5324 10UF/10V
R5309 10Ohm
C5311 0.1UF/25V
@R5310 0Ohm
@ C5317 4700PF/50V
@R5307 0Ohm
+0.9VO
+0.9VS
JP5300
2MM_OPEN_5MIL
(1A)
C5313 0.1UF/25V
C5314 10UF/6.3V
C5315 10UF/6.3V
C5310 10UF/6.3V
TPC28T T5300
TPC28T T5302
TPC28T T5303
TPC28T T5304
TPC28T T5305
TPC28T T5306
TPC28T T5307
TPC28T T5308
TPC28T T5317
TPC28T T5318
TPC28T T5319
TPC28T T5320
TPC28T T5321
TPC28T T5322
TPC28T T5323
TPC28T T5324
TPC28T T5309
TPC28T T5310
TPC28T T5311
TPC28T T5312
TPC28T T5313
TPC28T T5314
TPC28T T5315
TPC28T T5316
<Variant Name>
Title : POWER_I/O_DDR & VTT
<OrgName>
Engineer: Charlse/Mia
Size Custom
Project Name A6J
Rev 2.0
Date: Tuesday, November 22, 2005
Sheet 53 of 63

+3VA0



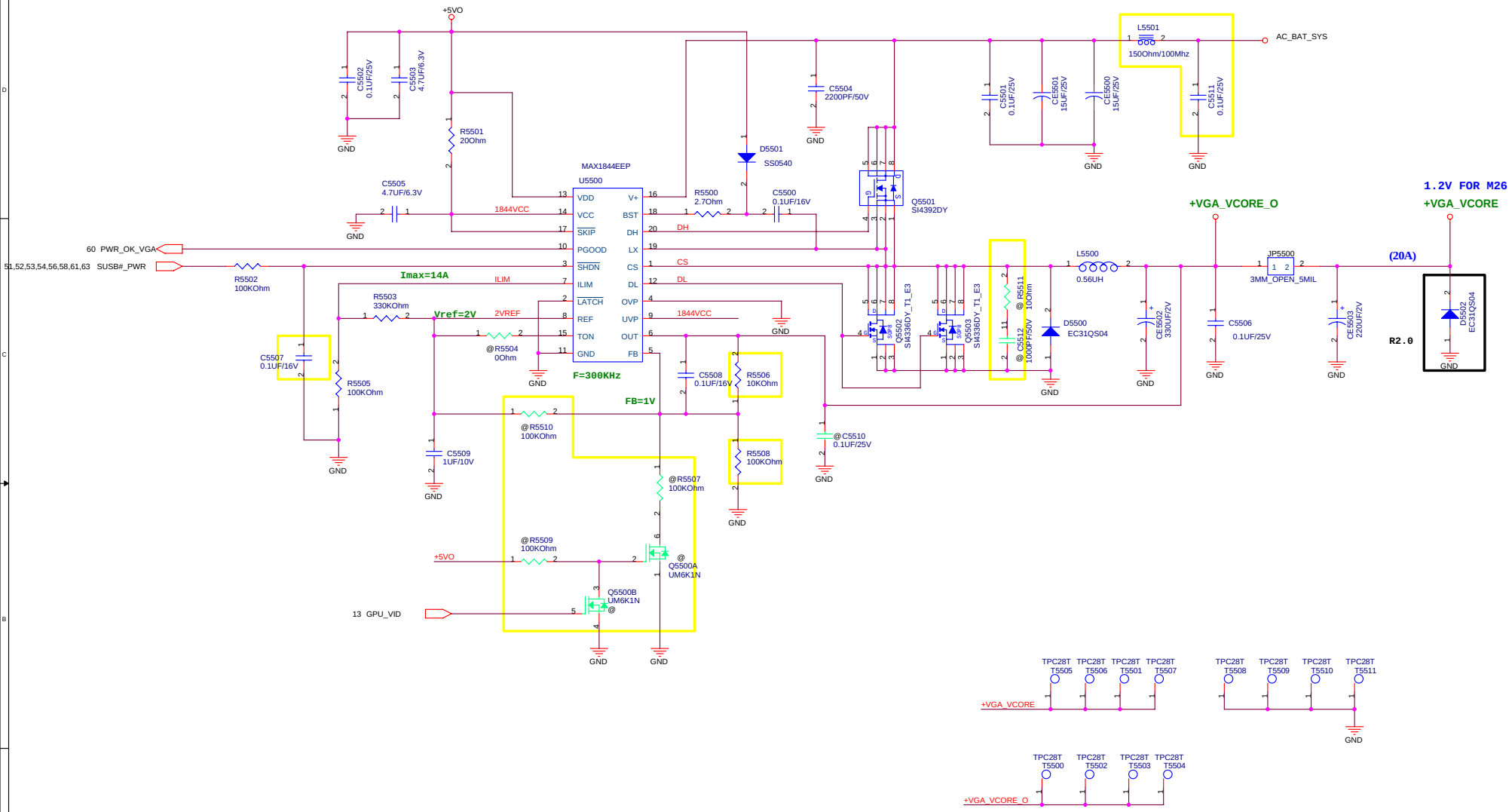


+2.5VS



<Variant Name>

ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer: Charlse/Mia	
Size: Custom	Project Name: A6J	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 54 of 63	



<Variant Name>

Title : + VGA_CORE

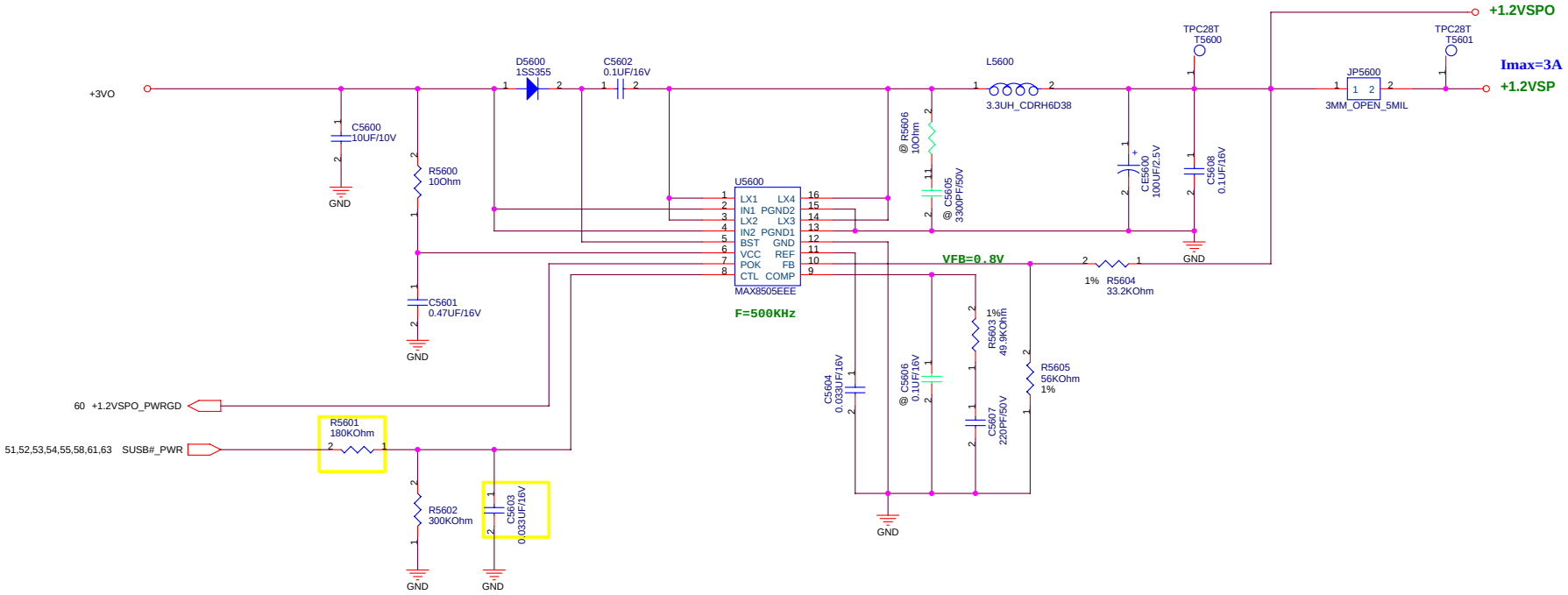
<OrgName>

Engineer: Charlse/Mia

Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 55 of 63

+1.2VSP



<Variant Name>

Title :	POWER_VGA_+1.2VSP	
<OrgName>	Engineer:	Charlse/Mia
Size: Custom	Project Name: A6JC	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 56 of 63	

TOTAL POWER=65W
-->3.42A

BATSEL_2P# = "H" (1P)			
BAT cpapcity	R5712	VICTL(V)	ICHG(A)
2000mAH	41.2K	1.8976	1.39
2200mAH	52.3K	2.0989	1.537
2400mAH	66.5K	2.2918	1.679
2600mAH	86.6K	2.4871	1.822

Vref = 4.096V
VLDO = 5.4V

VCTL= LDO
=> Vbatt = 4.2V X CELLS

VICTL= 3.325V => 3S
VICTL= 2.506V => 4S

Charge Current Ichg =
[0.075V/Rsense(CHG)]*[VCLS/4.096V]
Rsense(CHG)=0.025 ohm
VICTL= 3.4632V => Ichg = 2.53A

CHG_EN#	AC_APR_UC	SWITCH
H	H	OFF
H	L	ON
L	H	ON
L	L	ON

Adaptor error circuit for 4S battery

Vth = 17.5V (MAX. 17.8V & MIN. 17.2V)

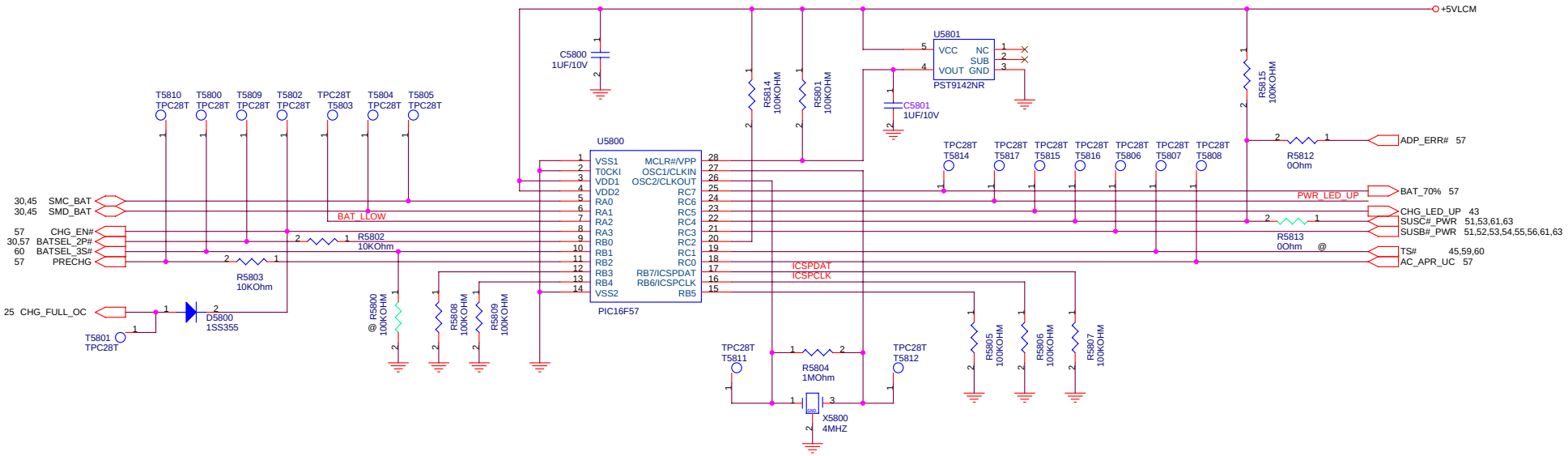
Power Limit Circuit

PRE_CHARGE CIRCUIT
Pre-charge voltage 12.6V

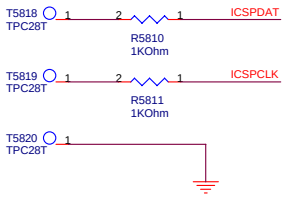
Vfb=1.25V

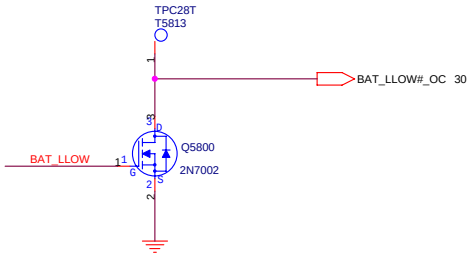
Title :	POWER_CHARGER
<OrgName>	Engineer: Charlse/Mia
Size: C	Project Name: A6J
Rev: 2.0	
Date: Tuesday, November 22, 2005	Sheet 57 of 63

PIC16F57



For PIC reflash

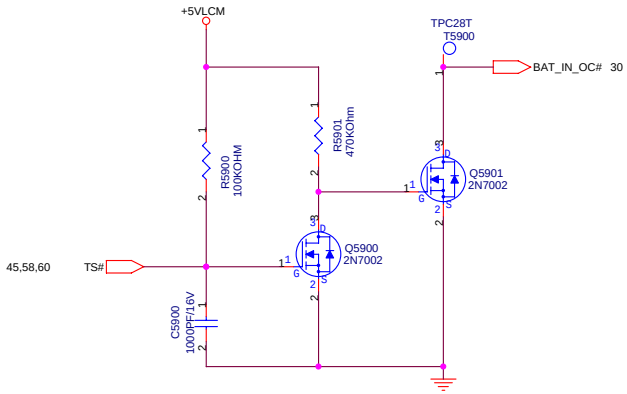




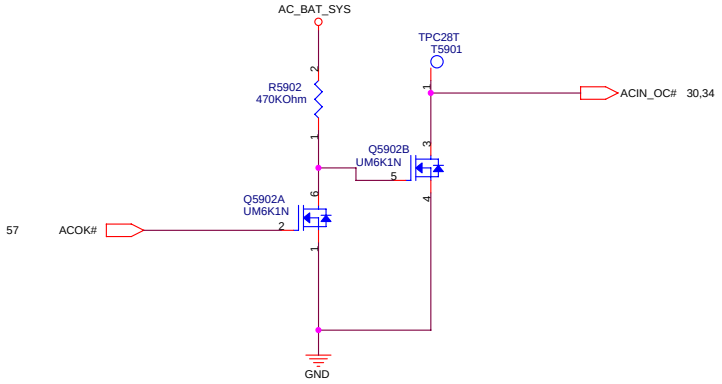
<Variant Name>

ASUS	Title : POWER_PIC	
<OrgName>	Engineer: Charlse/Mia	
Size: Custom	Project Name: A6J	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 58 of 63	

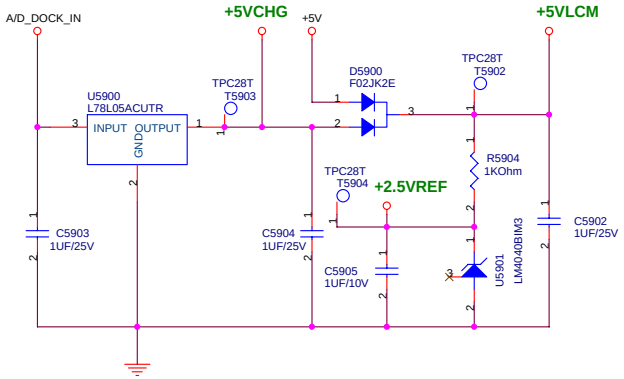
BATTERY IN DETECT



ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF



<Variant Name>

Title : POWER_DETECT

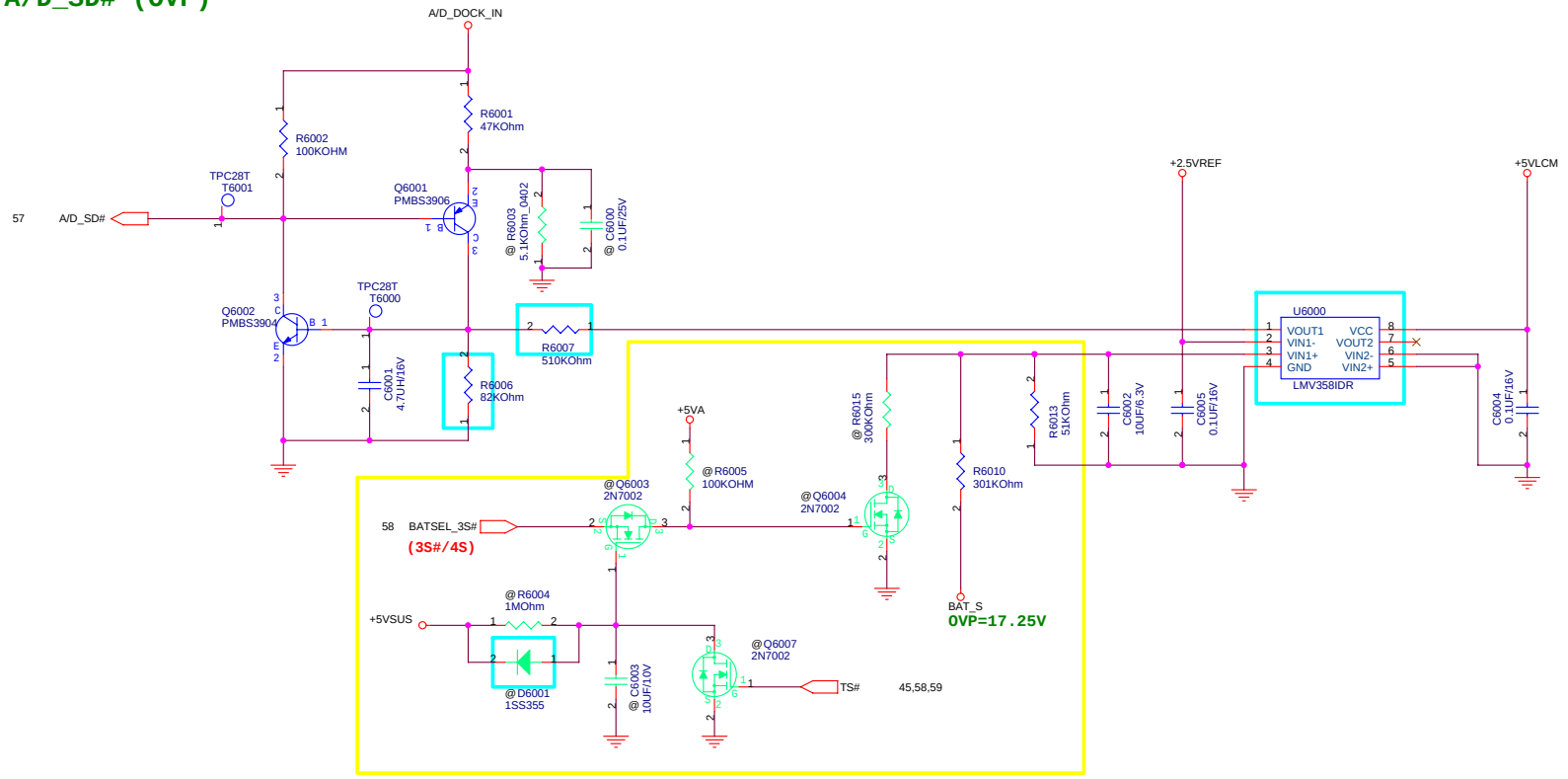
<OrgName>

Engineer: Charlse/Mia

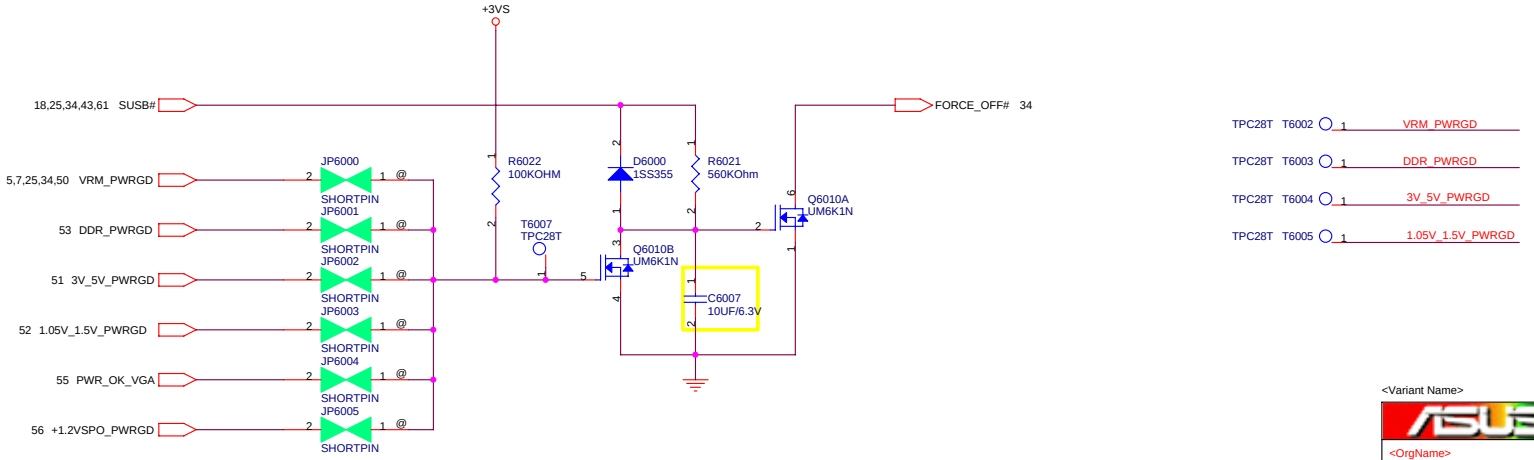
Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 59 of 63

BATTERY A/D_SD# (OVP)



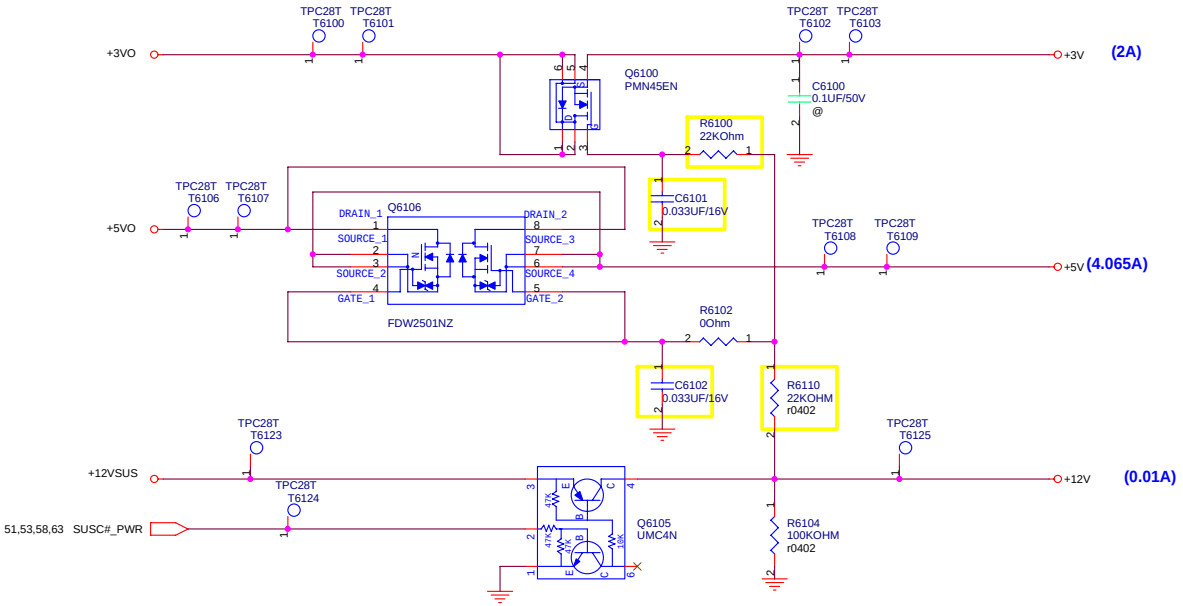
POWER GOOD DETECTER

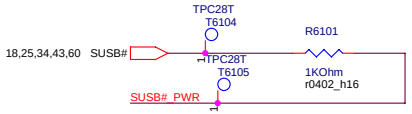


<Variant Name>

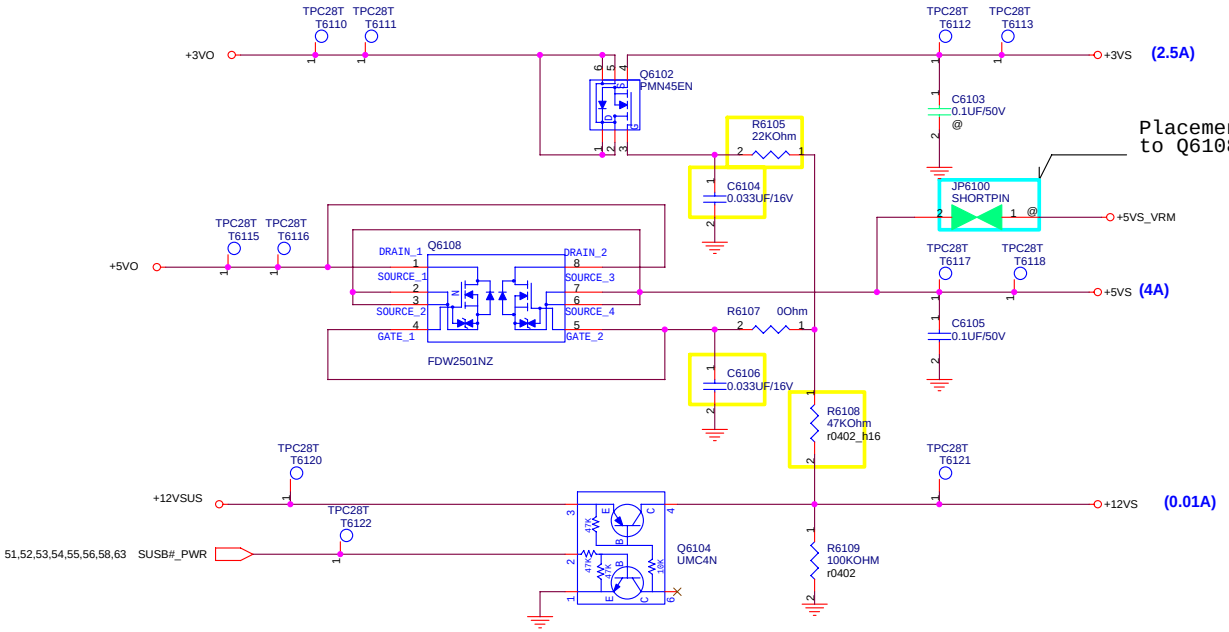
Title : POWER_PROTECT		
<OrgName>	Engineer: Charlse/Mia	
Size: Custom	Project Name: A6J	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 60 of 63	

SUSC#_PWR POWER

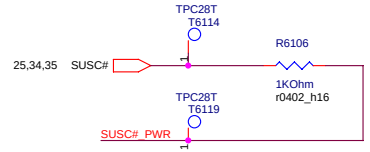


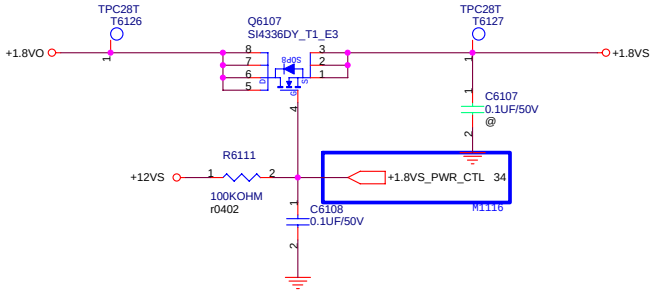


SUSB#_PWR POWER



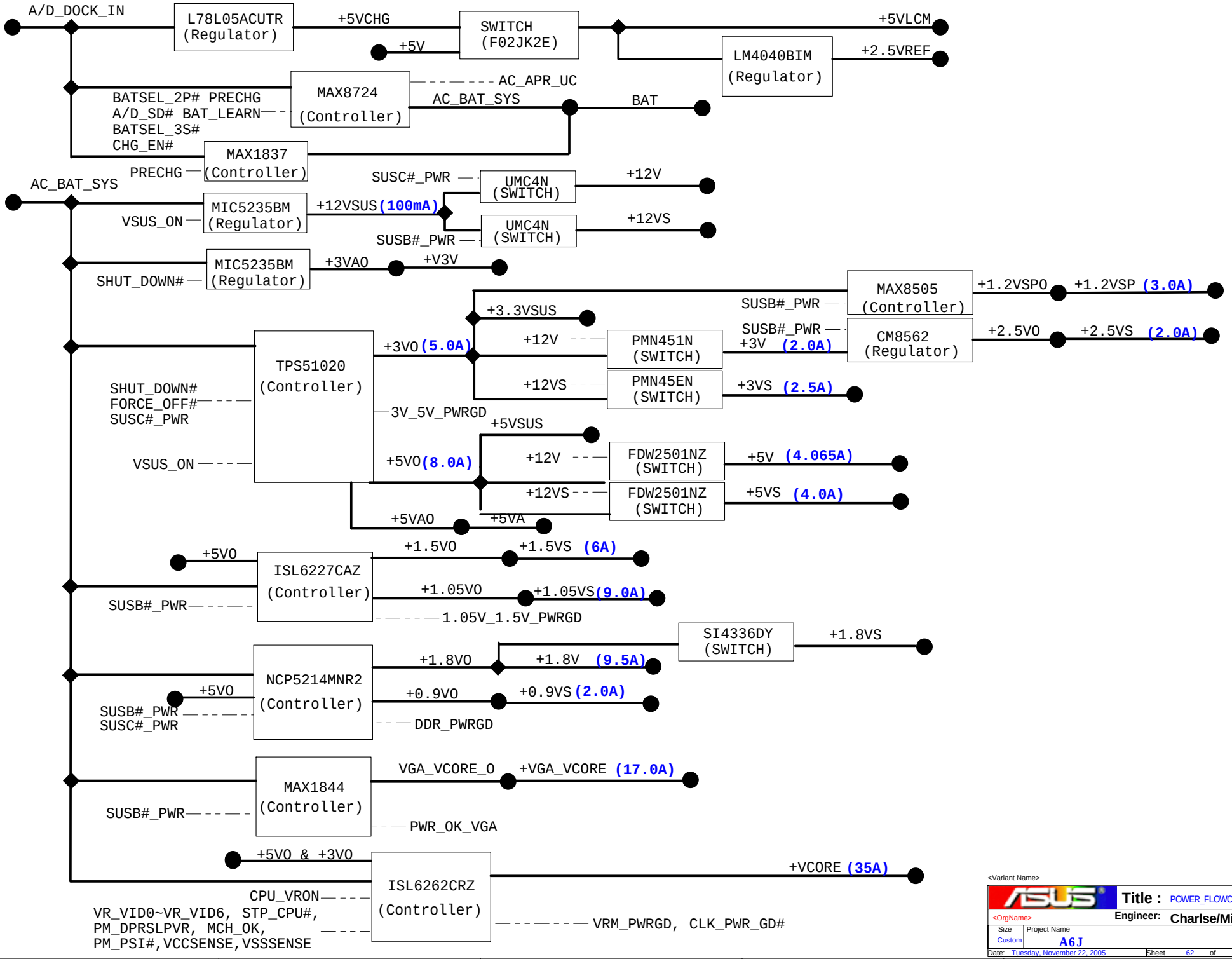
Placement near to Q6108





<Variant Name>

ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer: Charlse/Mia	
Size: Custom	Project Name: A6J	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 61 of 63	



<Variant Name>

<OrgName>	Title : POWER_FLOWCHART	
	Engineer: Charlse/Mia	
Size: Custom	Project Name: A6J	Rev: 2.0
Date: Tuesday, November 22, 2005	Sheet 62 of 63	

AC_BAT_SYS → AC_BAT_SYS 50,51,52,53,54,55,57,59

+3VA → +3VA 18,23,34,35,43,54

+5VA → +5VA 34,51,57,60

+5VO → +5VO 51,52,53,55,61

+3VO → +3VO 51,52,56,61

+3V → +3V 25,30,31,32,35,36,37,38,41,42,43,44,54,61

+3VS → +3VS 4,5,7,9,11,13,15,18,19,20,21,25,26,27,28,30,31,33,34,35,36,39,42,43,44,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 4,28,35,40,43,61

+12VS → +12VS 18,19,35,61

+5V → +5V 18,30,35,37,40,43,44,47,59,61

+5VS → +5VS 4,19,22,26,27,30,33,35,41,43,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 9,13,15,19,35,54

+1.8VO → +1.8VO 53,61

+1.8V → +1.8V 7,10,20,21,35,53

+1.8VS → +1.8VS 14,15,16,17,22,24,35,61

+0.9VS → +0.9VS 14,22,35,53

BAT → BAT 57

+5VCHG → +5VCHG 57,59

+5VLCM → +5VLCM 30,43,57,58,59,60

+2.5VREF → +2.5VREF 54,57,59,60

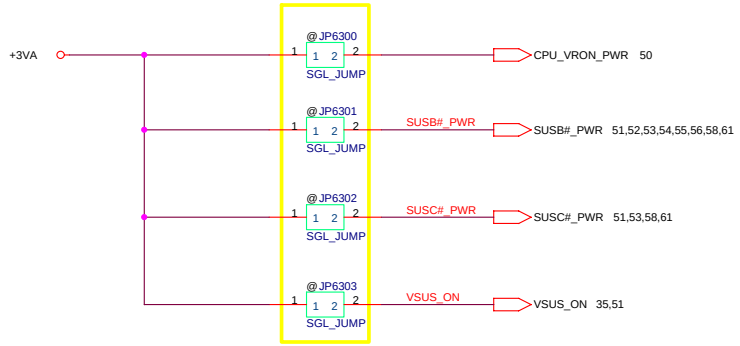
+VCORE → +VCORE 3,4,50

+VGA_VCORE → +VGA_VCORE 12,13,15,47,55

+1.2VSP → +1.2VSP 12,15,35,56

BAT_CON → BAT_CON 45,57

FOR POWER TEST



<Variant Name>

Title : POWER_SIGNAL

<OrgName>

Engineer: Charlse/Mia

Size	Project Name	Rev
Custom	A6J	2.0

Date: Tuesday, November 22, 2005 Sheet 63 of 63

www.s-manuals.com