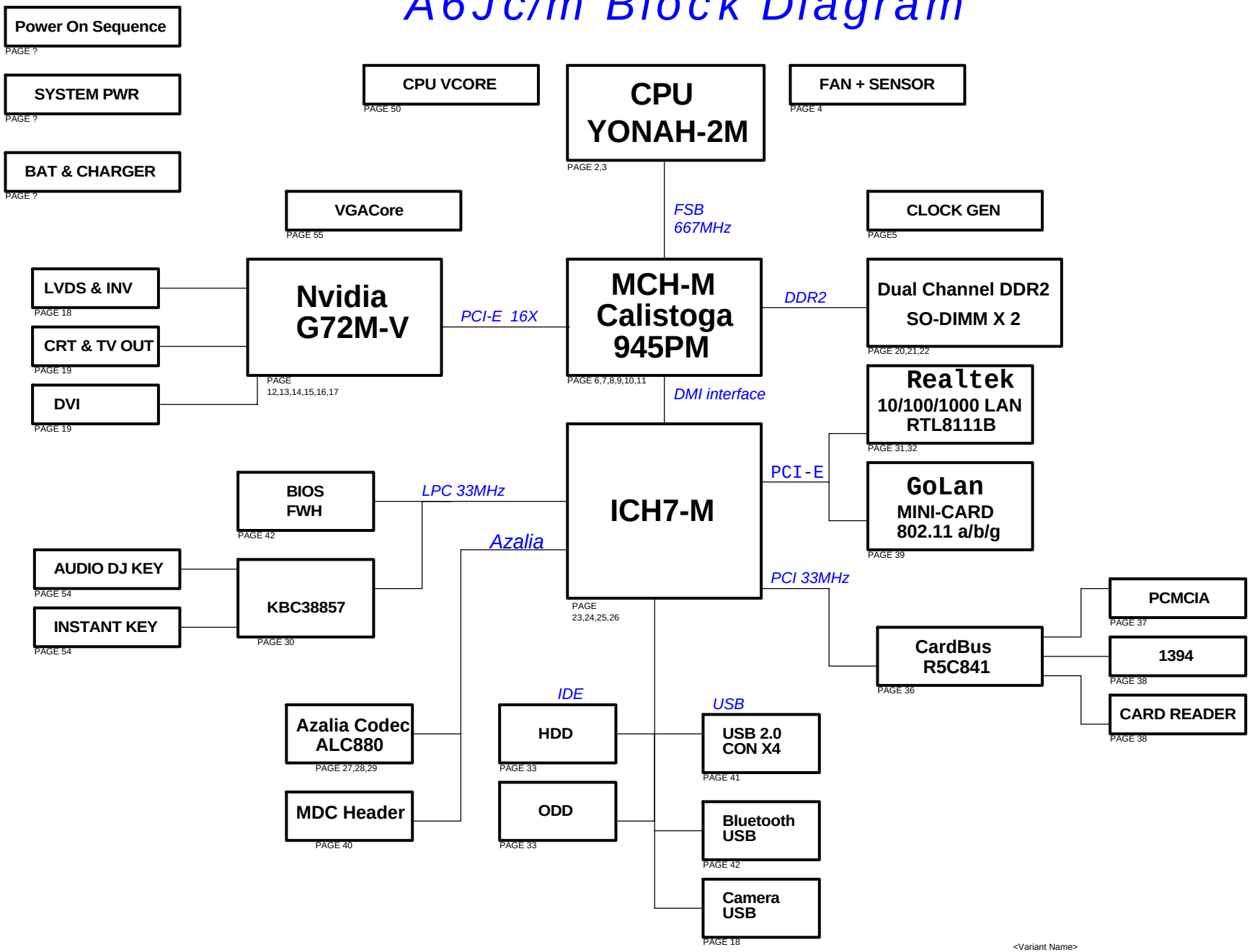
A6Jc/m Block Diagram



<Variant Name>

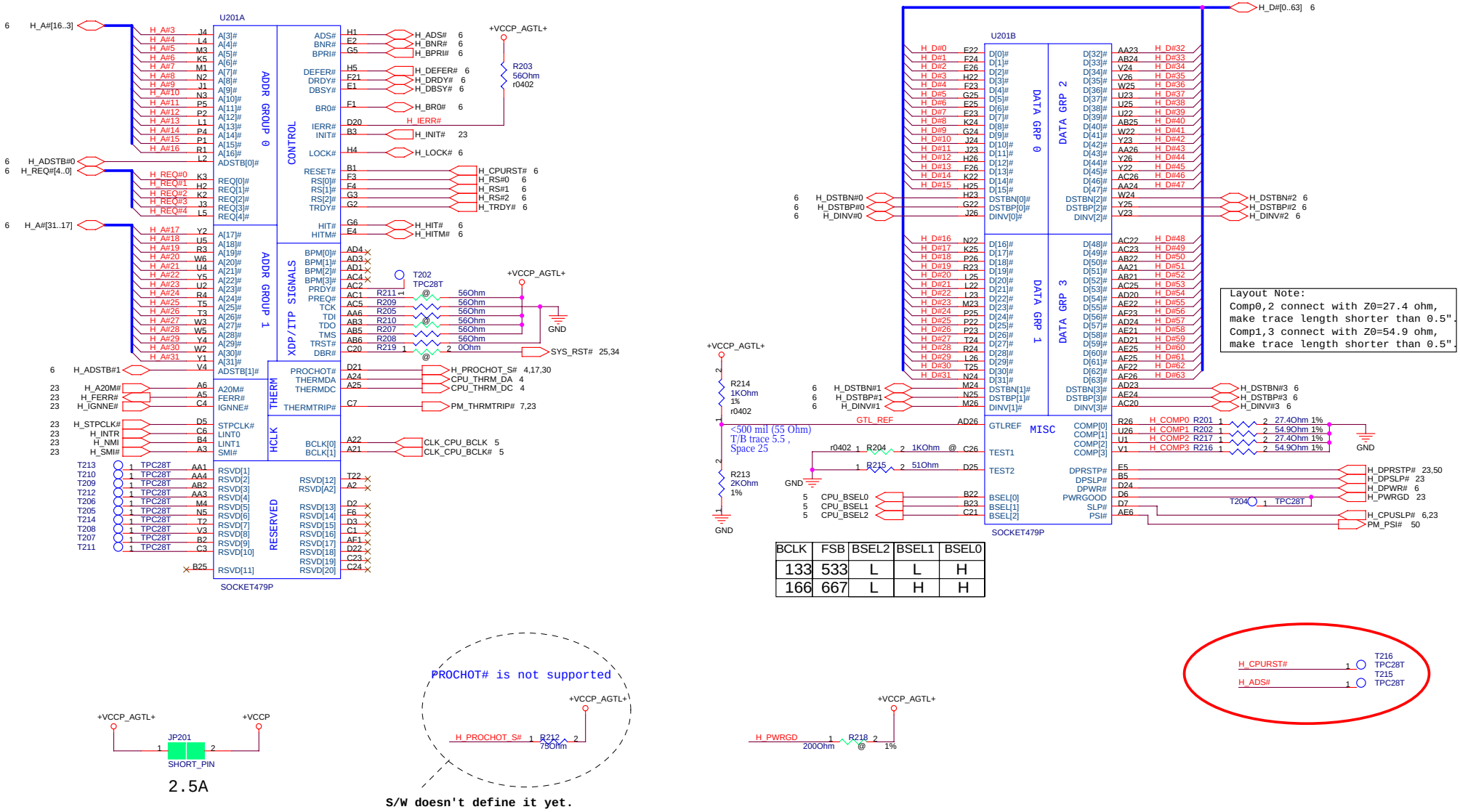
Title : BLOCK DIAGRAM

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 1 of 63



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

<Variant Name>

Title : YONAH CPU (1)

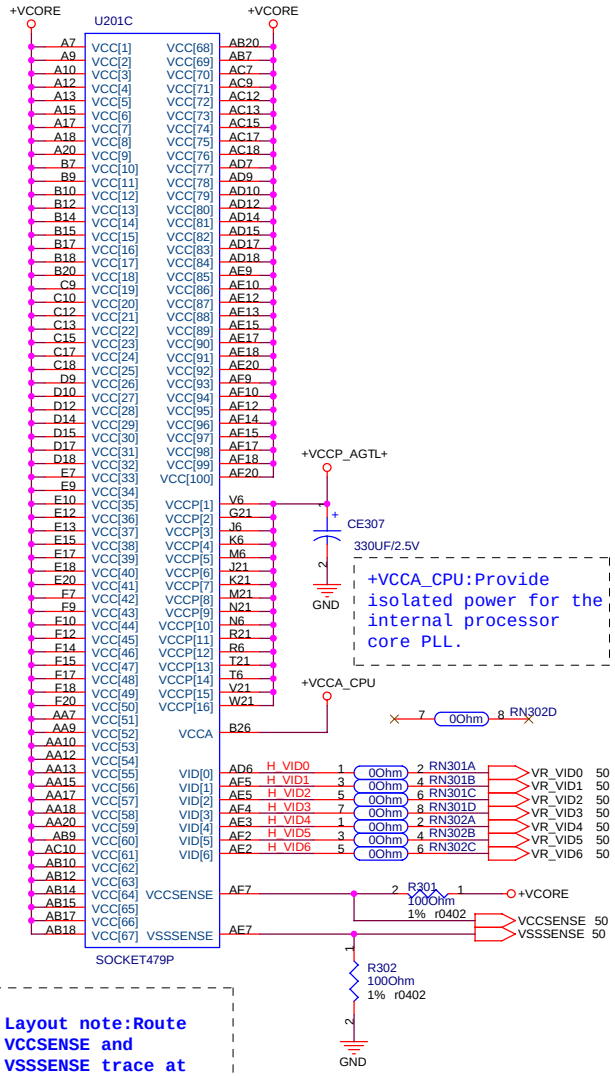
ASUSTeK COMPUTER INC Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 2 of 63

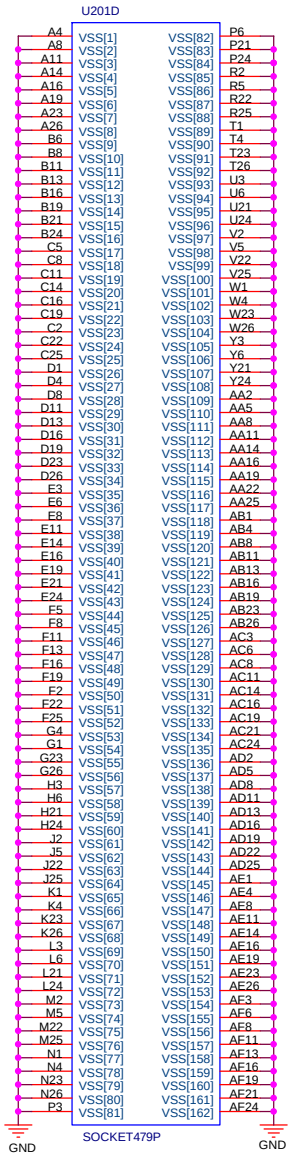
YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

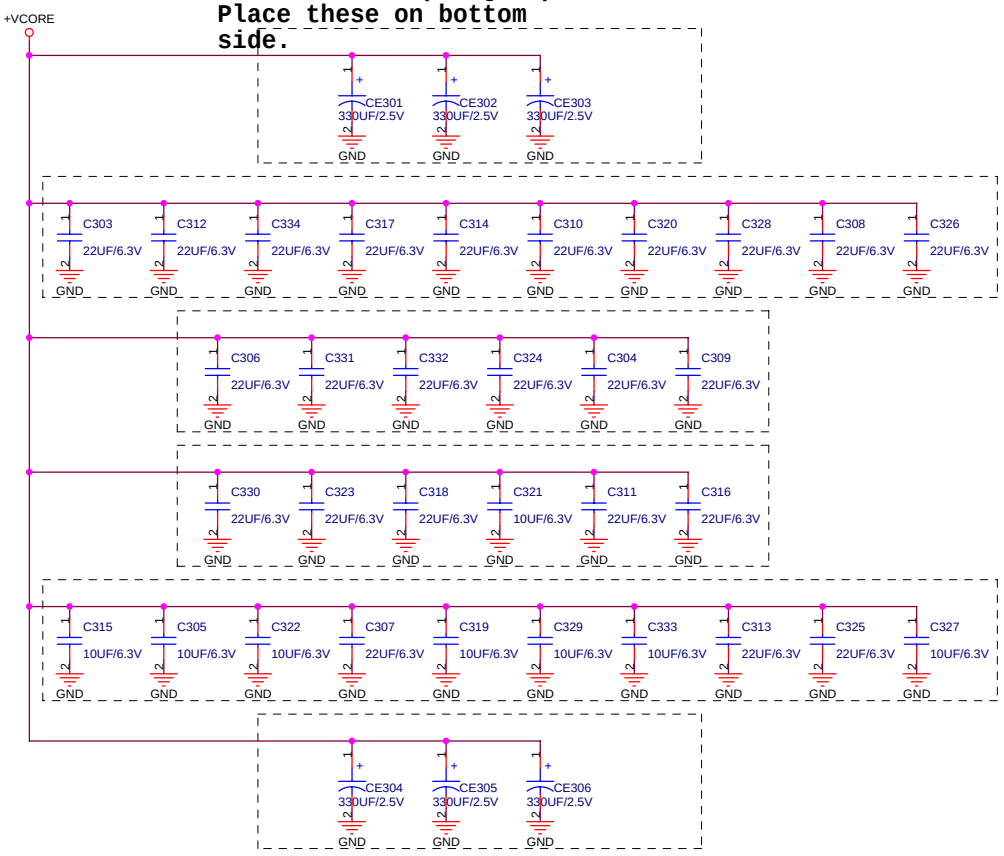


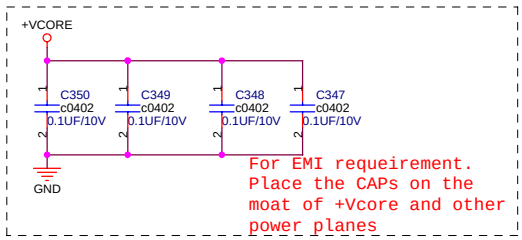
Layout note:Route VCCSENSE and VSSSENSE trace at 27.4 ohm with 25 mils spacing mismatch and 18mils trace on 7mils spacing.

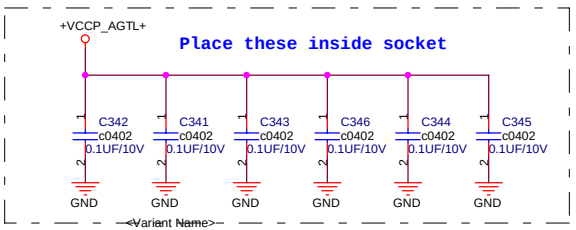
Place pull-up/down resisters within 1 inch of CPU.

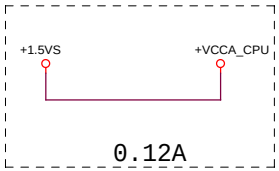


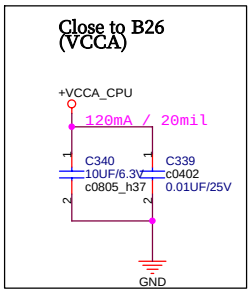
Vcc Core Decoupling Caps Place these on bottom side.











ASUSTeK COMPUTER INC

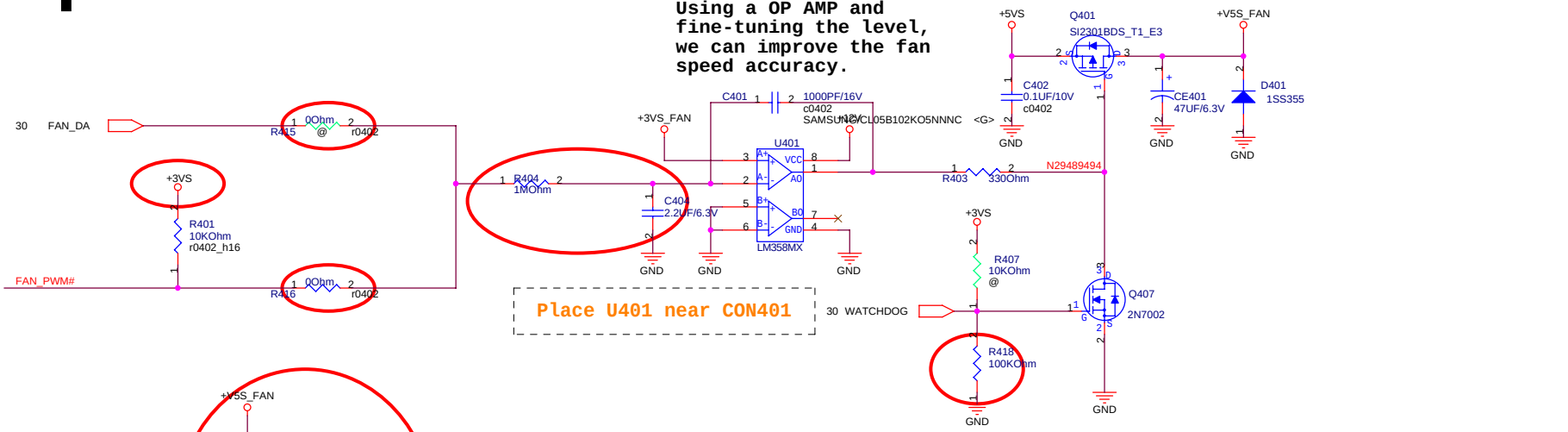
Title : Yonah CPU (2)

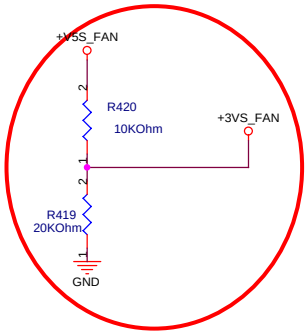
Engineer: *Charles Lee*

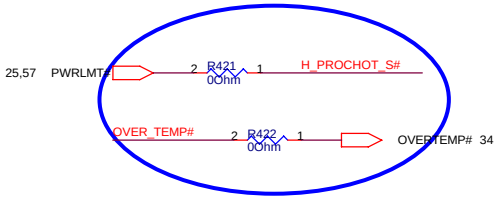
Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 3 of 63

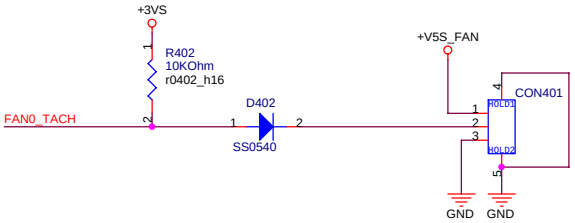
Fan Speed Control

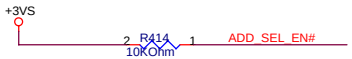


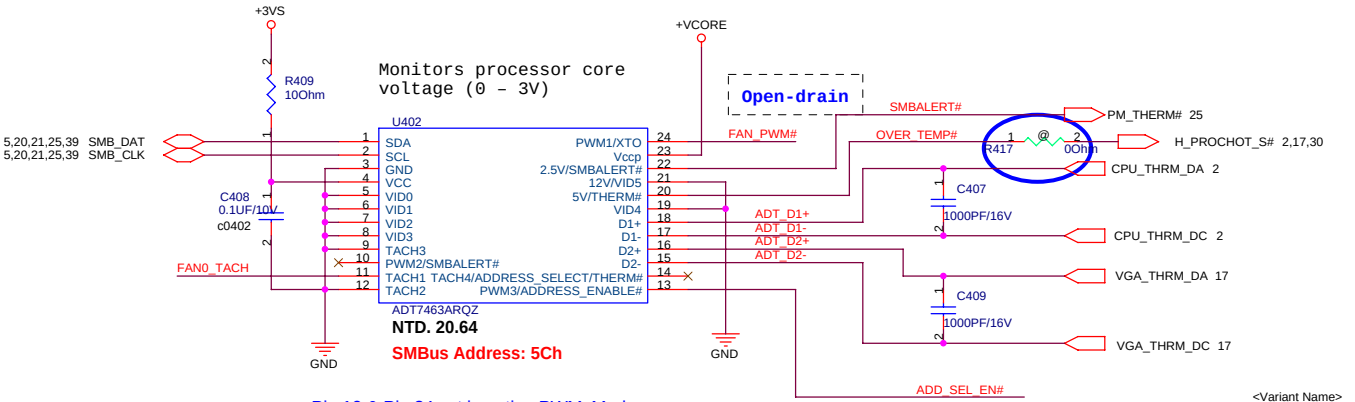




CPU FAN







Pin 10 & Pin 24 set inverting PWM Mode
Set INV=1 to invert PWM output

Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

<Variant Name>

ASUSTeK COMPUTER INC

Title : THER-SENSOR,FAN

Engineer: *Marco Chen*

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 4 of 63

Place termination closed to source IC

		FSLC	FSLB	FSLA
Bclk	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

SMBus Slave Address:D2H

U501

ICS954310BGLFT

Block 1

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD1(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#)	CLK_MCH_3GPLL(#)

<Variant Name>

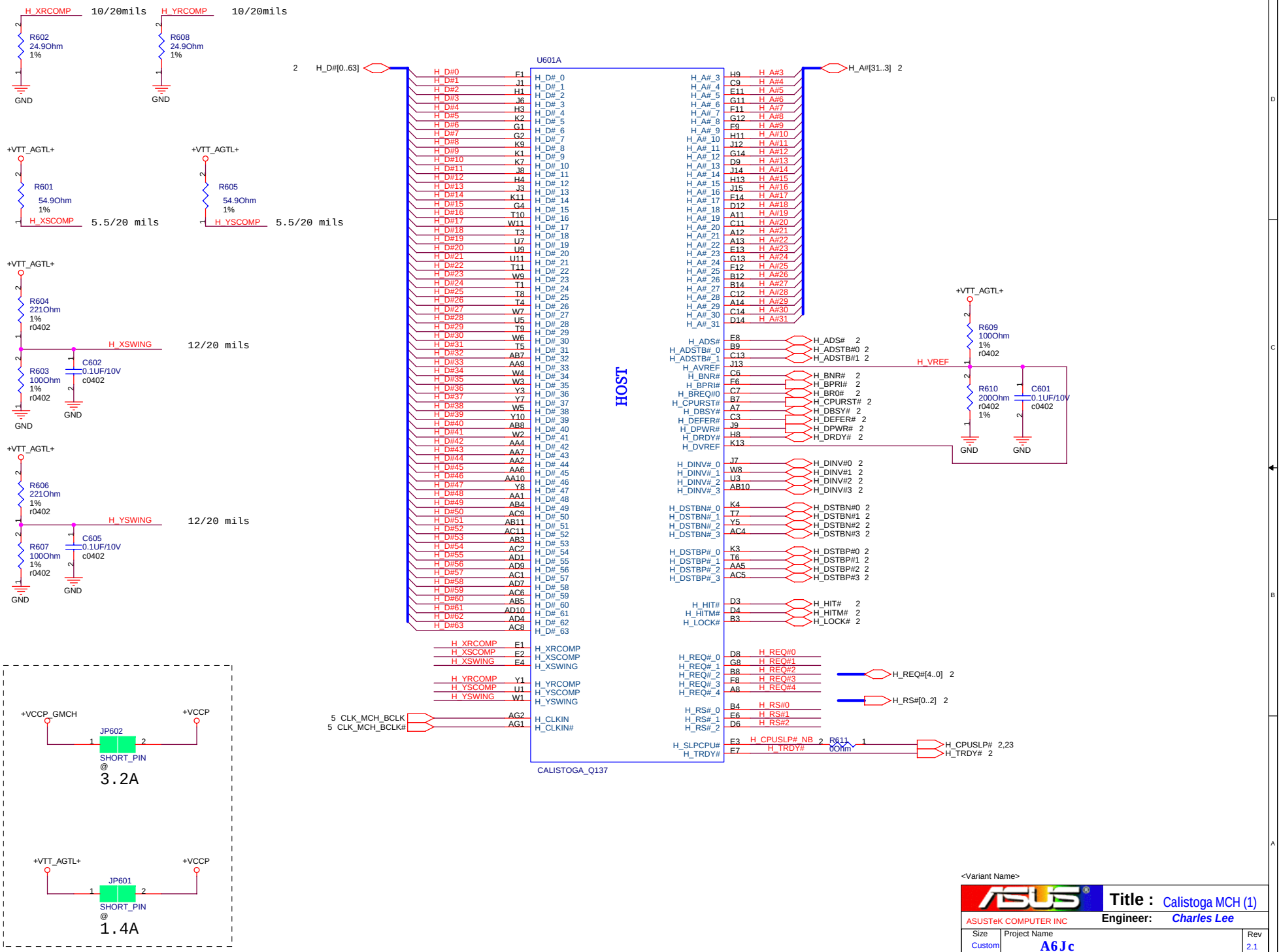
ASUSTeK COMPUTER INC

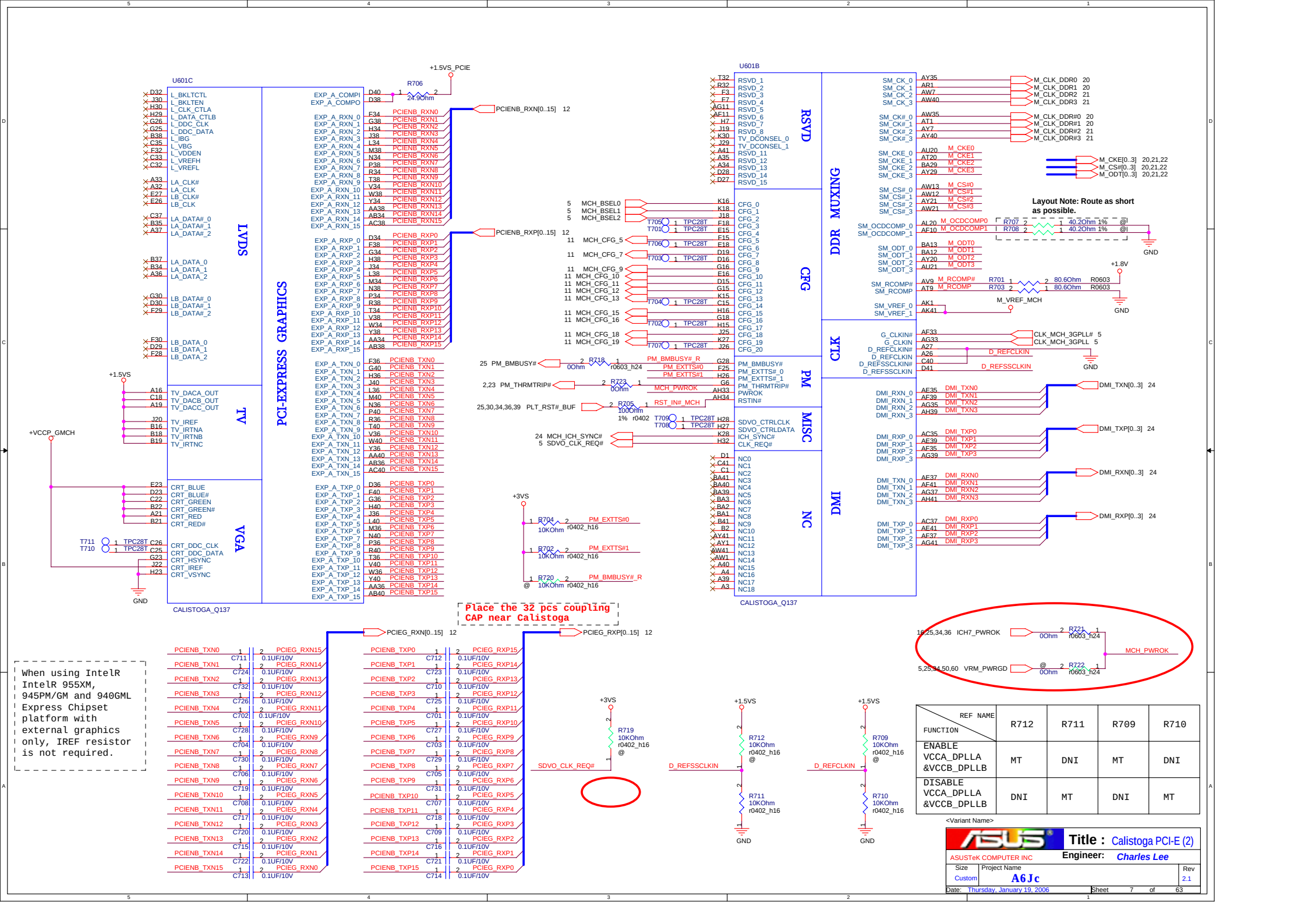
Title : CLOCK GEN

Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 5 of 63


H_XRCOMP 10/20mils
R602 24.9Ohm 1%
GND
H_YRCOMP 10/20mils
R608 24.9Ohm 1%
GND
+VTT_AGTL+
R601 54.9Ohm 1%
H_XSCOMP 5.5/20 mils
+VTT_AGTL+
R605 54.9Ohm 1%
H_YSCOMP 5.5/20 mils
+VTT_AGTL+
R604 221Ohm 1% r0402
H_XSWING 12/20 mils
R603 100Ohm 1% r0402
C602 0.1UF/10V c0402
GND
GND
+VTT_AGTL+
R606 221Ohm 1% r0402
H_YSWING 12/20 mils
R607 100Ohm 1% r0402
C605 0.1UF/10V c0402
GND
GND
+VCCP_GMCH
JP602
SHORT_PIN
@
3.2A
+VCCP
+VTT_AGTL+
JP601
SHORT_PIN
@
1.4A
+VCCP
U601A
HOST
CALISTOGA_Q137
2 H_D#[0..63]
H_D#0 F1
H_D#1 J1
H_D#2 H1
H_D#3 J6
H_D#4 H3
H_D#5 K2
H_D#6 G1
H_D#7 G2
H_D#8 K9
H_D#9 K1
H_D#10 K7
H_D#11 J8
H_D#12 H4
H_D#13 J3
H_D#14 K11
H_D#15 G4
H_D#16 T10
H_D#17 W11
H_D#18 T3
H_D#19 U7
H_D#20 U9
H_D#21 U11
H_D#22 T11
H_D#23 W9
H_D#24 T1
H_D#25 T8
H_D#26 T4
H_D#27 W7
H_D#28 U5
H_D#29 T9
H_D#30 W6
H_D#31 T5
H_D#32 AB7
H_D#33 AA9
H_D#34 W4
H_D#35 W3
H_D#36 Y3
H_D#37 Y7
H_D#38 W5
H_D#39 Y10
H_D#40 AB8
H_D#41 W2
H_D#42 AA4
H_D#43 AA7
H_D#44 AA2
H_D#45 AA6
H_D#46 AA10
H_D#47 Y8
H_D#48 AA1
H_D#49 AB4
H_D#50 AC9
H_D#51 AB11
H_D#52 AC11
H_D#53 AB3
H_D#54 AC2
H_D#55 AD1
H_D#56 AD9
H_D#57 AC1
H_D#58 AD7
H_D#59 AC6
H_D#60 AB5
H_D#61 AD10
H_D#62 AD4
H_D#63 AC8
H_XRCOMP E1
H_XSCOMP E2
H_XSWING E4
H_YRCOMP Y1
H_YSCOMP U1
H_YSWING W1
5 CLK_MCH_BCLK AG2
5 CLK_MCH_BCLK# AG1
H_A#3 H9
H_A#4 C9
H_A#5 E11
H_A#6 G11
H_A#7 F11
H_A#8 G12
H_A#9 F9
H_A#10 H11
H_A#11 J12
H_A#12 G14
H_A#13 D9
H_A#14 J14
H_A#15 H13
H_A#16 J15
H_A#17 F14
H_A#18 D12
H_A#19 A11
H_A#20 C11
H_A#21 A12
H_A#22 A13
H_A#23 E13
H_A#24 G13
H_A#25 F12
H_A#26 B12
H_A#27 B14
H_A#28 C12
H_A#29 A14
H_A#30 C14
H_A#31 D14
H_A#[31..3] 2
H_ADS# E8
H_ADSTB#_0 B9
H_ADSTB#_1 C13
H_AVREF J13
H_BNR# C6
H_BPRI# F6
H_BREQ#0 C7
H_CPURST# B7
H_DBSY# A7
H_DEFER# C3
H_DPWR# J9
H_DRDY# H8
H_DVREF K13
H_ADS# 2
H_ADSTB#0 2
H_ADSTB#1 2
H_BNR# 2
H_BPRI# 2
H_BR0# 2
H_CPURST# 2
H_DBSY# 2
H_DEFER# 2
H_DPWR# 2
H_DRDY# 2
H_VREF
+VTT_AGTL+
R609 100Ohm 1% r0402
R610 200Ohm r0402 1%
C601 0.1UF/10V c0402
GND
GND
H_DINV#_0 J7
H_DINV#_1 W8
H_DINV#_2 U3
H_DINV#_3 AB10
H_DINV#0 2
H_DINV#1 2
H_DINV#2 2
H_DINV#3 2
H_DSTBN#_0 K4
H_DSTBN#_1 T7
H_DSTBN#_2 Y5
H_DSTBN#_3 AC4
H_DSTBN#0 2
H_DSTBN#1 2
H_DSTBN#2 2
H_DSTBN#3 2
H_DSTBP#_0 K3
H_DSTBP#_1 T6
H_DSTBP#_2 AA5
H_DSTBP#_3 AC5
H_DSTBP#0 2
H_DSTBP#1 2
H_DSTBP#2 2
H_DSTBP#3 2
H_HIT# D3
H_HITM# D4
H_LOCK# B3
H_HIT# 2
H_HITM# 2
H_LOCK# 2
H_REQ#_0 D8
H_REQ#_1 G8
H_REQ#_2 B8
H_REQ#_3 F8
H_REQ#_4 A8
H_REQ#0
H_REQ#1
H_REQ#2
H_REQ#3
H_REQ#4
H_REQ#[4..0] 2
H_RS#_0 B4
H_RS#_1 E6
H_RS#_2 D6
H_RS#0
H_RS#1
H_RS#2
H_RS#[0..2] 2
H_SLPCPU# E3
H_TRDY# E7
H_CPUSLP# NB 2
H_TRDY#
R611 0Ohm
H_CPUSLP# 2,23
H_TRDY# 2
<Variant Name>
Title : Calistoga MCH (1)
ASUSTeK COMPUTER INC
Engineer: Charles Lee
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 6 of 63



REF NAME / FUNCTION	R712	R711	R709	R710
ENABLE VCCA_DPLLA &VCCB_DPLLB	MT	DNI	MT	DNI
DISABLE VCCA_DPLLA &VCCB_DPLLB	DNI	MT	DNI	MT

<Variant Name>

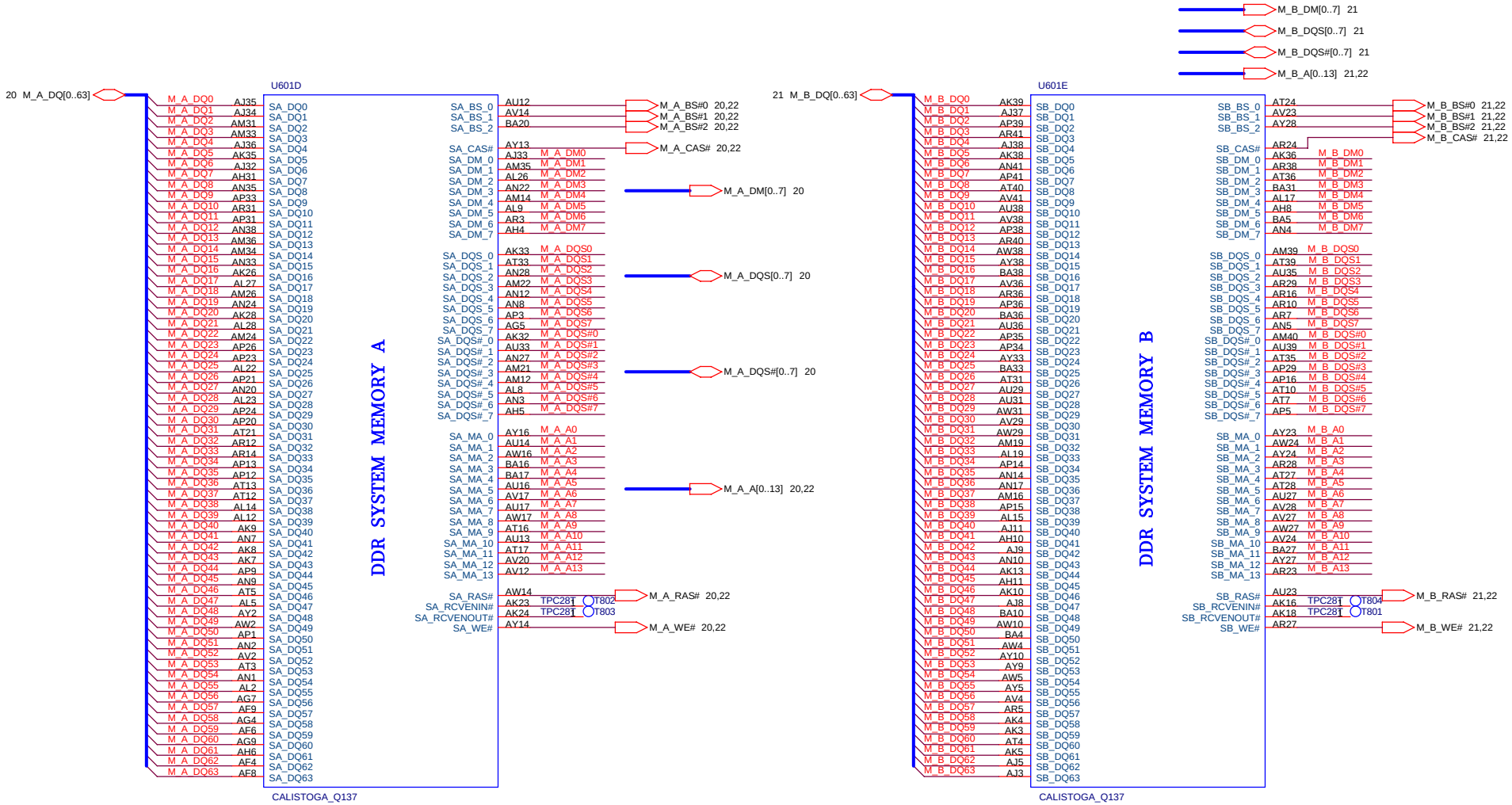
ASUSTeK COMPUTER INC

Title : Calistoga PCI-E (2)

Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 7 of 63



<variant_name>

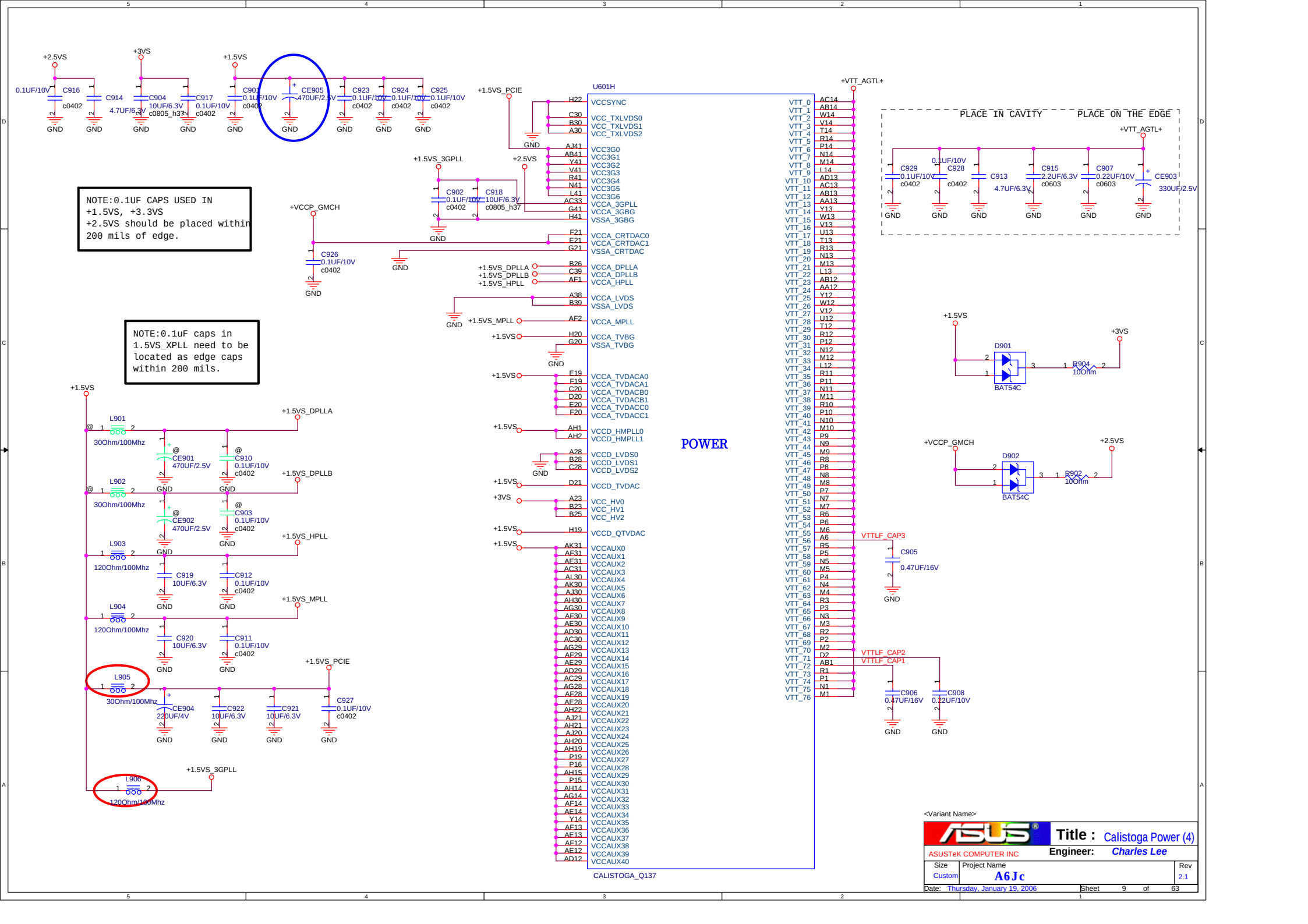
ASUSTeK COMPUTER INC

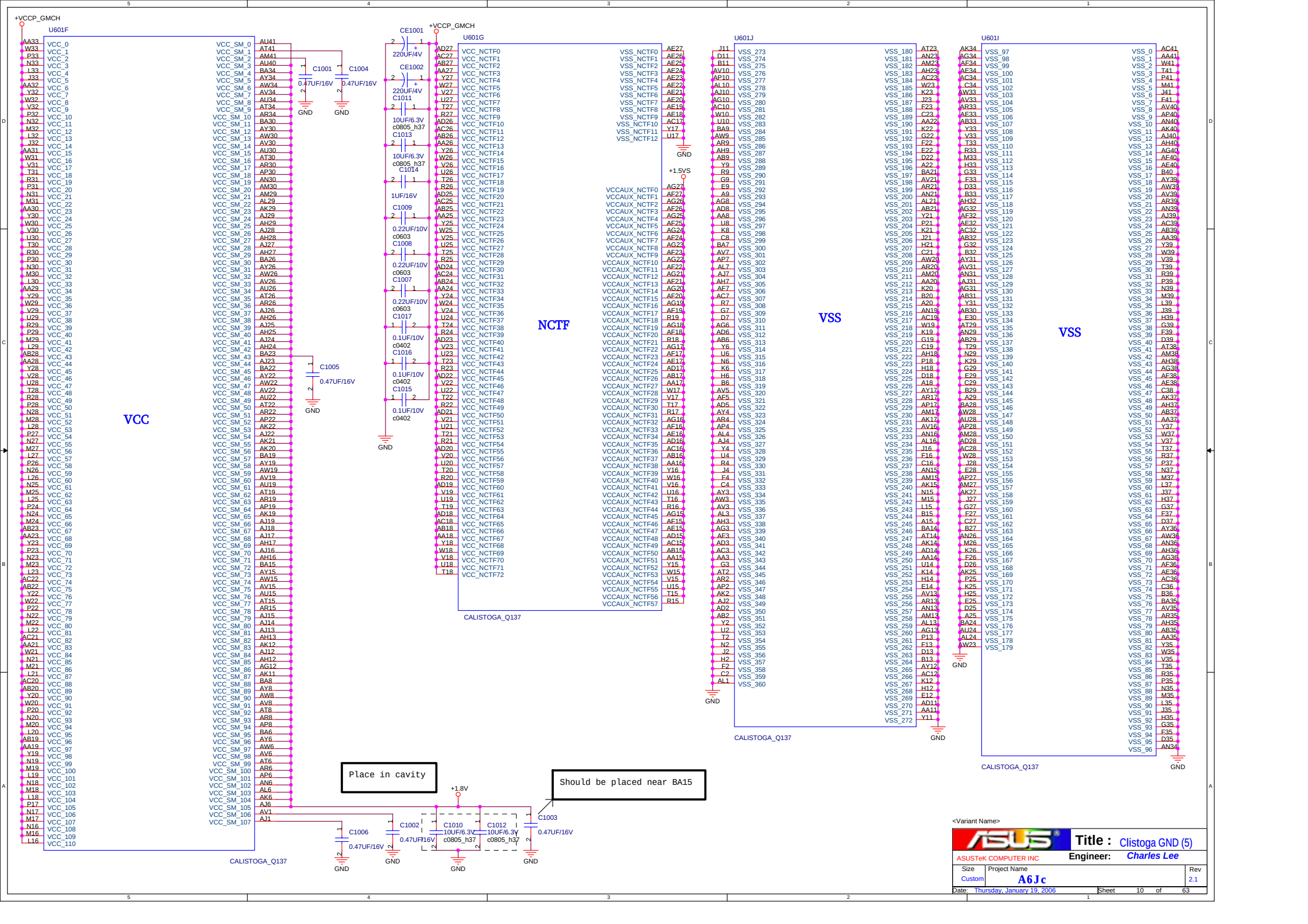
Title : Calistoga DDR2 (3)

Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 8 of 63

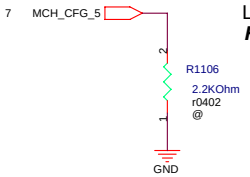

NOTE:0.1UF CAPS USED IN
+1.5VS, +3.3VS
+2.5VS should be placed within
200 mils of edge.
NOTE:0.1uF caps in
1.5VS_XPLL need to be
located as edge caps
within 200 mils.
POWER
U601H
CALISTOGA_Q137
PLACE IN CAVITY
PLACE ON THE EDGE
+2.5VS
+3VS
+1.5VS
+1.5VS_PCIE
+1.5VS_3GPLL
+VCCP_GMCH
+VTT_AGTL+
+1.5VS_DPLLA
+1.5VS_DPLLB
+1.5VS_HPLL
+1.5VS_MPLL
VTTLF_CAP3
VTTLF_CAP2
VTTLF_CAP1
D901
D902
BAT54C
R904
R902
10Ohm
L901
L902
L903
L904
L905
L906
30Ohm/100Mhz
120Ohm/100Mhz
C916
C914
C904
C917
C901
CE905
C923
C924
C925
C902
C918
C926
C929
C928
C913
C915
C907
CE903
C905
C906
C908
CE901
CE902
CE904
C910
C903
C919
C912
C920
C911
C922
C921
C927
GND
<Variant Name>
Title : Calistoga Power (4)
ASUSTeK COMPUTER INC
Engineer: Charles Lee
Size: Custom
Project Name: A6Jc
Rev: 2.1
Date: Thursday, January 19, 2006
Sheet 9 of 63


+VCCP_GMCH
U601F
VCC
CALISTOGA_Q137
C1001
C1004
C1005
0.47UF/16V
GND
CE1001
CE1002
220UF/4V
C1011
10UF/6.3V
c0805_h37
C1013
C1014
1UF/16V
C1009
0.22UF/10V
c0603
C1008
C1007
C1017
0.1UF/10V
c0402
C1016
C1015
U601G
NCTF
U601J
VSS
U601I
Place in cavity
Should be placed near BA15
+1.8V
C1006
C1002
C1010
C1012
C1003
+1.5VS
<Variant Name>
Title : Clistoga GND (5)
ASUSTeK COMPUTER INC
Engineer: Charles Lee
Size: Custom
Project Name: A6Jc
Rev: 2.1
Date: Thursday, January 19, 2006
Sheet 10 of 63

CFG[17..3] have internal pullup resistors.
CFG[20..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

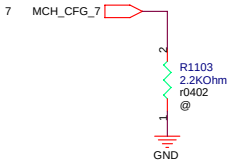
CFG5 : DMI STRAP

LOW = DMI X 2
HIGH = DMI X 4 (Default)



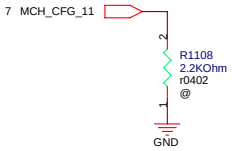
CFG7 : CPU STRAP

LOW = Mobile Prescott
HIGH = Dothan CPU (Default)



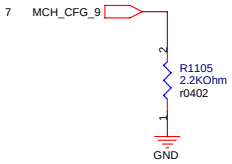
CFG11 : PSB 4X CLK ENABLE

LOW = REVERSAL
HIGH =Calistoga(Default)



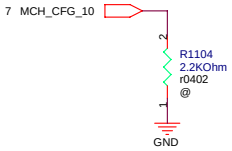
CFG9 : PCIE GRAPHIC LANE

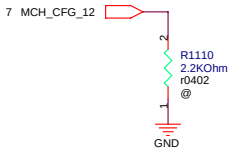
LOW = REVERSE LANE (Default)
HIGH = NORMAL OPERATION

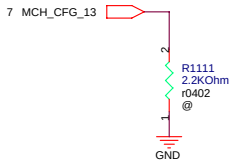


CFG10: HOST PLL VCO SELECT

LOW = RESERVED
HIGH = MOBILITY

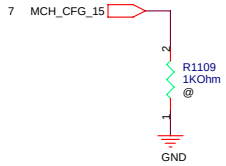






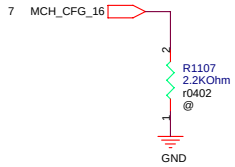
CFG15 :ICH RESET DISABLE

LOW = ICH RESET DISABLE
HIGH = NORMAL OPERATION



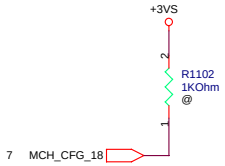
CFG16 : FSB DYNAMIC ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



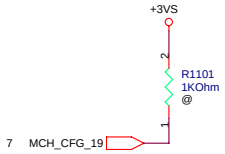
CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)
HIGH = 1.5V



CFG19 : DMI LANE REVERSAL

LOW = NORMAL
HIGH = LANES REVERSED



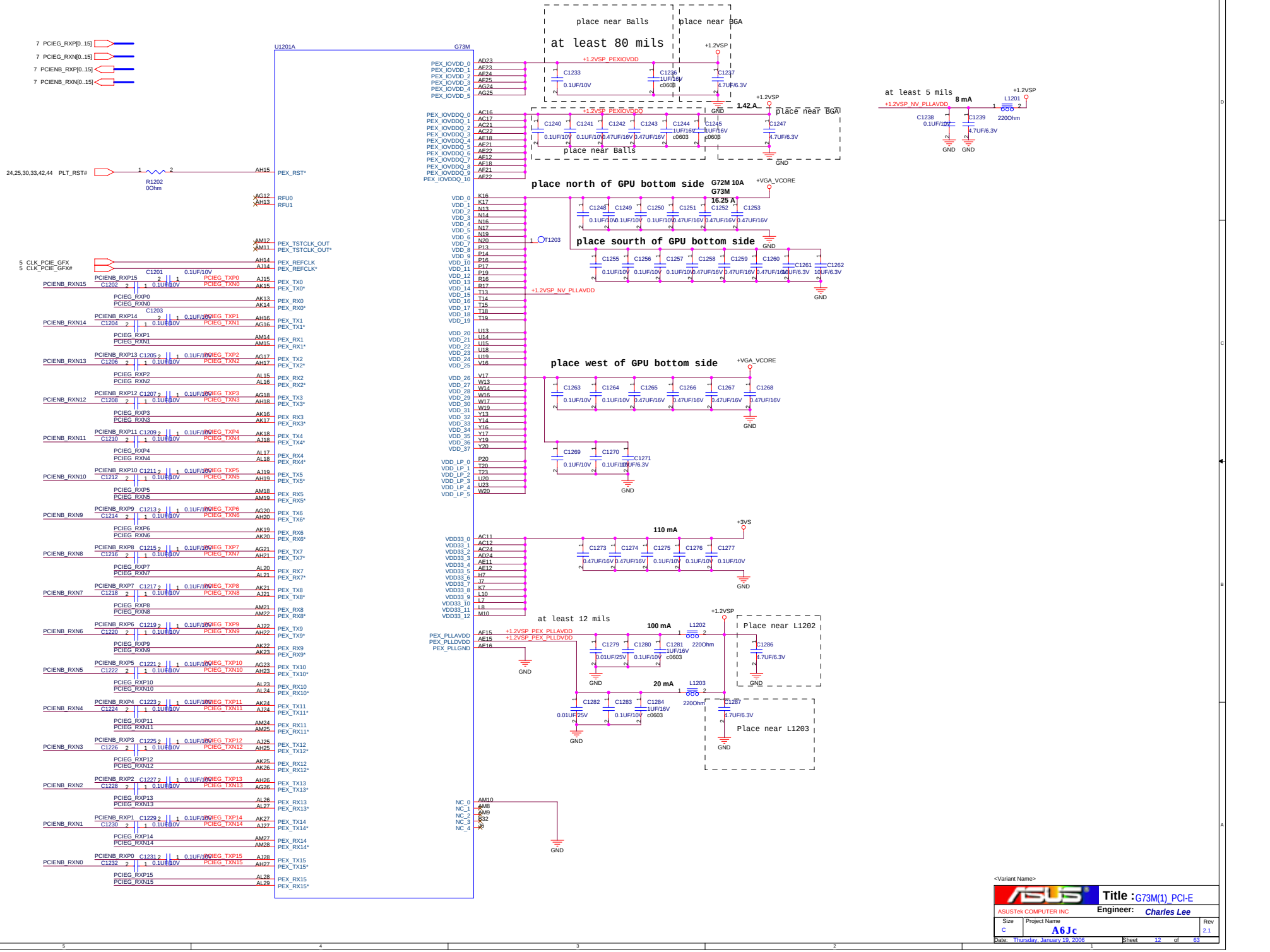
<Variant Name>

Title : Calistoga Strapping

ASUSTeK COMPUTER INC **Engineer:** *Charles Lee*

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 11 of 63



<Variant Name>

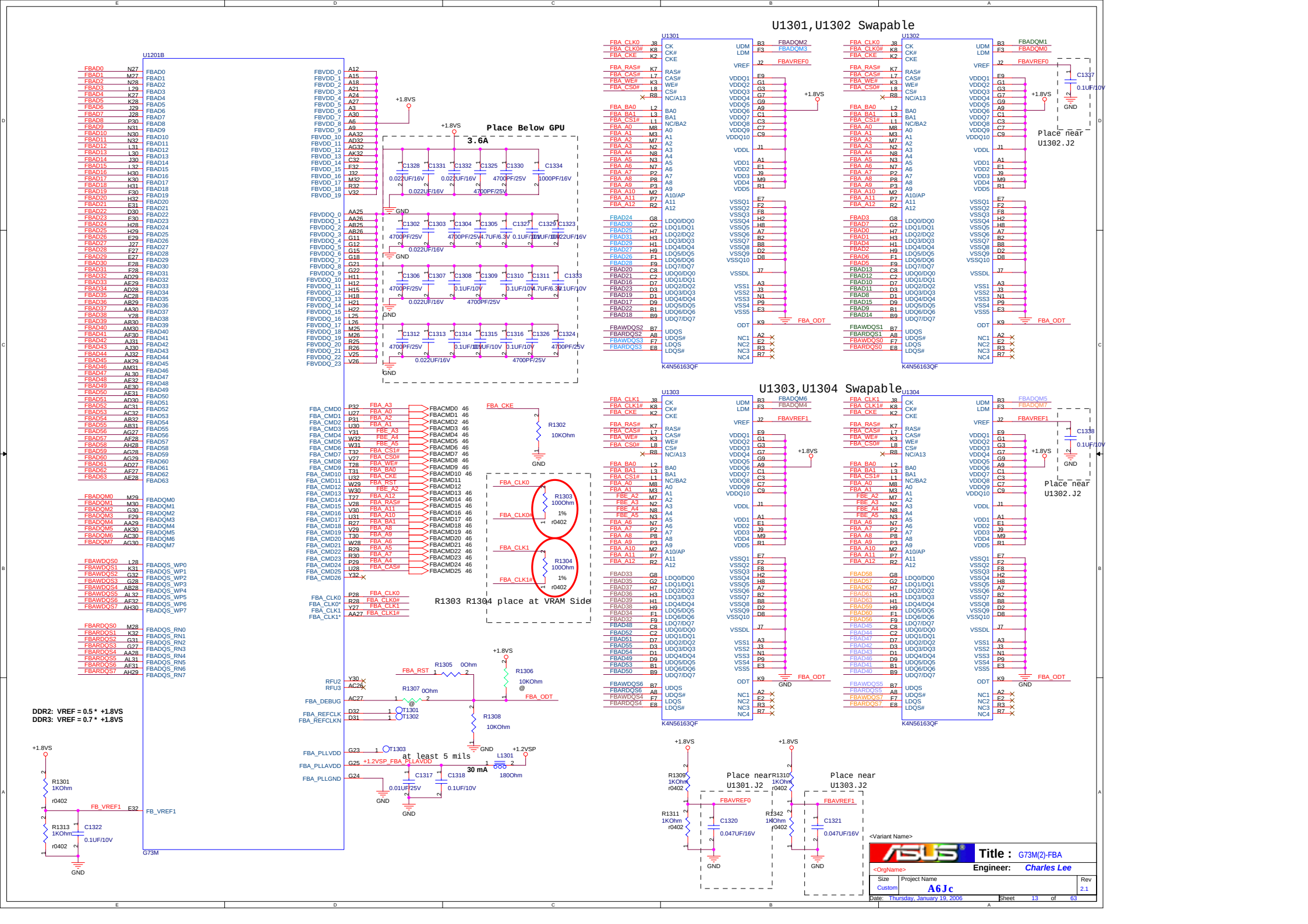
ASUSTek COMPUTER INC

Title : G73M(1)_PCI-E

Engineer: Charles Lee

Size	Project Name	Rev
C	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 12 of 63


U1301,U1302 Swapable
U1303,U1304 Swapable
U1201B
G73M
U1301
U1302
U1303
U1304
K4N56163QF
Place Below GPU
3.6A
Place near U1302.J2
Place near U1301.J2
Place near U1303.J2
Place near U1304.J2
R1303 R1304 place at VRAM Side
at least 5 mils
30 mA
DDR2: VREF = 0.5 * +1.8VS
DDR3: VREF = 0.7 * +1.8VS
+1.8VS
+1.2VSP
GND
FBA_ODT
FBAVREF0
FBAVREF1
FB_VREF1
Title : G73M(2)-FBA
Engineer: Charles Lee
Project Name A6Jc
Rev 2.1
Sheet 13 of 63
Date: Thursday, January 19, 2006

DDR2 Terminated FBVTT=0.5* +1.8VS
Unterminated FBVTT=+1.8VS

U1201C

G73M

U1401,U1402 Swapable

U1401

U1402

K4N56163QF

U1403,U1404 Swapable

U1403

U1404

K4N56163QF

R1402 R1403 place at VRAM Side

at least 5 mils

30 mA

place near U1402.J2

place near U1404.J2

place near U1401.J2

place near U1403.J2

TPC28t

<Variant Name>

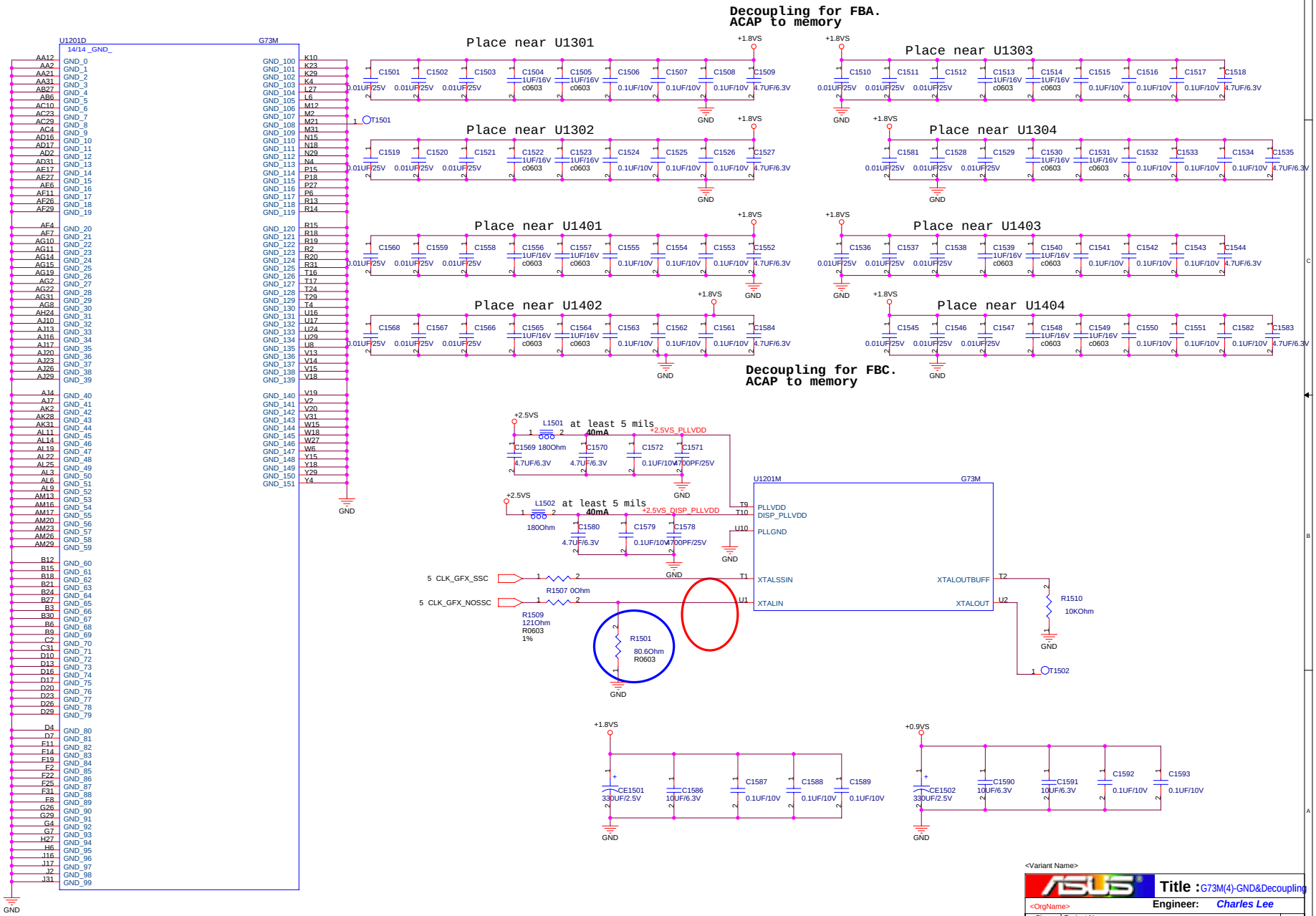
Title : G73M(3)-FBC

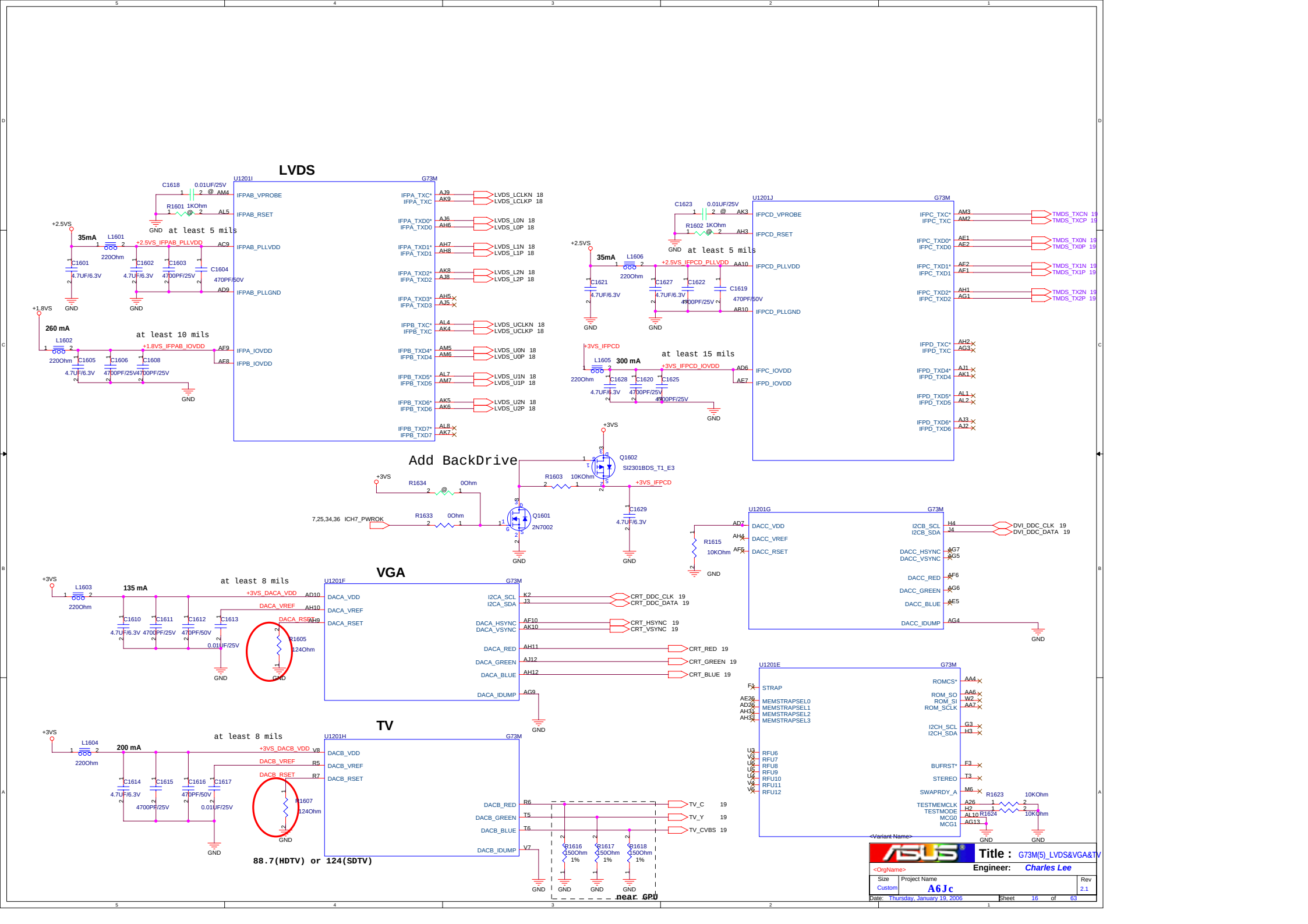
<OrgName>

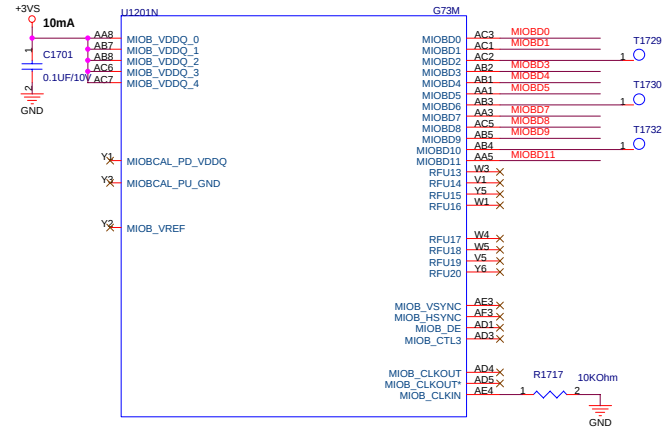
Engineer: Charles Lee

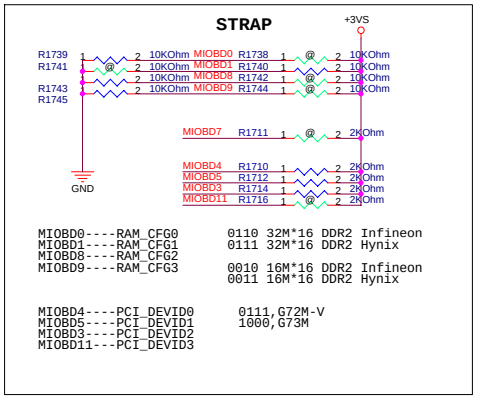
Size	Project Name	Rev
Custom	A6Jc	2.1

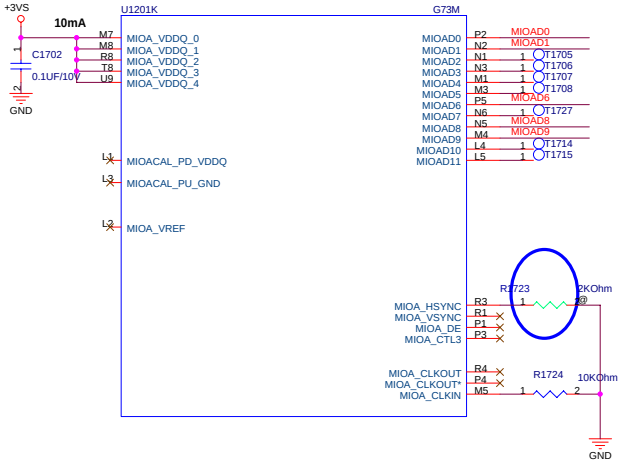
Date: Thursday, January 19, 2006 Sheet 14 of 63

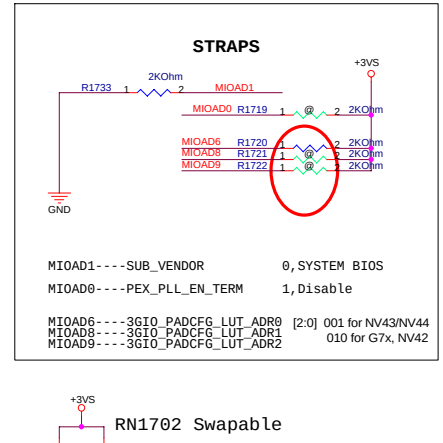

Decoupling for FBA.
ACAP to memory
U1201D
G73M
14/14 _GND_
Place near U1301
Place near U1302
Place near U1303
Place near U1304
Place near U1401
Place near U1402
Place near U1403
Place near U1404
+1.8VS
GND
C1501 C1502 C1503 C1504 C1505 C1506 C1507 C1508 C1509
C1510 C1511 C1512 C1513 C1514 C1515 C1516 C1517 C1518
C1519 C1520 C1521 C1522 C1523 C1524 C1525 C1526 C1527
C1581 C1528 C1529 C1530 C1531 C1532 C1533 C1534 C1535
C1560 C1559 C1558 C1556 C1557 C1555 C1554 C1553 C1552
C1536 C1537 C1538 C1539 C1540 C1541 C1542 C1543 C1544
C1568 C1567 C1566 C1565 C1564 C1563 C1562 C1561 C1584
C1545 C1546 C1547 C1548 C1549 C1550 C1551 C1582 C1583
0.01UF/25V
1UF/16V
c0603
0.1UF/10V
4.7UF/6.3V
T1501
Decoupling for FBC.
ACAP to memory
+2.5VS
L1501 at least 5 mils
40mA
+2.5VS_PLLVDD
C1569 180Ohm
C1570 4.7UF/6.3V
C1572 0.1UF/10V
C1571 4700PF/25V
L1502 at least 5 mils
+2.5VS_DISP_PLLVDD
180Ohm
C1580 4.7UF/6.3V
C1579 0.1UF/10V
C1578 4700PF/25V
U1201M
G73M
PLLVDD
DISP_PLLVDD
PLLGND
5 CLK_GFX_SSC
5 CLK_GFX_NOSSC
R1507 0Ohm
R1509 121Ohm R0603 1%
R1501 80.6Ohm R0603
XTALSSIN
XTALIN
XTALOUTBUFF
XTALOUT
R1510 10KOhm
T1502
+1.8VS
+0.9VS
CE1501 330UF/2.5V
C1586 10UF/6.3V
C1587 0.1UF/10V
C1588 0.1UF/10V
C1589 0.1UF/10V
CE1502 330UF/2.5V
C1590 10UF/6.3V
C1591 10UF/6.3V
C1592 0.1UF/10V
C1593 0.1UF/10V
<Variant Name>
Title : G73M(4)-GND&Decoupling
<OrgName>
Engineer: Charles Lee
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 15 of 63

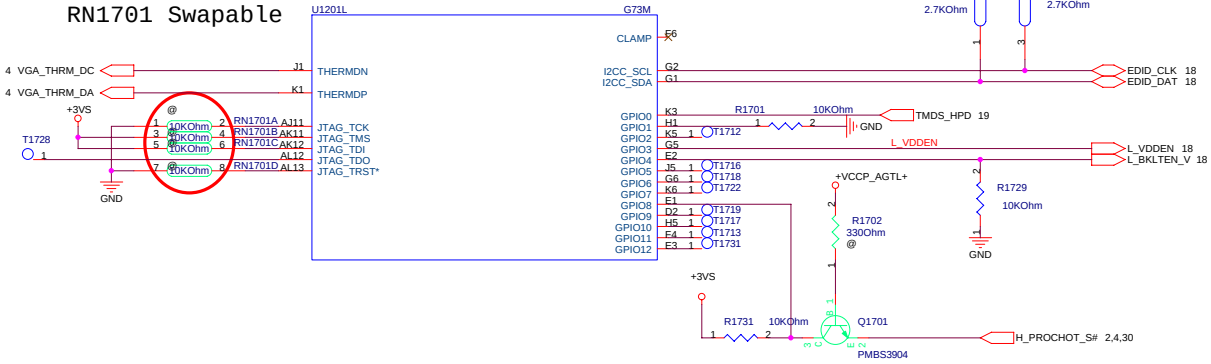

LVDS
U1201I
G73M
C1618
0.01UF/25V
R1601 1KOhm
GND at least 5 mils
+2.5VS
35mA
L1601
220Ohm
+2.5VS_IFPAB_PLLVDD
C1601
4.7UF/6.3V
C1602
4.7UF/6.3V
C1603
4700PF/25V
C1604
470PF/50V
+1.8VS
260 mA
L1602
220Ohm
at least 10 mils
+1.8VS_IFPAB_IOVDD
C1605
4.7UF/6.3V
C1606
4700PF/25V
C1608
4700PF/25V
IFPAB_VPROBE
IFPAB_RSET
IFPAB_PLLVDD
IFPAB_PLLGND
IFPA_IOVDD
IFPB_IOVDD
IFPA_TXC*
IFPA_TXC
IFPA_TXD0*
IFPA_TXD0
IFPA_TXD1*
IFPA_TXD1
IFPA_TXD2*
IFPA_TXD2
IFPA_TXD3*
IFPA_TXD3
IFPB_TXC*
IFPB_TXC
IFPB_TXD4*
IFPB_TXD4
IFPB_TXD5*
IFPB_TXD5
IFPB_TXD6*
IFPB_TXD6
IFPB_TXD7*
IFPB_TXD7
LVDS_LCLKN 18
LVDS_LCLKP 18
LVDS_L0N 18
LVDS_L0P 18
LVDS_L1N 18
LVDS_L1P 18
LVDS_L2N 18
LVDS_L2P 18
LVDS_UCLKN 18
LVDS_UCLKP 18
LVDS_U0N 18
LVDS_U0P 18
LVDS_U1N 18
LVDS_U1P 18
LVDS_U2N 18
LVDS_U2P 18
U1201J
G73M
C1623
0.01UF/25V
R1602 1KOhm
GND at least 5 mils
+2.5VS
35mA
L1606
220Ohm
+2.5VS_IFPCD_PLLVDD
C1621
4.7UF/6.3V
C1627
4.7UF/6.3V
C1622
4700PF/25V
C1619
470PF/50V
+3VS_IFPCD
L1605
300 mA
220Ohm
at least 15 mils
+3VS_IFPCD_IOVDD
C1628
4.7UF/6.3V
C1620
4700PF/25V
C1625
4700PF/25V
IFPCD_VPROBE
IFPCD_RSET
IFPCD_PLLVDD
IFPCD_PLLGND
IFPC_IOVDD
IFPD_IOVDD
IFPC_TXC*
IFPC_TXC
IFPC_TXD0*
IFPC_TXD0
IFPC_TXD1*
IFPC_TXD1
IFPC_TXD2*
IFPC_TXD2
IFPD_TXC*
IFPD_TXC
IFPD_TXD4*
IFPD_TXD4
IFPD_TXD5*
IFPD_TXD5
IFPD_TXD6*
IFPD_TXD6
TMDS_TXCN 19
TMDS_TXCP 19
TMDS_TX0N 19
TMDS_TX0P 19
TMDS_TX1N 19
TMDS_TX1P 19
TMDS_TX2N 19
TMDS_TX2P 19
Add BackDrive
+3VS
R1634 0Ohm
7,25,34,36 ICH7_PWROK
R1633 0Ohm
Q1601
2N7002
R1603 10KOhm
Q1602
SI2301BDS_T1_E3
+3VS_IFPCD
C1629
4.7UF/6.3V
U1201G
G73M
DACC_VDD
DACC_VREF
DACC_RSET
R1615
10KOhm
I2CB_SCL
I2CB_SDA
DACC_HSYNC
DACC_VSYNC
DACC_RED
DACC_GREEN
DACC_BLUE
DACC_IDUMP
DVI_DDC_CLK 19
DVI_DDC_DATA 19
VGA
+3VS
L1603
135 mA
220Ohm
at least 8 mils
C1610
4.7UF/6.3V
C1611
4700PF/25V
C1612
470PF/50V
C1613
0.01UF/25V
R1605
124Ohm
+3VS_DACA_VDD
DACA_VREF
DACA_RSET
U1201F
G73M
DACA_VDD
DACA_VREF
DACA_RSET
I2CA_SCL
I2CA_SDA
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
DACA_IDUMP
CRT_DDC_CLK 19
CRT_DDC_DATA 19
CRT_HSYNC 19
CRT_VSYNC 19
CRT_RED 19
CRT_GREEN 19
CRT_BLUE 19
TV
+3VS
L1604
200 mA
220Ohm
at least 8 mils
C1614
4.7UF/6.3V
C1615
4700PF/25V
C1616
470PF/50V
C1617
0.01UF/25V
R1607
124Ohm
+3VS_DACB_VDD
DACB_VREF
DACB_RSET
U1201H
G73M
DACB_VDD
DACB_VREF
DACB_RSET
DACB_RED
DACB_GREEN
DACB_BLUE
DACB_IDUMP
TV_C 19
TV_Y 19
TV_CVBS 19
R1616 150Ohm 1%
R1617 150Ohm 1%
R1618 150Ohm 1%
88.7(HDTV) or 124(SDTV)
near GPU
U1201E
G73M
STRAP
MEMSTRAPSEL0
MEMSTRAPSEL1
MEMSTRAPSEL2
MEMSTRAPSEL3
RFU6
RFU7
RFU8
RFU9
RFU10
RFU11
RFU12
ROMCS*
ROM_SO
ROM_SI
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*
STEREO
SWAPRDY_A
TESTMEMCLK
TESTMODE
MCG0
MCG1
R1623 10KOhm
R1624 10KOhm
<Variant Name>
Title : G73M(5)_LVDS&VGA&TV
<OrgName>
Engineer: Charles Lee
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 16 of 63











GPIO0, 1 -- Hot Plug Detect (For DVI)
GPIO2 -- Panel backlight brightness (PWM),
GPIO3 -- Panel power enable
GPIO4 -- Panel backlight ON/OFF
GPIO5 -- GPU VID0
GPIO6 -- GPU VID1
GPIO7 -- GPU VID2 or MEM VID
GPIO8 -- Thermal diode ALERT
GPIO9 -- Fan control
GPIO11 -- HDTV enable

Internal Pull-down
GPIO0, 1, 2, 4, 5, 6, 7

<Variant Name>

Title : G73M(6)_MIOBD&GPIO

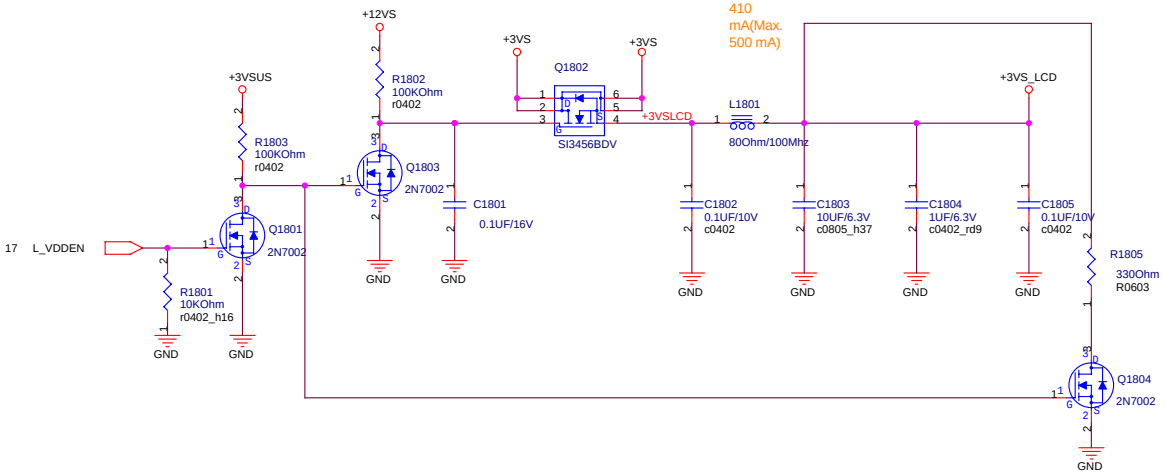
<OrgName> Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6Jc	2.1

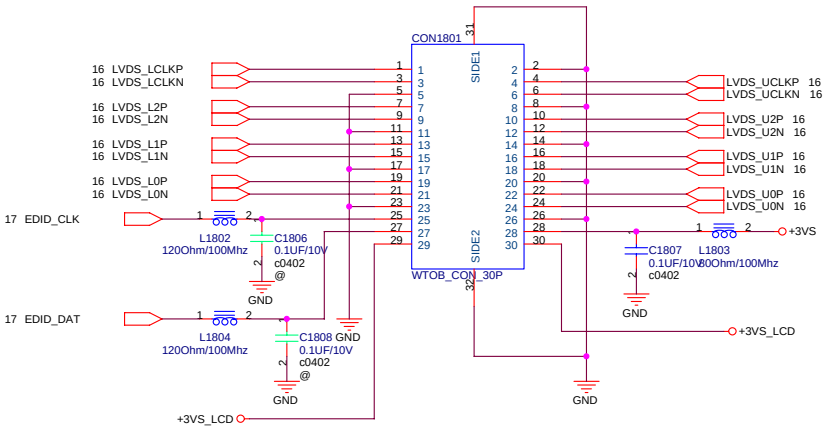
Date: Thursday, January 19, 2006 Sheet 17 of 63

LCD Power

3V-3.6V Full Active: 410 mA(Max. 500 mA)



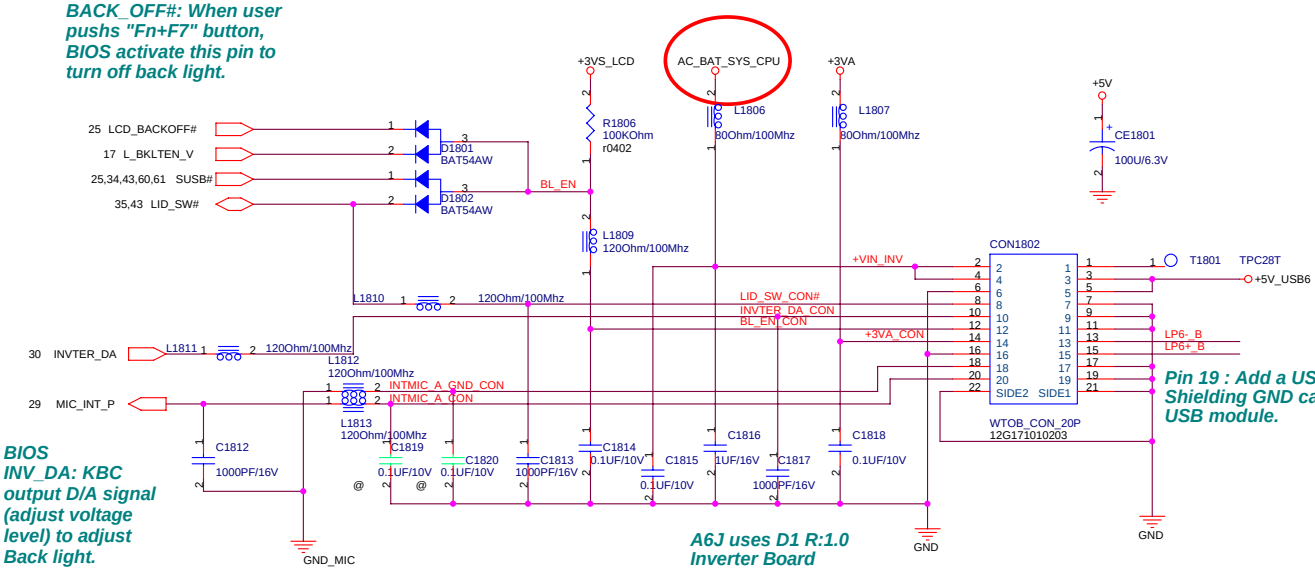
LCD LVDS Interface



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

INVERTER Interface

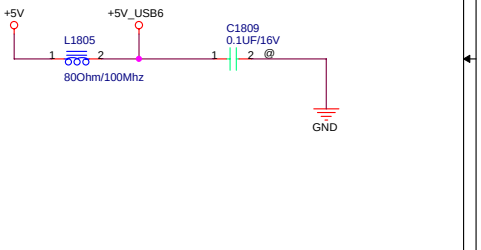
BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.



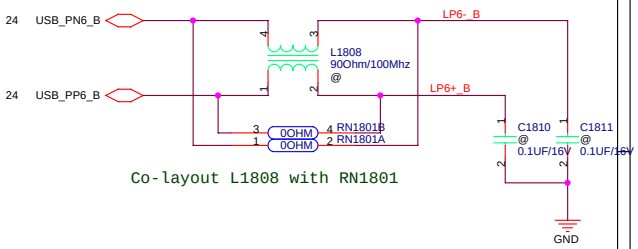
BIOS
INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.

A6J uses D1 R:1.0 Inverter Board

Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.

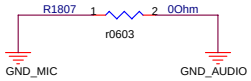


USB PORT 6 for USB CAMERA



Co-layout L1808 with RN1801

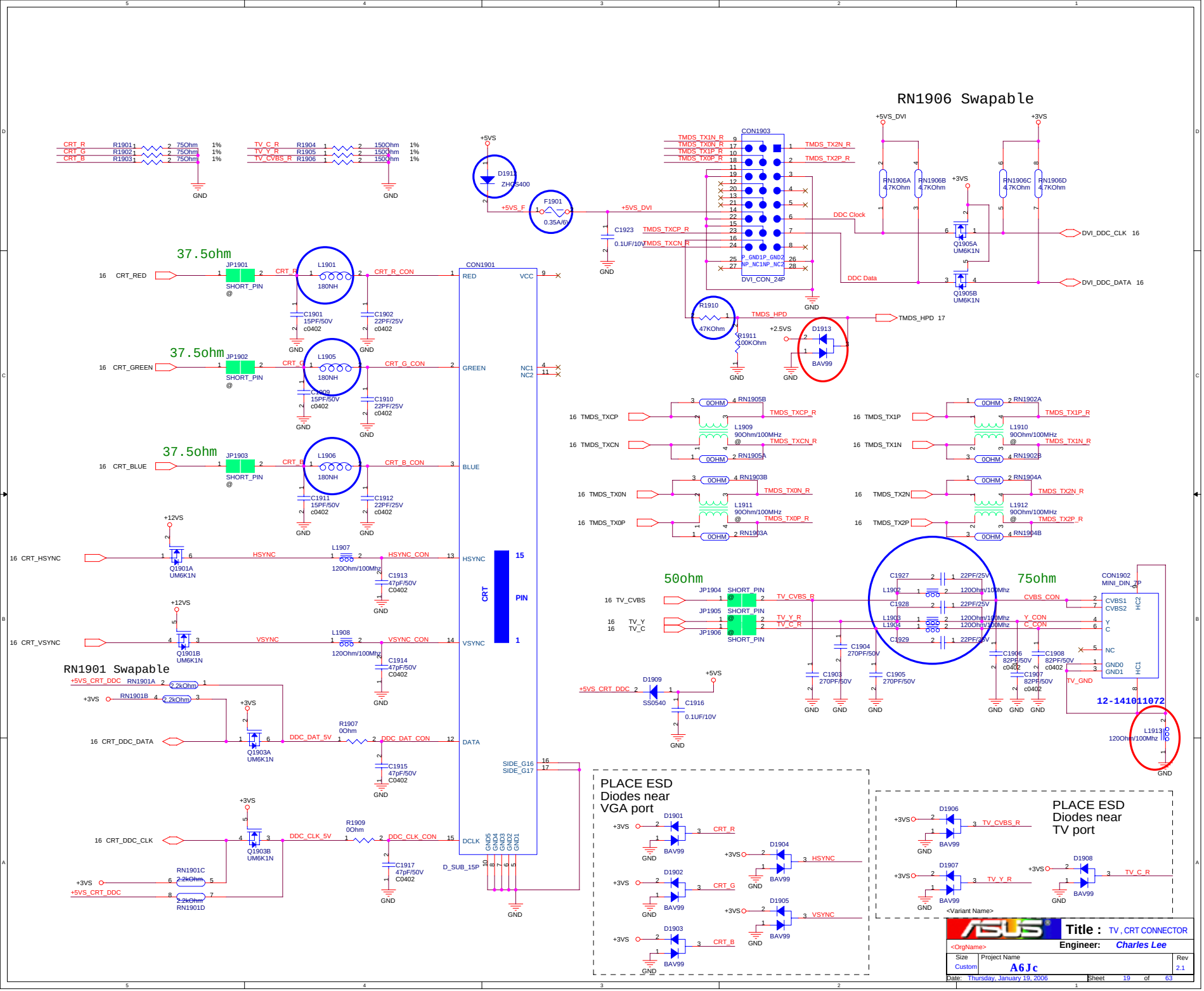
For EMI

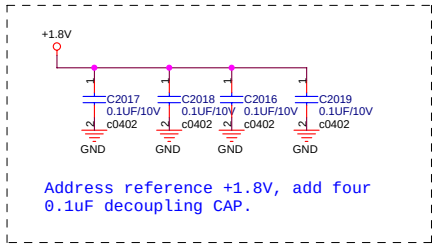


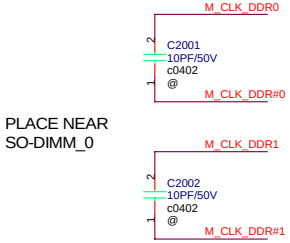
A6J doesn't support USB WLAN function!

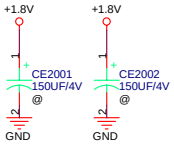
<Variant Name>

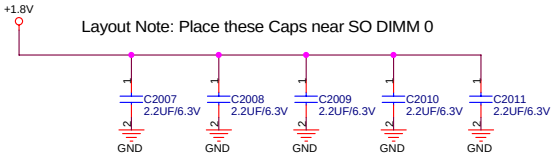
<OrgName>	Title : LVDS & INVERTER	
	Engineer: Charles Lee	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 18 of 63	


RN1906 Swapable
RN1901 Swapable
37.5ohm
37.5ohm
37.5ohm
50ohm
75ohm
CON1901
CON1903
DVI_CON_24P
CON1902
MINI_DIN_7P
12-141011072
PLACE ESD
Diodes near
VGA port
PLACE ESD
Diodes near
TV port
<Variant Name>
Title : TV , CRT CONNECTOR
<OrgName>
Engineer: Charles Lee
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 19 of 63

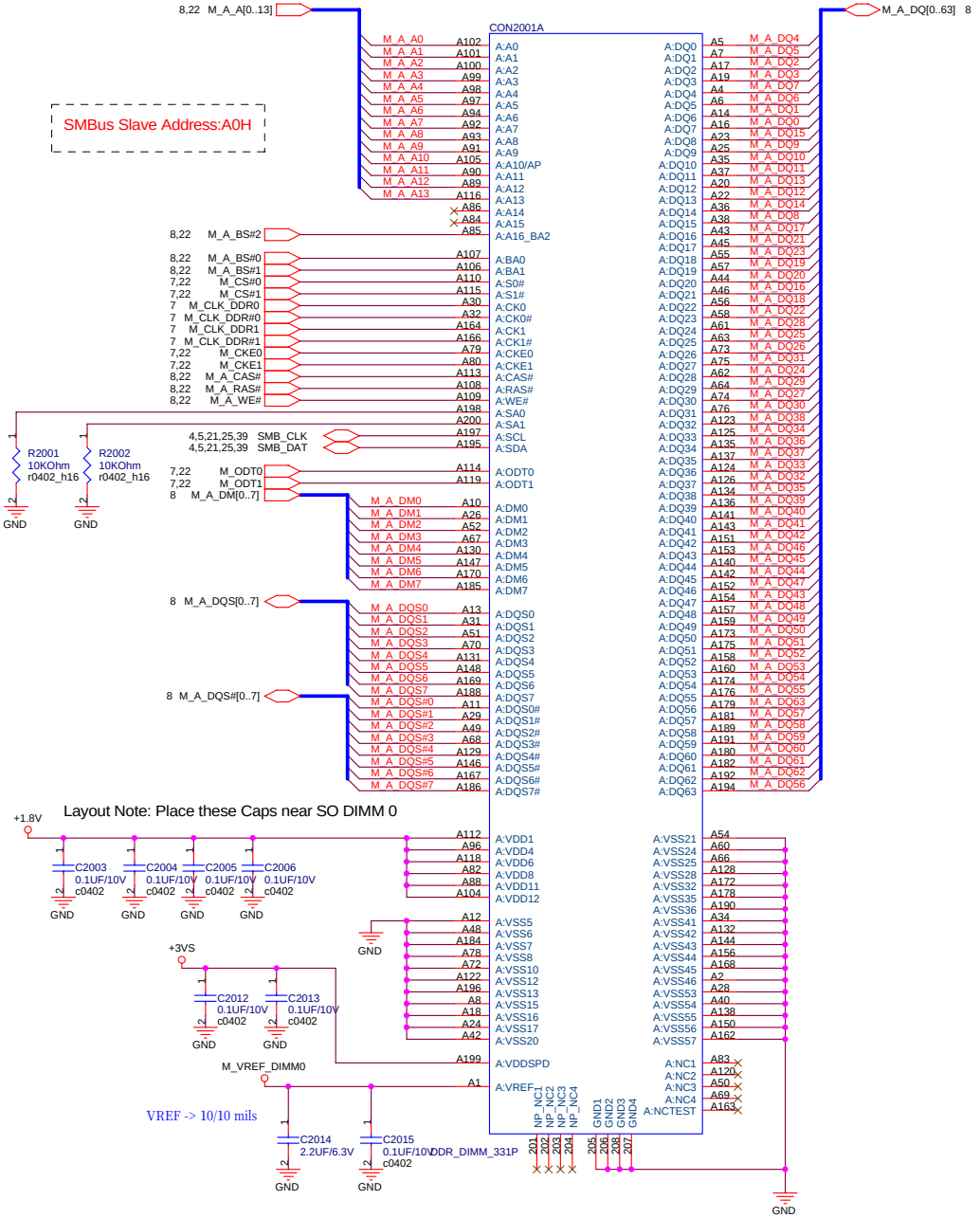




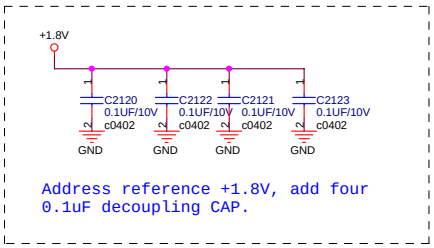




SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1



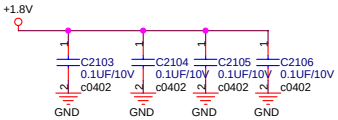
<Variant Name>
Title : DDR2 SO-DIMM_0
<OrgName>
Engineer: Charles Lee
Size: Custom
Project Name: A6Jc
Rev: 2.1
Date: Thursday, January 19, 2006
Sheet 20 of 63



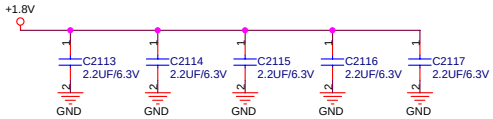


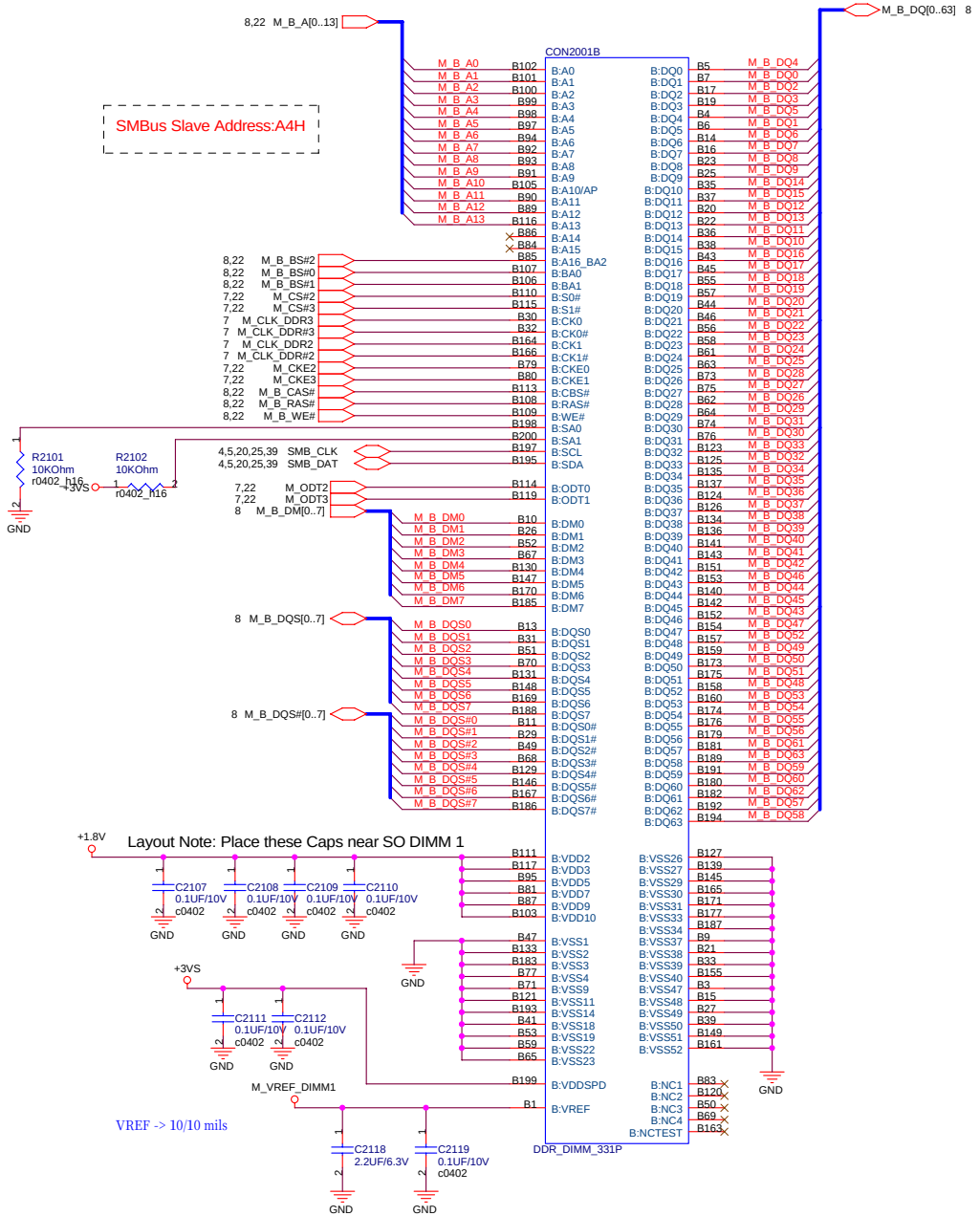


Layout Note: Place these High-Freq decoupling Caps near the GMCH

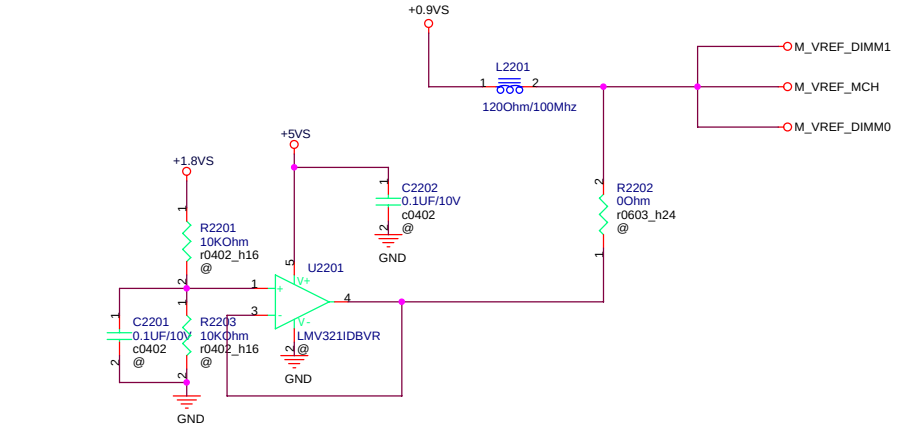


Layout Note: Place these CAPs near the GMCH





<Variant Name>
Title : DDR2 SO-DIMM_1
<OrgName>
Engineer: Charles Lee
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 21 of 63



M_A_A[0..13] 8,20

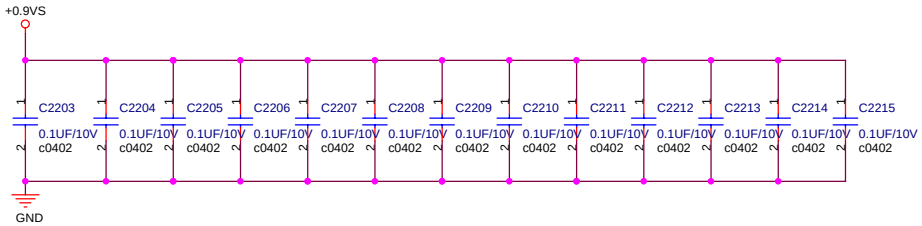
M_A_BS#[0..2] 8,20

M_A_CAS# 8,20
M_A_RAS# 8,20
M_A_WE# 8,20

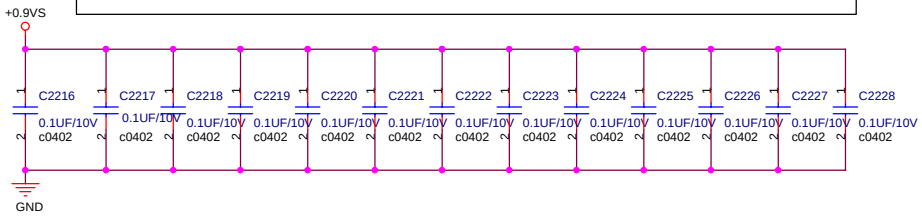
M_B_A[0..13] 8,21

M_B_BS#[0..2] 8,21

M_B_CAS# 8,21
M_B_RAS# 8,21
M_B_WE# 8,21



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



M_CS#[0..3] 7,20,21

M_ODT[0..3] 7,20,21

M_CKE[0..3] 7,20,21

HAD SWAPED

+0.9VS

1	56Ohm	16	RN2201A	M_B_RAS#
2	56Ohm	15	RN2201B	M_A_BS#1
3	56Ohm	14	RN2201C	
4	56Ohm	13	RN2201D	M_B_A13
5	56Ohm	12	RN2201E	M_ODT2
6	56Ohm	11	RN2201F	M_A_RAS#
7	56Ohm	10	RN2201G	M_A_A13
8	56Ohm	9	RN2201H	M_A_A11

1	56Ohm	16	RN2202A	M_A_BS#0
2	56Ohm	15	RN2202B	M_B_BS#2
3	56Ohm	14	RN2202C	M_B_A12
4	56Ohm	13	RN2202D	M_B_A9
5	56Ohm	12	RN2202E	M_B_A8
6	56Ohm	11	RN2202F	M_B_A5
7	56Ohm	10	RN2202G	M_B_A3
8	56Ohm	9	RN2202H	M_B_A1

1	56Ohm	16	RN2203A	M_ODT1
2	56Ohm	15	RN2203B	M_CS#1
3	56Ohm	14	RN2203C	M_A_CAS#
4	56Ohm	13	RN2203D	M_A_WE#
5	56Ohm	12	RN2203E	M_A_A10
6	56Ohm	11	RN2203F	M_A_A1
7	56Ohm	10	RN2203G	M_A_A5
8	56Ohm	9	RN2203H	M_A_A3

1	56Ohm	16	RN2204A	M_CKE1
2	56Ohm	15	RN2204B	M_B_A7
3	56Ohm	14	RN2204C	M_B_A11
4	56Ohm	13	RN2204D	M_B_A6
5	56Ohm	12	RN2204E	M_B_A2
6	56Ohm	11	RN2204F	M_B_A0
7	56Ohm	10	RN2204G	M_A_A0
8	56Ohm	9	RN2204H	M_B_BS#1

1	56Ohm	16	RN2205A	M_A_A8
2	56Ohm	15	RN2205B	M_A_A9
3	56Ohm	14	RN2205C	M_A_A12
4	56Ohm	13	RN2205D	M_B_A4
5	56Ohm	12	RN2205E	M_A_BS#2
6	56Ohm	11	RN2205F	M_CKE0
7	56Ohm	10	RN2205G	M_CKE3
8	56Ohm	9	RN2205H	M_CKE2

1	56Ohm	16	RN2206A	M_ODT3
2	56Ohm	15	RN2206B	M_CS#3
3	56Ohm	14	RN2206C	M_A_A7
4	56Ohm	13	RN2206D	M_A_A4
5	56Ohm	12	RN2206E	M_A_A6
6	56Ohm	11	RN2206F	M_A_A2
7	56Ohm	10	RN2206G	M_ODT0
8	56Ohm	9	RN2206H	M_CS#0

1	56Ohm	16	RN2207A	
2	56Ohm	15	RN2207B	
3	56Ohm	14	RN2207C	M_B_A10
4	56Ohm	13	RN2207D	M_B_BS#0
5	56Ohm	12	RN2207E	M_B_WE#
6	56Ohm	11	RN2207F	M_B_CAS#
7	56Ohm	10	RN2207G	
8	56Ohm	9	RN2207H	M_CS#2

<Variant Name>

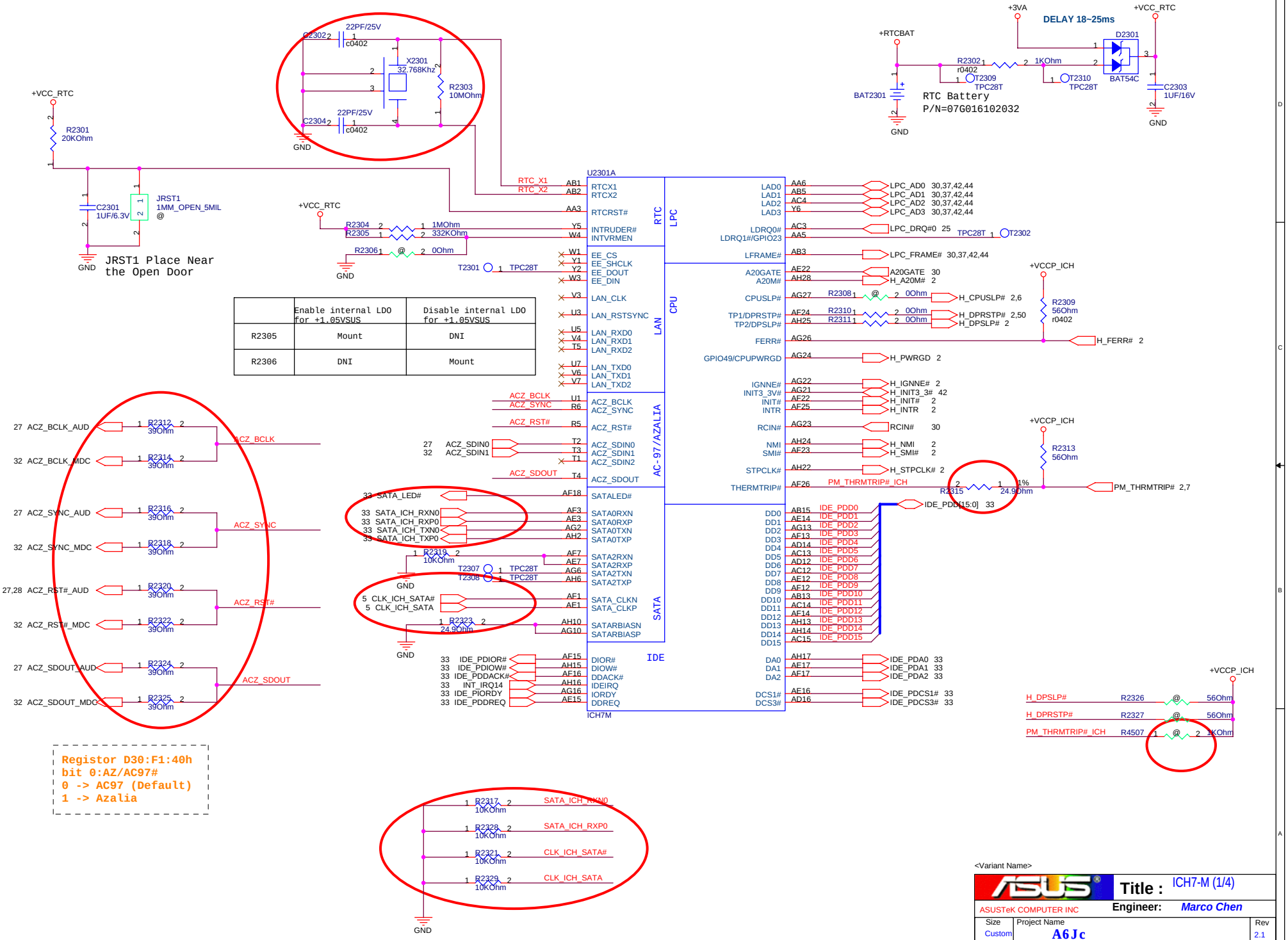
Title : DDR2 TERM

ASUSTeK COMPUTER INC

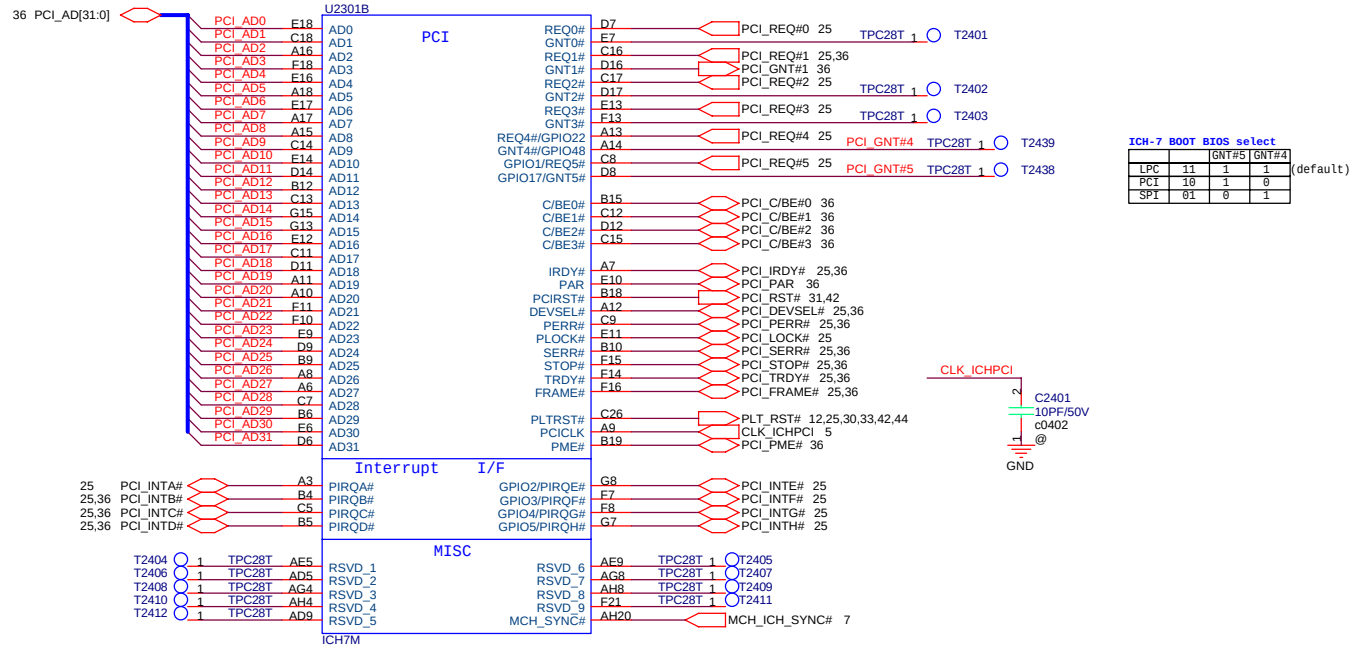
Engineer: Charles Lee

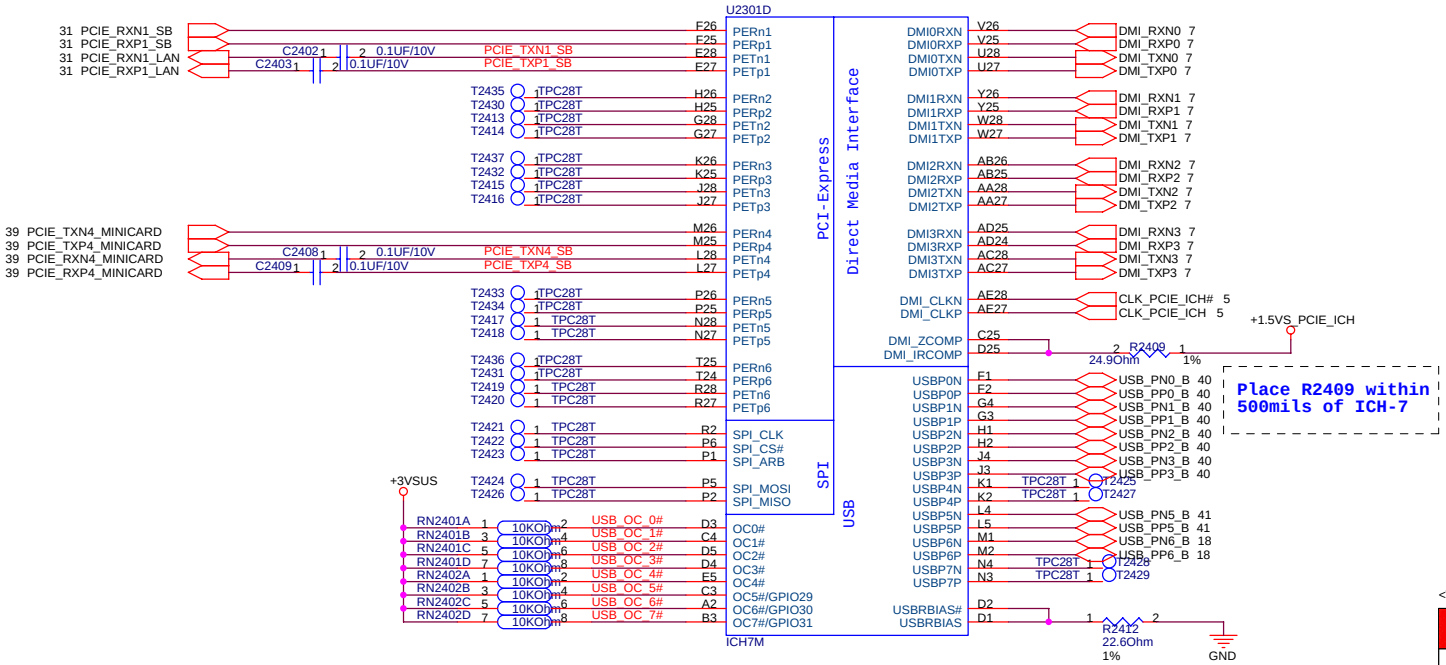
Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 22 of 63



	Enable internal LDO for +1.05VSUS	Disable internal LDO for +1.05VSUS
R2305	Mount	DNI
R2306	DNI	Mount





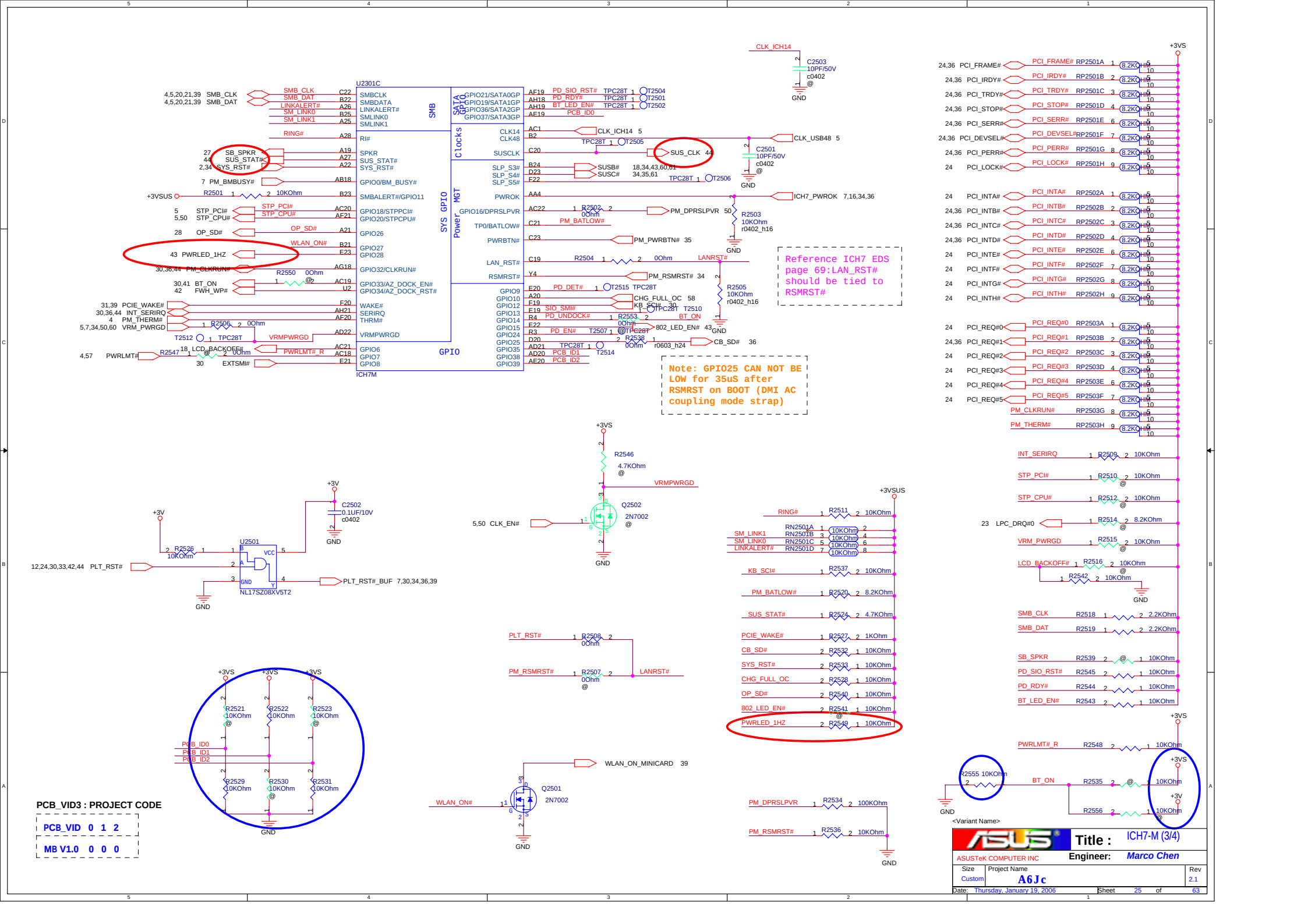
<Variant Name>

Title : ICH7-M (2/4)

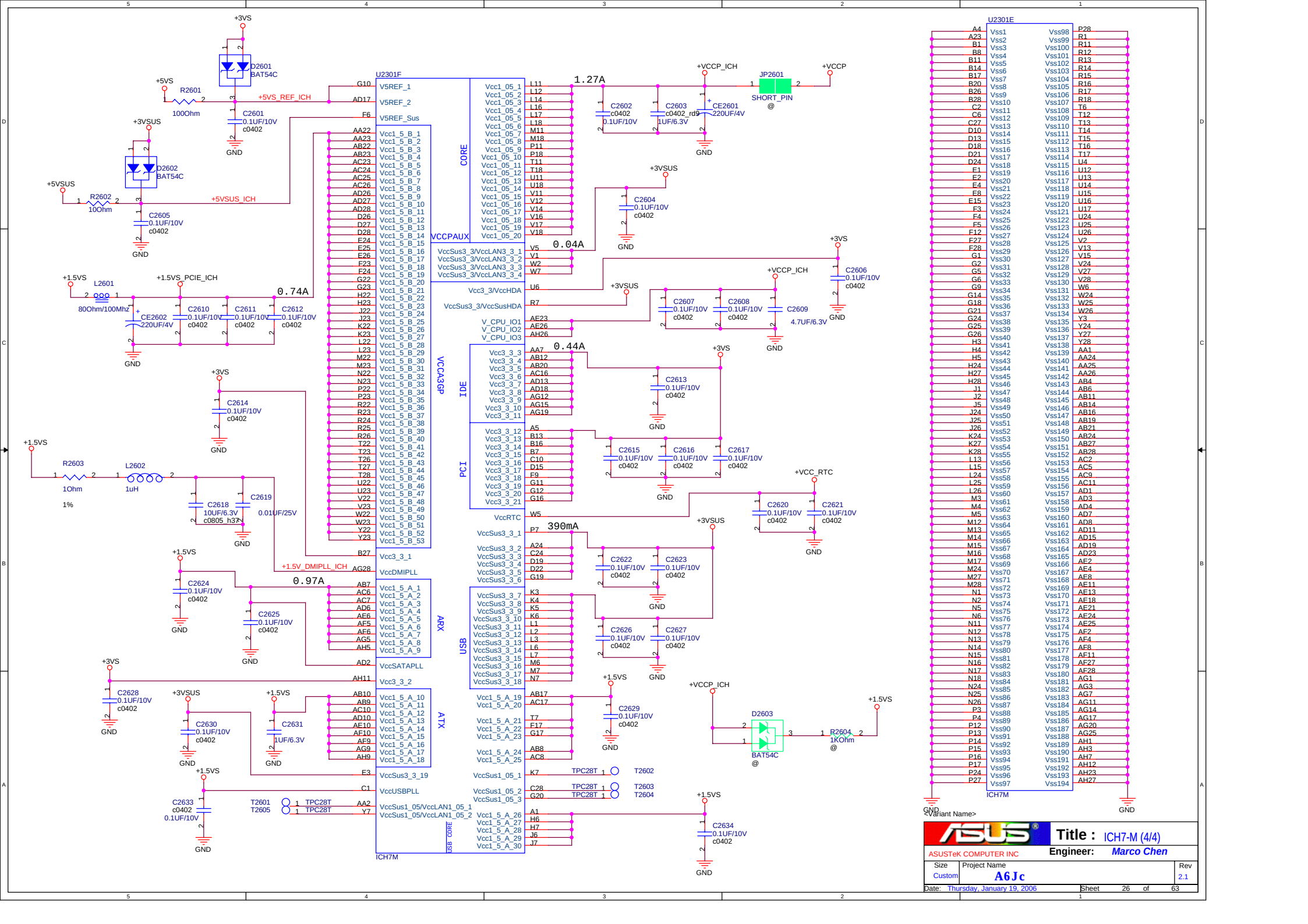
ASUSTeK COMPUTER INC Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 24 of 63



U2301C
ICH7M
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
SMBALERT#/GPIO11
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39
SMB_CLK
SMB_DAT
LINKALERT#
SM_LINK0
SM_LINK1
RING#
SB_SPKR
SUS_STAT#
SYS_RST#
PM_BMBUSY#
+3VSUS
R2501 10KOhm
STP_PCI#
STP_CPU#
OP_SD#
WLAN_ON#
PWRLED_1HZ
PM_CLKRUN#
R2550 0Ohm
BT_ON
FWH_WP#
PCIE_WAKE#
INT_SERIRQ
PM_THERM#
VRM_PWRGD
R2506 0Ohm
T2512 TPC28T
VRMPWRGD
LCD_BACKOFF#
PWRLMT#
R2547 0Ohm
PWRLMT#_R
EXTSMI#
PD_SIO_RST# TPC28T T2504
PD_RDY# TPC28T T2501
BT_LED_EN# TPC28T T2502
PCB_ID0
CLK_ICH14 5
TPC28T T2505
SUS_CLK 44
SUSB# 18,34,43,60,61
SUSC# 34,35,61
TPC28T T2506
ICH7_PWROK 7,16,34,36
R2502 0Ohm
PM_DPRSLPVR 50
R2503 10KOhm r0402_h16
PM_BATLOW#
PM_PWRBTN# 35
R2504 0Ohm
LANRST#
PM_RSMRST# 34
R2505 10KOhm r0402_h16
PD_DET# T2515 TPC28T
CHG_FULL_OC 58
KB_SCI# 30
SIO_SMI# TPC28T T2510
PD_UNDOCK# R2553 0Ohm
BT_ON
PD_EN# T2507 TPC28T
802_LED_EN# 43
R2538 0Ohm r0603_h24
CB_SD# 36
TPC28T T2514
PCB_ID1
PCB_ID2
CLK_ICH14
C2503 10PF/50V c0402
GND
CLK_USB48 5
C2501 10PF/50V c0402
Reference ICH7 EDS page 69:LAN_RST# should be tied to RSMRST#
Note: GPIO25 CAN NOT BE LOW for 35uS after RSMRST on BOOT (DMI AC coupling mode strap)
+3VS
24,36 PCI_FRAME# RP2501A
24,36 PCI_IRDY# RP2501B
24,36 PCI_TRDY# RP2501C
24,36 PCI_STOP# RP2501D
24,36 PCI_SERR# RP2501E
24,36 PCI_DEVSEL# RP2501F
24,36 PCI_PERR# RP2501G
24 PCI_LOCK# RP2501H
24 PCI_INTA# RP2502A
24,36 PCI_INTB# RP2502B
24,36 PCI_INTC# RP2502C
24,36 PCI_INTD# RP2502D
24 PCI_INTE# RP2502E
24 PCI_INTF# RP2502F
24 PCI_INTG# RP2502G
24 PCI_INTH# RP2502H
24 PCI_REQ#0 RP2503A
24,36 PCI_REQ#1 RP2503B
24 PCI_REQ#2 RP2503C
24 PCI_REQ#3 RP2503D
24 PCI_REQ#4 RP2503E
24 PCI_REQ#5 RP2503F
PM_CLKRUN# RP2503G
PM_THERM# RP2503H
8.2KOhm
INT_SERIRQ R2509 10KOhm
STP_PCI# R2510 10KOhm
STP_CPU# R2512 10KOhm
23 LPC_DRQ#0 R2514 8.2KOhm
VRM_PWRGD R2515 10KOhm
LCD_BACKOFF# R2516 10KOhm
R2542 10KOhm
SMB_CLK R2518 2.2KOhm
SMB_DAT R2519 2.2KOhm
SB_SPKR R2539 10KOhm
PD_SIO_RST# R2545 10KOhm
PD_RDY# R2544 10KOhm
BT_LED_EN# R2543 10KOhm
PWRLMT#_R R2548 10KOhm
R2555 10KOhm
BT_ON R2535 10KOhm
R2556 10KOhm
+3V
R2546 4.7KOhm
VRMPWRGD
Q2502 2N7002
5,50 CLK_EN#
C2502 0.1UF/10V c0402
U2501
NL17SZ08XV5T2
R2526 10KOhm
12,24,30,33,42,44 PLT_RST#
PLT_RST#_BUF 7,30,34,36,39
+3VSUS
RING# R2511 10KOhm
RN2501A
RN2501B
RN2501C
RN2501D
SM_LINK1
SM_LINK0
LINKALERT#
KB_SCI# R2537 10KOhm
PM_BATLOW# R2520 8.2KOhm
SUS_STAT# R2524 4.7KOhm
PCIE_WAKE# R2527 1KOhm
CB_SD# R2532 10KOhm
SYS_RST# R2533 10KOhm
CHG_FULL_OC R2528 10KOhm
OP_SD# R2540 10KOhm
802_LED_EN# R2541 10KOhm
PWRLED_1HZ R2549 10KOhm
PLT_RST# R2508 0Ohm
PM_RSMRST# R2507 0Ohm
LANRST#
R2521 10KOhm
R2522 10KOhm
R2523 10KOhm
R2529 10KOhm
R2530 10KOhm
R2531 10KOhm
PCB_ID0
PCB_ID1
PCB_ID2
WLAN_ON_MINICARD 39
Q2501 2N7002
WLAN_ON#
PM_DPRSLPVR R2534 100KOhm
PM_RSMRST# R2536 10KOhm
PCB_VID3 : PROJECT CODE
PCB_VID 0 1 2
MB V1.0 0 0 0
<Variant Name>
Title : ICH7-M (3/4)
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 25 of 63


U2301F
U2301E
ICH7M
CORE
VCCPAUX
VCCA3GP
IDE
PCI
ARX
USB
ATX
+3VS
+5VS
+5VSUS
+1.5VS
+VCCP
+VCCP_ICH
+VCC_RTC
+3VSUS
+1.5VS_PCIE_ICH
+5VS_REF_ICH
+5VSUS_ICH
+1.5V_DMIPLL_ICH
1.27A
0.04A
0.44A
390mA
0.74A
0.97A
R2601 100Ohm
R2602 10Ohm
R2603 1Ohm 1%
R2604 1KOhm @
L2601 80Ohm/100Mhz
L2602 1uH
JP2601 SHORT_PIN @
D2601 BAT54C
D2602 BAT54C
D2603 BAT54C @
C2601 0.1UF/10V c0402
C2602 c0402 0.1UF/10V
C2603 c0402_rd9 1UF/6.3V
CE2601 220UF/4V
C2604 0.1UF/10V c0402
C2605 0.1UF/10V c0402
C2606 0.1UF/10V c0402
C2607 0.1UF/10V c0402
C2608 0.1UF/10V c0402
C2609 4.7UF/6.3V
CE2602 220UF/4V
C2610 0.1UF/10V c0402
C2611 0.1UF/10V c0402
C2612 0.1UF/10V c0402
C2613 0.1UF/10V c0402
C2614 0.1UF/10V c0402
C2615 0.1UF/10V c0402
C2616 0.1UF/10V c0402
C2617 0.1UF/10V c0402
C2618 10UF/6.3V c0805_h32
C2619 0.01UF/25V
C2620 0.1UF/10V c0402
C2621 0.1UF/10V c0402
C2622 0.1UF/10V c0402
C2623 0.1UF/10V c0402
C2624 0.1UF/10V c0402
C2625 0.1UF/10V c0402
C2626 0.1UF/10V c0402
C2627 0.1UF/10V c0402
C2628 0.1UF/10V c0402
C2629 0.1UF/10V c0402
C2630 0.1UF/10V c0402
C2631 1UF/6.3V
C2633 0.1UF/10V c0402
C2634 0.1UF/10V c0402
T2601 TPC28T
T2602 TPC28T
T2603 TPC28T
T2604 TPC28T
T2605 TPC28T
GND
<Variant Name>
Title : ICH7-M (4/4)
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
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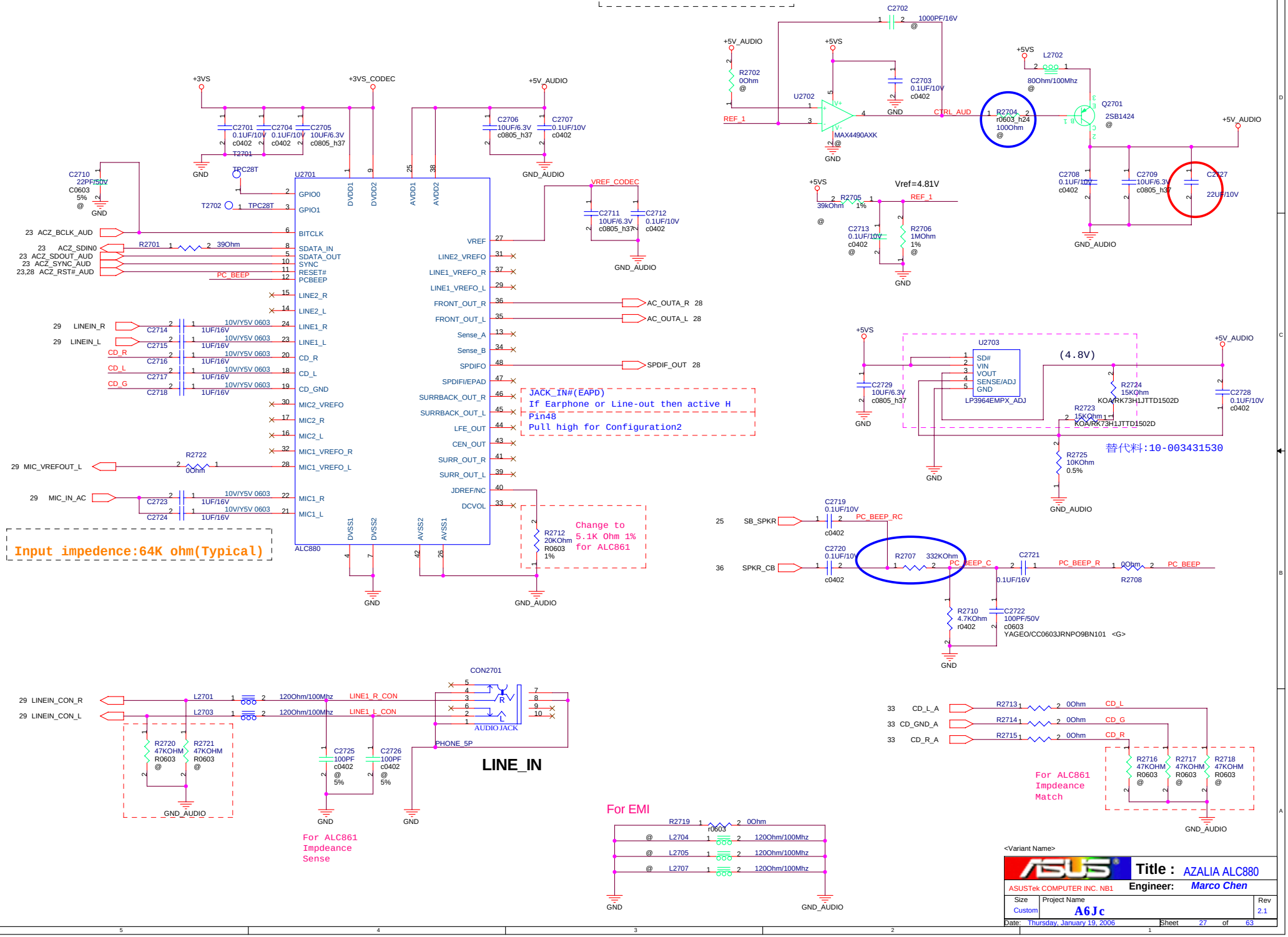
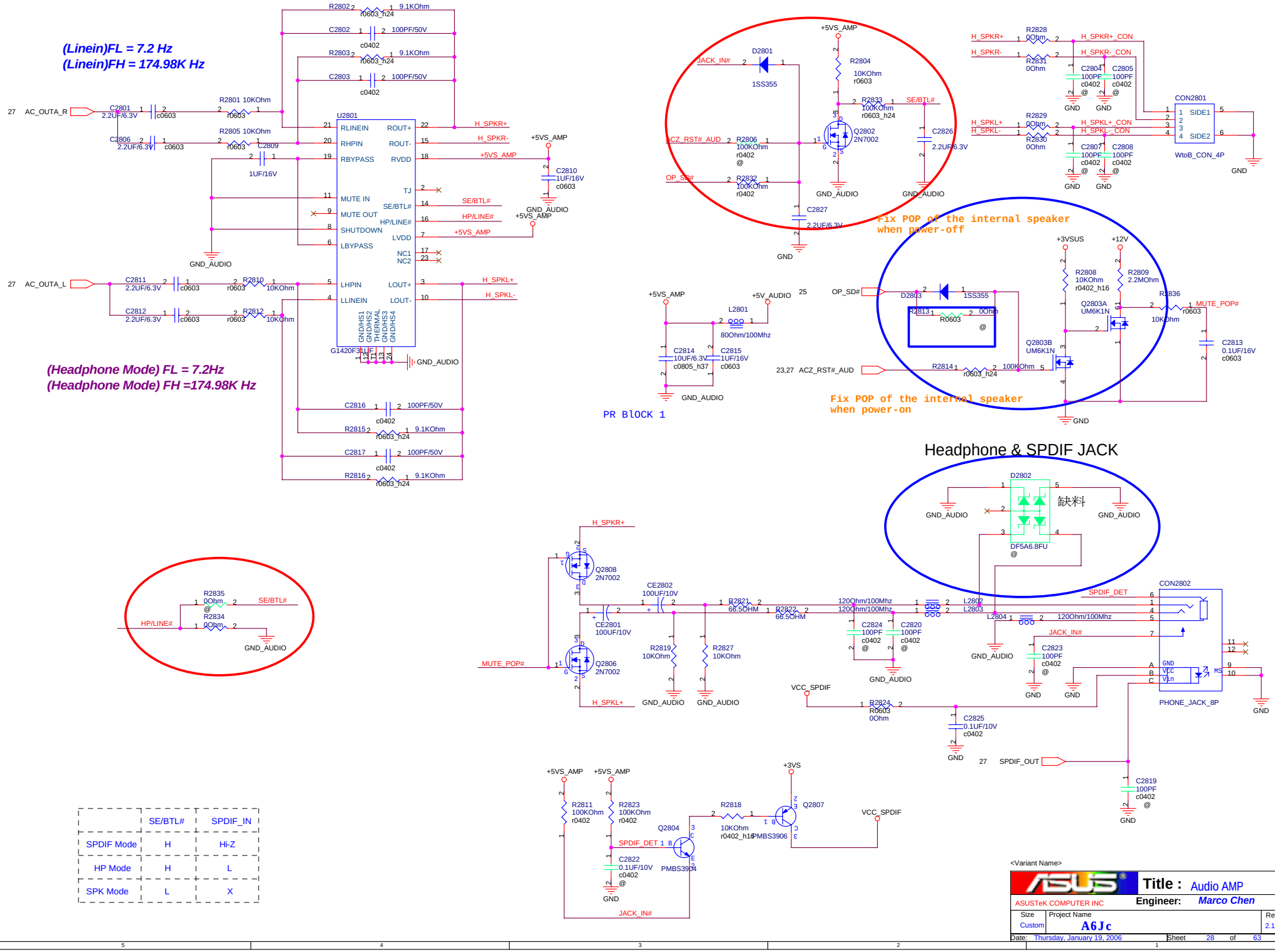
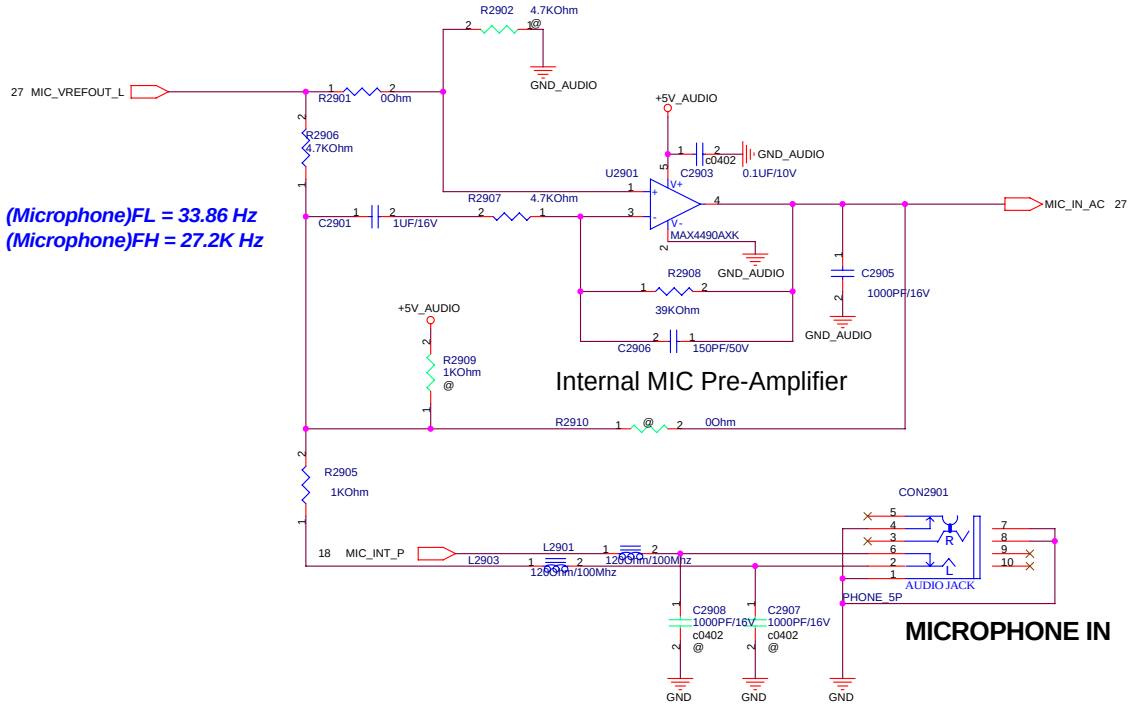
Place U2802near U2801

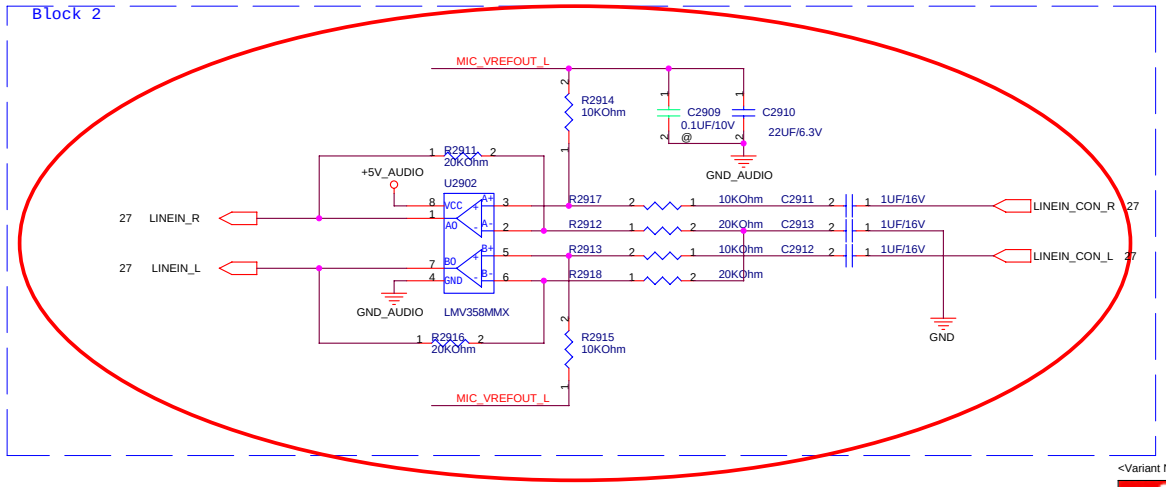


<Variant Name>

ASUSTek COMPUTER INC. NB1	Title : AZALIA ALC880	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 27 of 63	

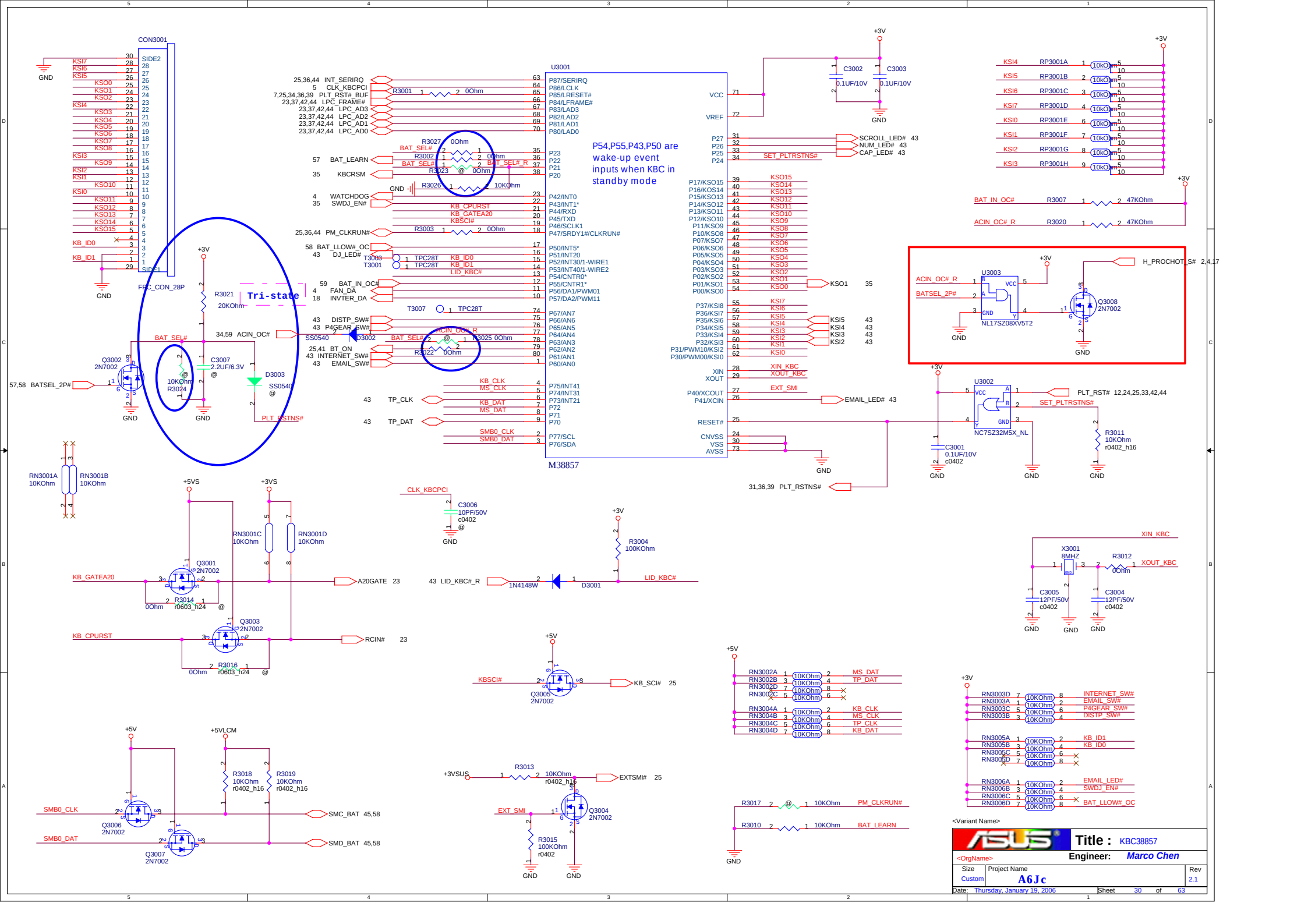

(Linein)FL = 7.2 Hz
(Linein)FH = 174.98K Hz
(Headphone Mode) FL = 7.2Hz
(Headphone Mode) FH =174.98K Hz
U2801
G1420F31UF
AC_OUTA_R
AC_OUTA_L
RLINEIN
RHPIN
RBYPASS
MUTE IN
MUTE OUT
SHUTDOWN
LBYPASS
LHPIN
LLINEIN
ROUT+
ROUT-
RVDD
TJ
SE/BTL#
HP/LINE#
LVDD
NC1
NC2
LOUT+
LOUT-
GND/HS1
GND/HS2
THERMAL
GND/HS3
GND/HS4
H_SPKR+
H_SPKR-
H_SPKL+
H_SPKL-
+5VS_AMP
GND_AUDIO
JACK_IN#
D2801
1SS355
ACZ_RST#_AUD
OP_SD#
Q2802
2N7002
Fix POP of the internal speaker when power-off
Fix POP of the internal speaker when power-on
+5V_AUDIO
+3VSUS
+12V
MUTE_POP#
23,27 ACZ_RST#_AUD
PR BlOCK 1
Headphone & SPDIF JACK
缺料
DF5A6.8FU
CON2801
WtoB_CON_4P
CON2802
PHONE_JACK_8P
SPDIF_DET
SPDIF_OUT
VCC_SPDIF
Q2808
Q2806
Q2807
Q2804
PMBS3904
HP/LINE#
SE/BTL#
SPDIF_IN
SPDIF Mode
HP Mode
SPK Mode
Title : Audio AMP
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 28 of 63

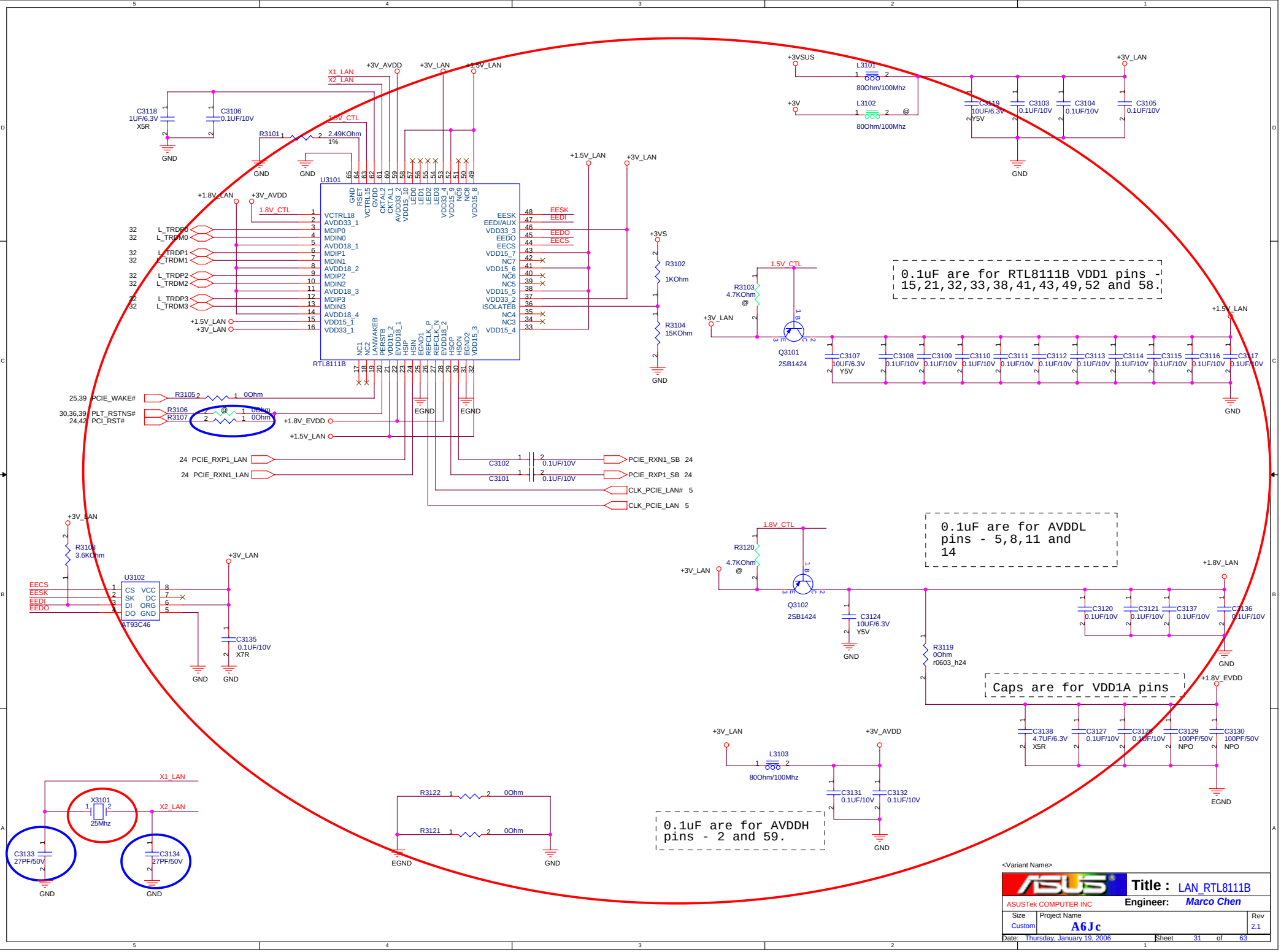




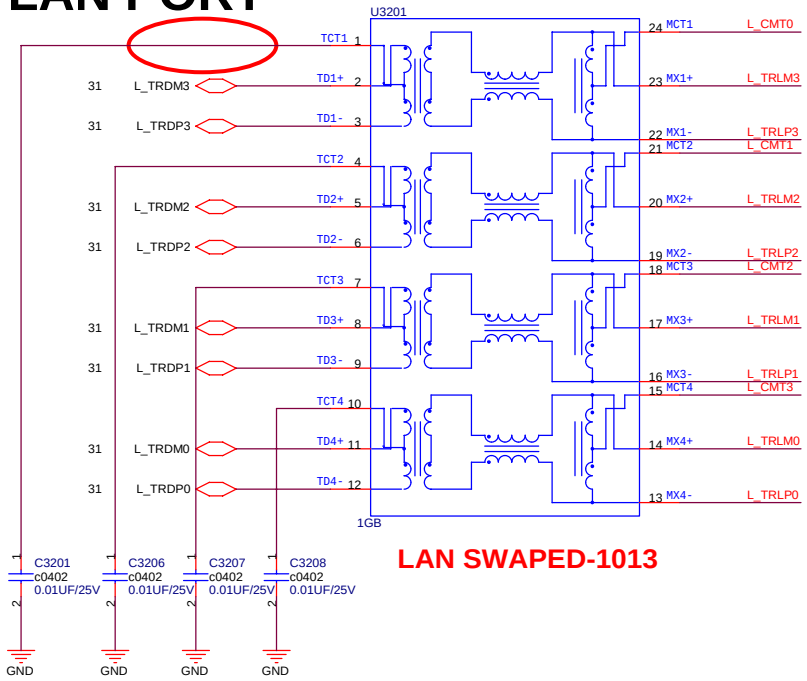
<Variant Name>

ASUSTeK COMPUTER INC	Title : MICROPHONE	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 29 of 63	

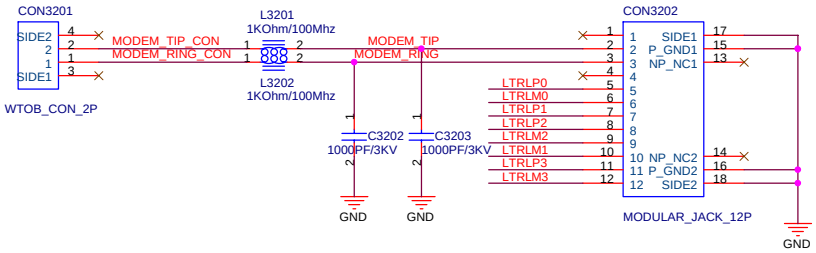

CON3001
FRC_CON_28P
U3001
M38857
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
Tri-state
R3021 20KOhm
BAT_SEL#
ACIN_OC#
Q3002 2N7002
C3007 2.2UF/6.3V
D3003 SS0540
PLT_RSTNS#
SS0540
D3002
R3025 0Ohm
R3022 0Ohm
R3027 0Ohm
R3002 0Ohm
R3023 @ 0Ohm
R3026 10KOhm
R3001 0Ohm
R3003 0Ohm
T3003 TPC28T
T3001 TPC28T
T3007 TPC28T
KB_ID0
KB_ID1
LID_KBC#
BAT_SEL#_R
ACIN_OC#_R
BAT_LLOW#_OC
DJ_LED#
FAN_DA
INVTER_DA
DISTP_SW#
P4GEAR_SW#
INTERNET_SW#
EMAIL_SW#
BT_ON
INT_SERIRQ
CLK_KBCPCI
PLT_RST#_BUF
LPC_FRAME#
LPC_AD3
LPC_AD2
LPC_AD1
LPC_AD0
BAT_LEARN
KBCRSM
WATCHDOG
SWDJ_EN#
KB_CPURST
KB_GATEA20
KBSCI#
PM_CLKRUN#
TP_CLK
TP_DAT
KB_CLK
MS_CLK
KB_DAT
MS_DAT
SMB0_CLK
SMB0_DAT
KSO0
KSO1
KSO2
KSO3
KSO4
KSO5
KSO6
KSO7
KSO8
KSO9
KSO10
KSO11
KSO12
KSO13
KSO14
KSO15
KSI0
KSI1
KSI2
KSI3
KSI4
KSI5
KSI6
KSI7
SCROLL_LED# 43
NUM_LED# 43
CAP_LED# 43
SET_PLTRSTNS#
EMAIL_LED# 43
EXT_SMI
XIN_KBC
XOUT_KBC
RESET#
CNVSS
VCC
VREF
VSS
AVSS
C3002 0.1UF/10V
C3003 0.1UF/10V
C3001 0.1UF/10V c0402
RP3001A
RP3001B
RP3001C
RP3001D
RP3001E
RP3001F
RP3001G
RP3001H
10KOhm
BAT_IN_OC#
ACIN_OC#_R
R3007 47KOhm
R3020 47KOhm
H_PROCHOT_S# 2,4,17
U3003 NL17SZ08XV5T2
Q3008 2N7002
U3002 NC7SZ32M5X_NL
PLT_RST# 12,24,25,33,42,44
SET_PLTRSTNS#
R3011 10KOhm r0402_h16
31,36,39 PLT_RSTNS#
RN3001A 10KOhm
RN3001B 10KOhm
RN3001C 10KOhm
RN3001D 10KOhm
Q3001 2N7002
Q3003 2N7002
R3014 0Ohm r0603_h24
R3016 0Ohm r0603_h24
A20GATE 23
RCIN# 23
C3006 10PF/50V c0402
R3004 100KOhm
1N4148W
D3001
43 LID_KBC#_R
LID_KBC#
X3001 8MHZ
R3012 0Ohm
C3005 12PF/50V c0402
C3004 12PF/50V c0402
Q3005 2N7002
KB_SCI# 25
RN3002A
RN3002B
RN3002D
RN3002C
RN3004A
RN3004B
RN3004C
RN3004D
MS_DAT
TP_DAT
KB_CLK
MS_CLK
TP_CLK
KB_DAT
RN3003D
RN3003A
RN3003C
RN3003B
INTERNET_SW#
EMAIL_SW#
P4GEAR_SW#
DISTP_SW#
RN3005A
RN3005B
RN3005C
RN3005D
KB_ID1
KB_ID0
RN3006A
RN3006B
RN3006C
RN3006D
EMAIL_LED#
SWDJ_EN#
BAT_LLOW#_OC
R3018 10KOhm r0402_h16
R3019 10KOhm r0402_h16
Q3006 2N7002
Q3007 2N7002
SMC_BAT 45,58
SMD_BAT 45,58
R3013 10KOhm r0402_h16
EXTSMI# 25
Q3004 2N7002
R3015 100KOhm r0402
R3017 10KOhm PM_CLKRUN#
R3010 10KOhm BAT_LEARN
<Variant Name>
Title : KBC38857
<OrgName>
Engineer: Marco Chen
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 30 of 63

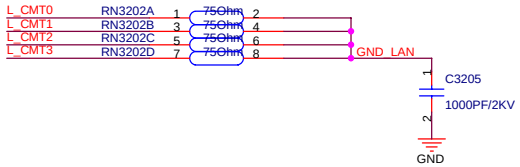

U3101
RTL8111B
VCTRL18
AVDD33_1
MDIP0
MDIN0
AVDD18_1
MDIP1
MDIN1
AVDD18_2
MDIP2
MDIN2
AVDD18_3
MDIP3
MDIN3
AVDD18_4
VDD15_1
VDD33_1
EESK
EEDI/AUX
VDD33_3
EEDO
EECS
VDD15_7
NC7
VDD15_6
NC6
NC5
VDD15_5
VDD33_2
ISOLATEB
NC4
NC3
VDD15_4
L_TRDP0
L_TRDM0
L_TRDP1
L_TRDM1
L_TRDP2
L_TRDM2
L_TRDP3
L_TRDM3
1.8V_CTL
1.5V_CTL
+1.8V_LAN
+3V_AVDD
+3V_LAN
+1.5V_LAN
+3VS
+3VSUS
+3V
R3102 1KOhm
R3104 15KOhm
R3101 2.49KOhm 1%
R3103 4.7KOhm @
R3105 0Ohm
R3106 @ 0Ohm
R3107 0Ohm
R3108 3.6KOhm
R3120 4.7KOhm @
R3119 0Ohm r0603_h24
R3122 0Ohm
R3121 0Ohm
L3101 80Ohm/100Mhz
L3102 @ 80Ohm/100Mhz
L3103 80Ohm/100Mhz
Q3101 2SB1424
Q3102 2SB1424
U3102 AT93C46
X3101 25Mhz
C3118 1UF/6.3V X5R
C3106 0.1UF/10V
C3119 10UF/6.3V Y5V
C3103 0.1UF/10V
C3104 0.1UF/10V
C3105 0.1UF/10V
C3107 10UF/6.3V Y5V
C3108 0.1UF/10V
C3109 0.1UF/10V
C3110 0.1UF/10V
C3111 0.1UF/10V
C3112 0.1UF/10V
C3113 0.1UF/10V
C3114 0.1UF/10V
C3115 0.1UF/10V
C3116 0.1UF/10V
C3117 0.1UF/10V
C3102 0.1UF/10V
C3101 0.1UF/10V
C3124 10UF/6.3V Y5V
C3120 0.1UF/10V
C3121 0.1UF/10V
C3137 0.1UF/10V
C3136 0.1UF/10V
C3135 0.1UF/10V X7R
C3138 4.7UF/6.3V X5R
C3127 0.1UF/10V
C3128 0.1UF/10V
C3129 100PF/50V NPO
C3130 100PF/50V NPO
C3131 0.1UF/10V
C3132 0.1UF/10V
C3133 27PF/50V
C3134 27PF/50V
0.1uF are for RTL8111B VDD1 pins - 15,21,32,33,38,41,43,49,52 and 58.
0.1uF are for AVDDL pins - 5,8,11 and 14
Caps are for VDD1A pins
0.1uF are for AVDDH pins - 2 and 59.
25,39 PCIE_WAKE#
30,36,39 PLT_RSTNS#
24,42 PCI_RST#
24 PCIE_RXP1_LAN
24 PCIE_RXN1_LAN
PCIE_RXN1_SB 24
PCIE_RXP1_SB 24
CLK_PCIE_LAN# 5
CLK_PCIE_LAN 5
EECS
EESK
EEDI
EEDO
GND
EGND
X1_LAN
X2_LAN
<Variant Name>
Title : LAN_RTL8111B
ASUSTek COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 31 of 63

LAN PORT

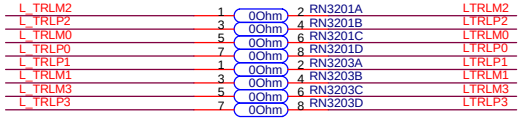


LAN SWAPED-1013

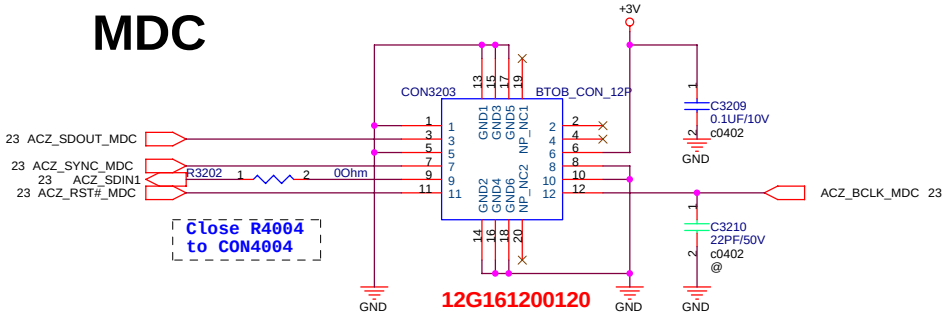


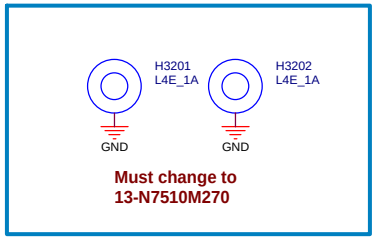


FOR EMI



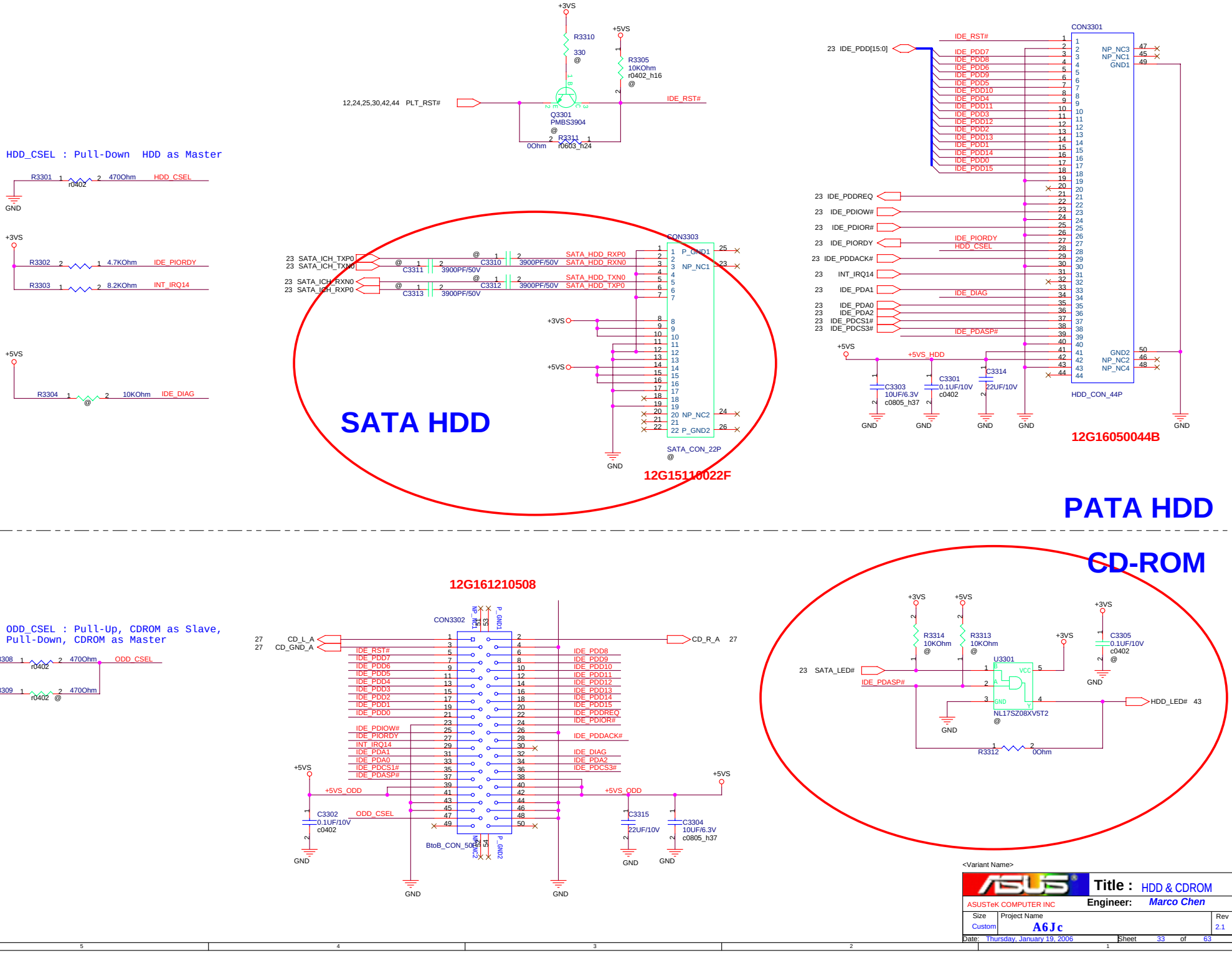
MDC

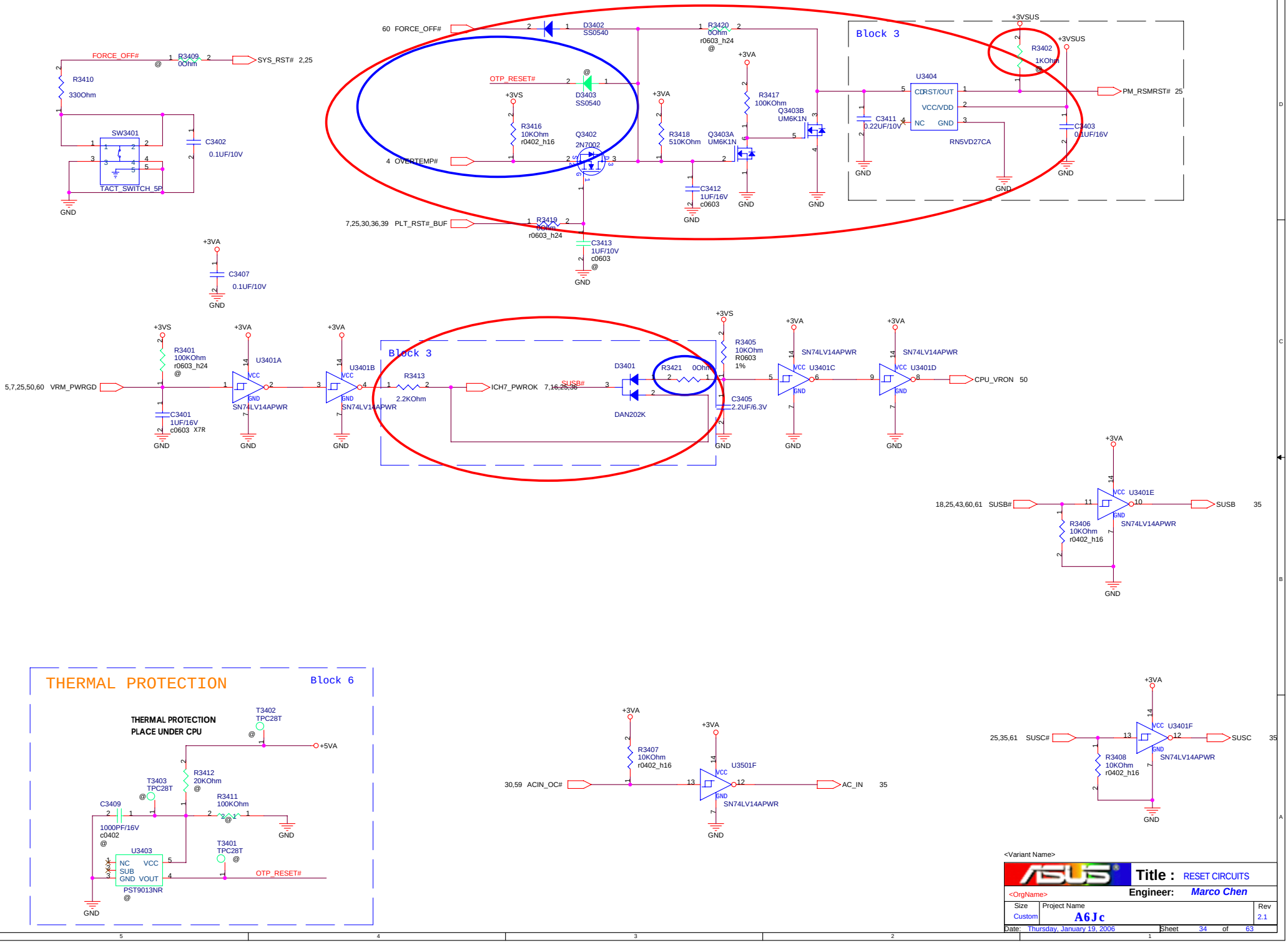




<Variant Name>

ASUSTeK COMPUTER INC	Title : RJ11+45,MDC	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 32 of 63	


HDD_CSEL : Pull-Down HDD as Master
R3301 470Ohm HDD_CSEL
R3302 4.7KOhm IDE_PIORDY
R3303 8.2KOhm INT_IRQ14
R3304 10KOhm IDE_DIAG
+3VS
+5VS
GND
R3310 330
R3305 10KOhm r0402_h16
12,24,25,30,42,44 PLT_RST#
IDE_RST#
Q3301 PMBS3904
R3311 0Ohm r0603_h24
SATA HDD
CON3303
SATA_CON_22P
12G15110022F
CON3301
HDD_CON_44P
12G16050044B
PATA HDD
CD-ROM
ODD_CSEL : Pull-Up, CDROM as Slave, Pull-Down, CDROM as Master
R3308 470Ohm ODD_CSEL
R3309 470Ohm
12G161210508
CON3302
BtoB_CON_50P
C3302 0.1UF/10V
C3315 22UF/10V
C3304 10UF/6.3V
R3314 10KOhm
R3313 10KOhm
U3301
NL17SZ08XV5T2
C3305 0.1UF/10V
R3312 0Ohm
SATA_LED#
HDD_LED# 43
<Variant Name>
Title : HDD & CDROM
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 33 of 63



<Variant Name>

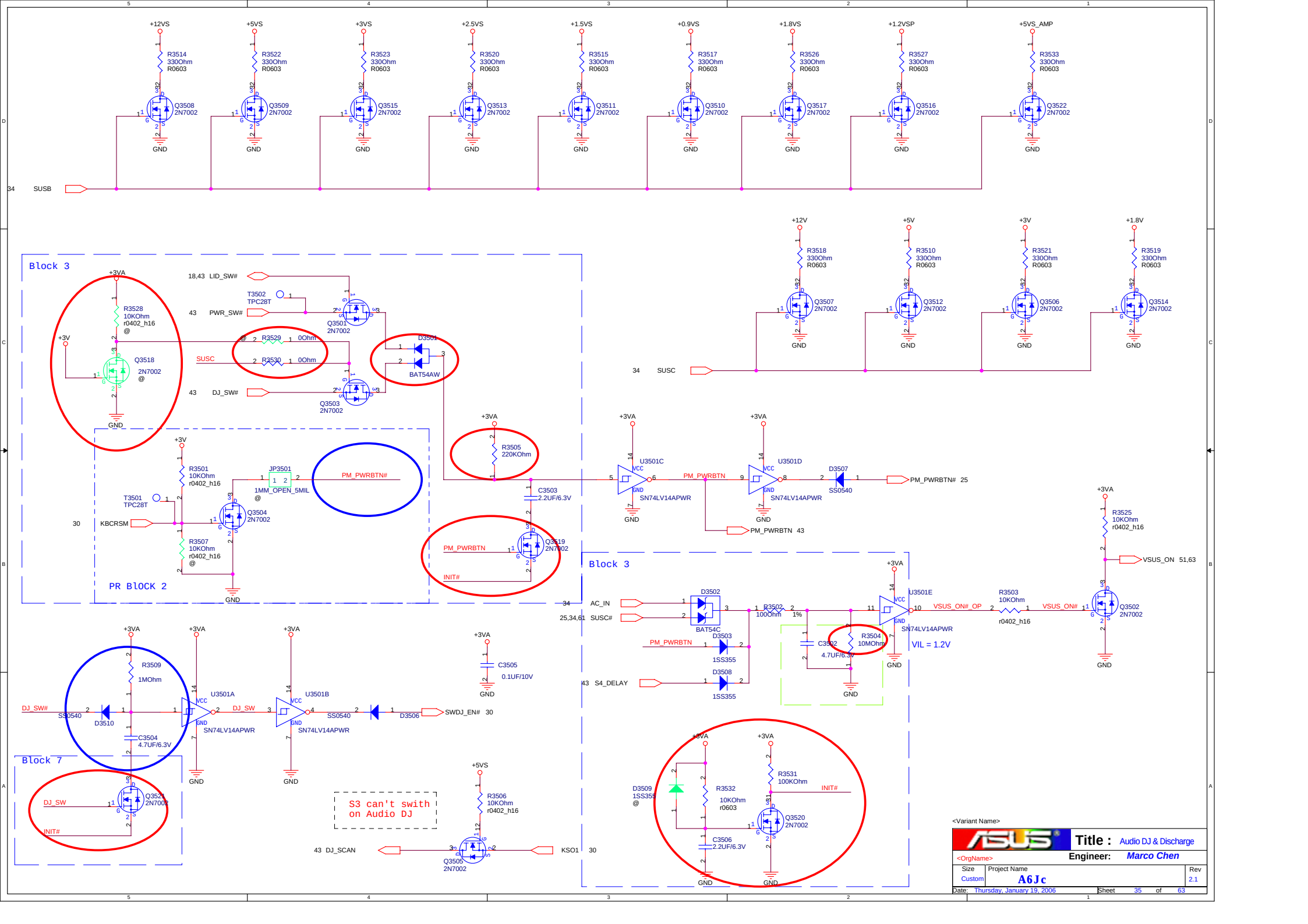
Title : RESET CIRCUITS

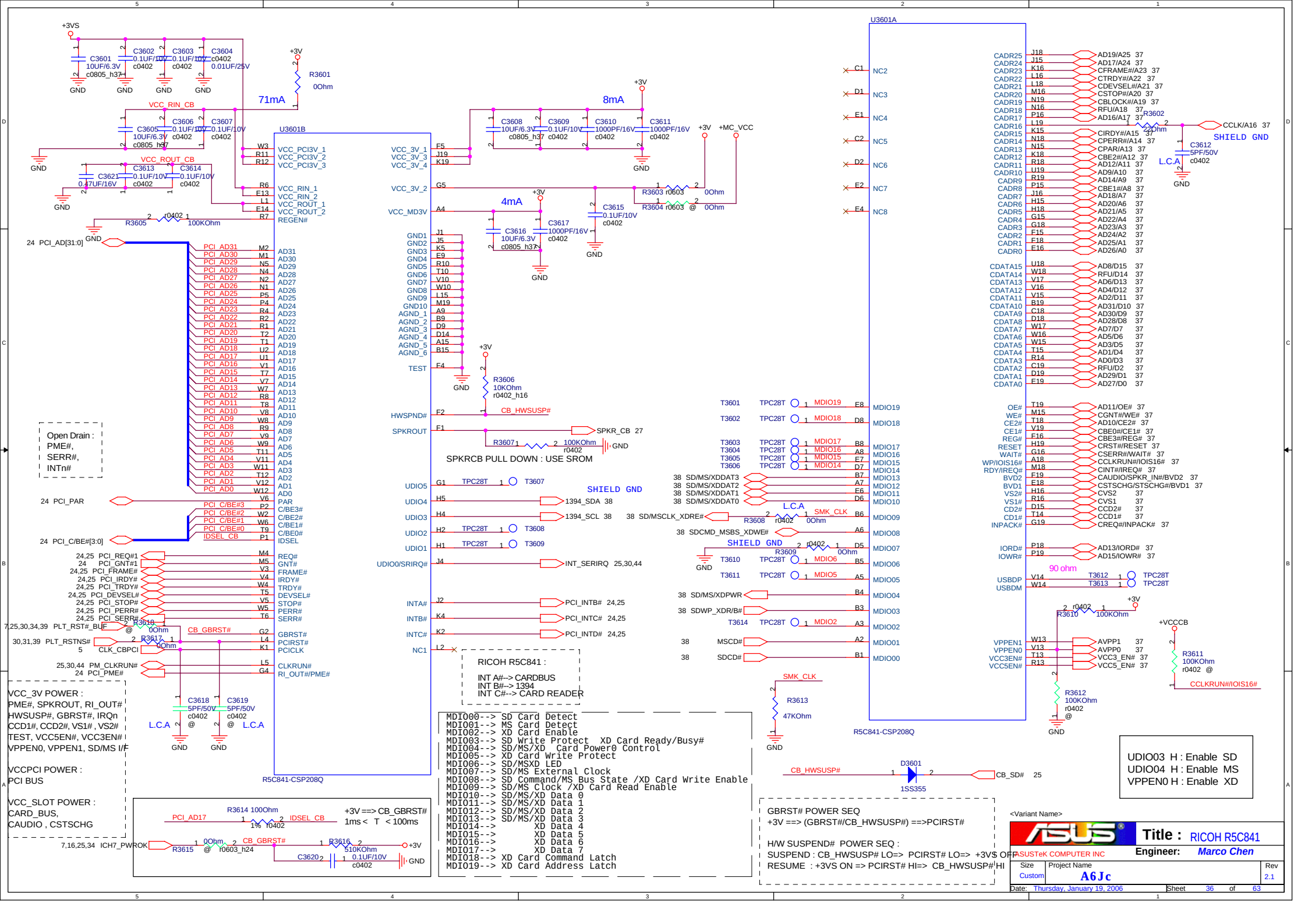
<OrgName>

Engineer: *Marco Chen*

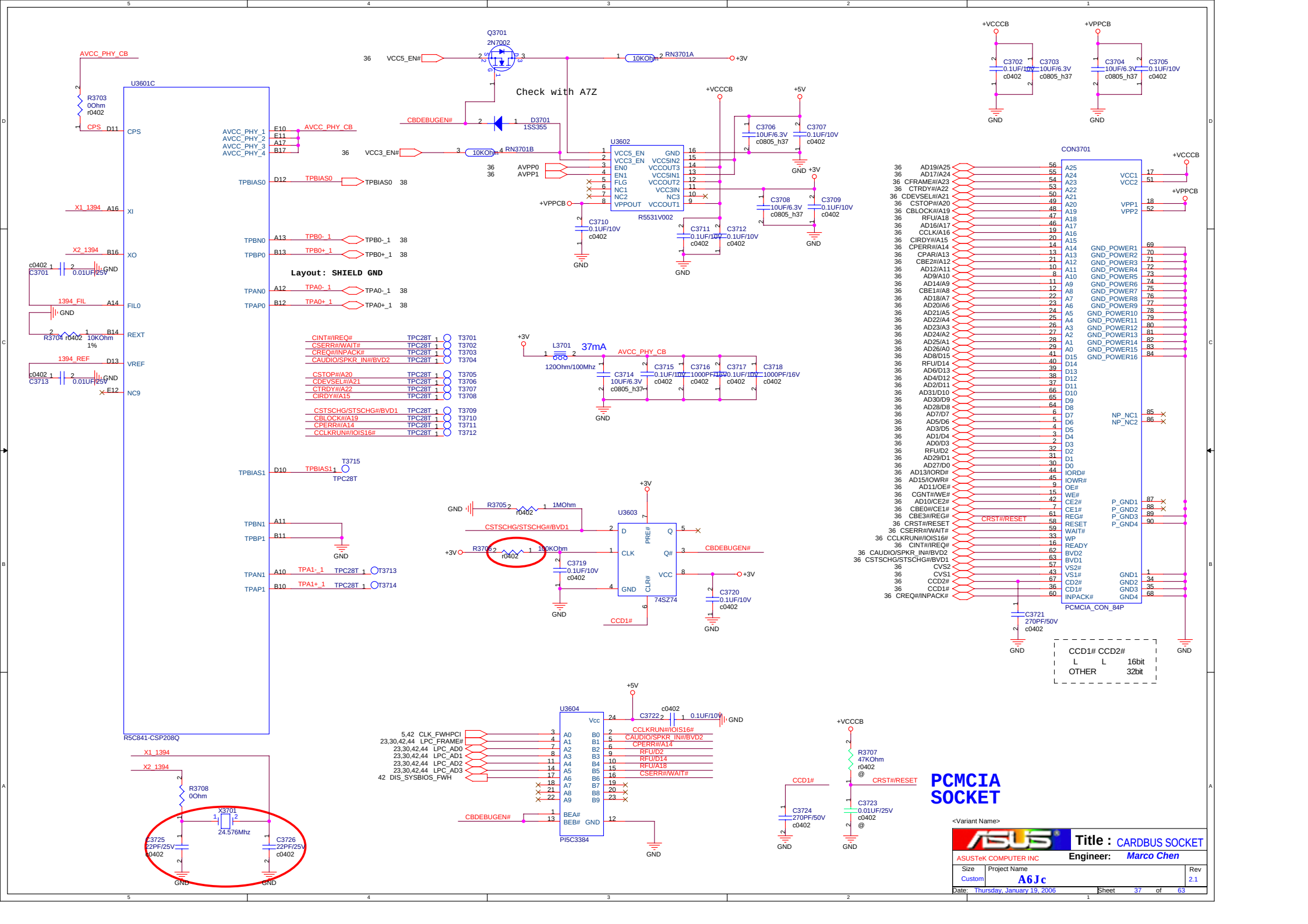
Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 34 of 63


+12VS
+5VS
+3VS
+2.5VS
+1.5VS
+0.9VS
+1.8VS
+1.2VSP
+5VS_AMP
R3514 330Ohm R0603
R3522 330Ohm R0603
R3523 330Ohm R0603
R3520 330Ohm R0603
R3515 330Ohm R0603
R3517 330Ohm R0603
R3526 330Ohm R0603
R3527 330Ohm R0603
R3533 330Ohm R0603
Q3508 2N7002
Q3509 2N7002
Q3515 2N7002
Q3513 2N7002
Q3511 2N7002
Q3510 2N7002
Q3517 2N7002
Q3516 2N7002
Q3522 2N7002
GND
34 SUSB
+12V
+5V
+3V
+1.8V
R3518 330Ohm R0603
R3510 330Ohm R0603
R3521 330Ohm R0603
R3519 330Ohm R0603
Q3507 2N7002
Q3512 2N7002
Q3506 2N7002
Q3514 2N7002
34 SUSC
Block 3
+3VA
18,43 LID_SW#
T3502 TPC28T
43 PWR_SW#
R3528 10KOhm r0402_h16 @
+3V
Q3518 2N7002 @
SUSC
R3529 0Ohm
R3530 0Ohm
43 DJ_SW#
Q3501 2N7002
Q3503 2N7002
D3501
BAT54AW
R3505 220KOhm
C3503 2.2UF/6.3V
PR BLOCK 2
R3501 10KOhm r0402_h16
JP3501 1MM_OPEN_5MIL @
PM_PWRBTN#
T3501 TPC28T
30 KBCRSM
Q3504 2N7002
R3507 10KOhm r0402_h16 @
Q3519 2N7002
INIT#
U3501C
U3501D
SN74LV14APWR
PM_PWRBTN
D3507 SS0540
PM_PWRBTN# 25
PM_PWRBTN 43
Block 3
AC_IN
25,34,61 SUSC#
D3502 BAT54C
D3503 1SS355
43 S4_DELAY
D3508 1SS355
R3502 100Ohm 1%
U3501E
VSUS_ON#_OP
R3504 10MOhm
C3502 4.7UF/6.3V
VIL = 1.2V
R3503 10KOhm r0402_h16
VSUS_ON#
R3525 10KOhm r0402_h16
VSUS_ON 51,63
Q3502 2N7002
R3509 1MOhm
U3501A
U3501B
DJ_SW#
SS0540
D3510
DJ_SW
C3504 4.7UF/6.3V
D3506
SWDJ_EN# 30
C3505 0.1UF/10V
Block 7
Q3521 2N7002
INIT#
S3 can't swith on Audio DJ
+5VS
R3506 10KOhm r0402_h16
43 DJ_SCAN
Q3505 2N7002
KSO1 30
D3509 1SS355 @
R3532 10KOhm r0603
R3531 100KOhm
C3506 2.2UF/6.3V
Q3520 2N7002
<Variant Name>
Title : Audio DJ & Discharge
<OrgName>
Engineer: Marco Chen
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 35 of 63



U3601B
U3601A
R5C841-CSP208Q
71mA
8mA
4mA
VCC_RIN_CB
VCC_ROUT_CB
SHIELD GND
L.C.A
90 ohm
SPKRCB PULL DOWN : USE SROM
Open Drain :
PME#,
SERR#,
INTn#
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1#, VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
+3V ==> CB_GBRST#
1ms < T < 100ms
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
<Variant Name>
ASUSTeK COMPUTER INC
Title : RICOH R5C841
Engineer: Marco Chen
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 36 of 63


PCMCIA SOCKET
Title : CARDBUS SOCKET
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size: Custom
Project Name: A6Jc
Rev: 2.1
Date: Thursday, January 19, 2006
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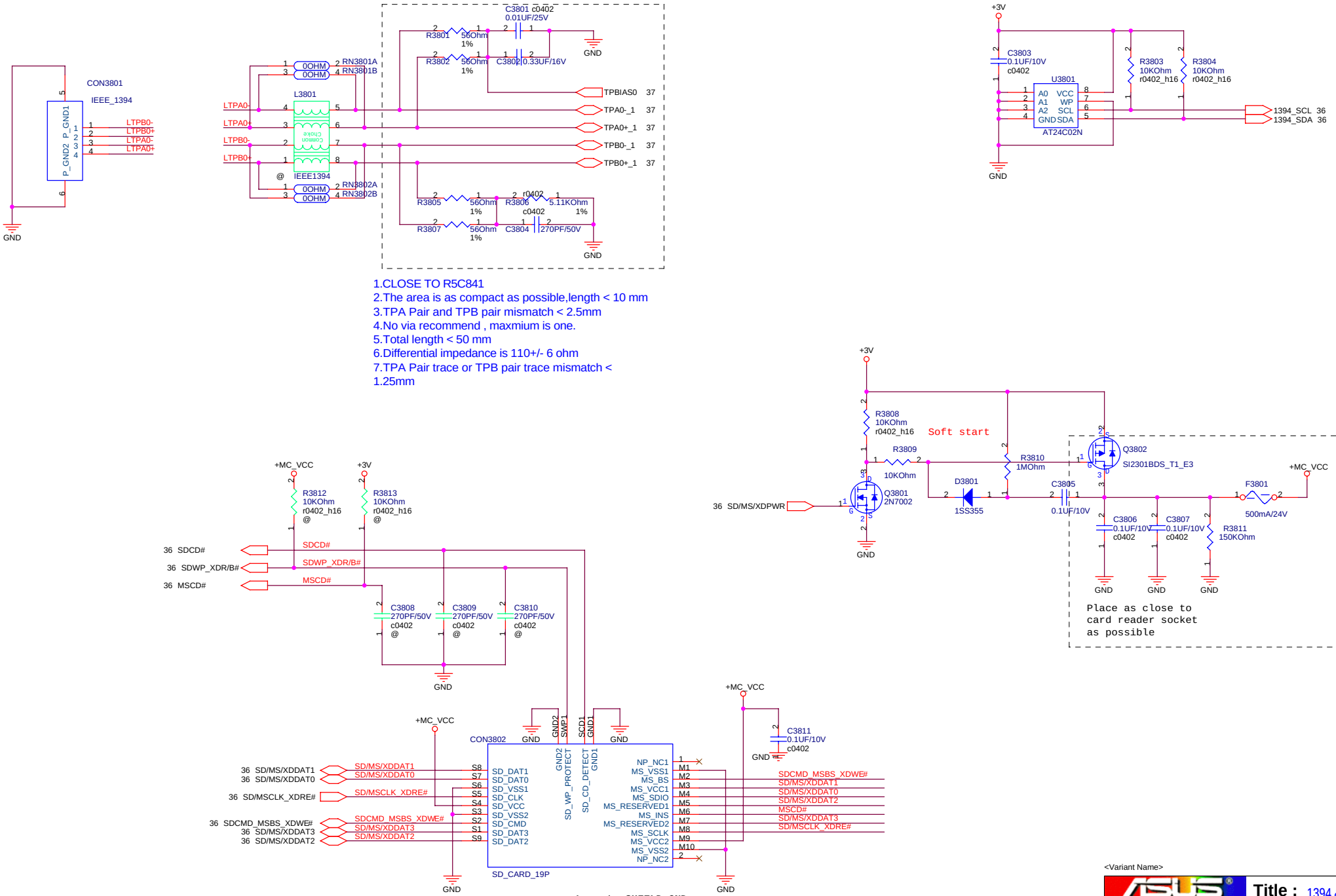
U3601C
R5C841-CSP208Q
Q3701
2N7002
Check with A7Z
U3602
R5531V002
U3603
74SZ74
U3604
PI5C3384
CON3701
PCMCIA_CON_84P
Layout: SHIELD GND
CCD1# CCD2#
L L 16bit
OTHER 32bit



<Variant Name>

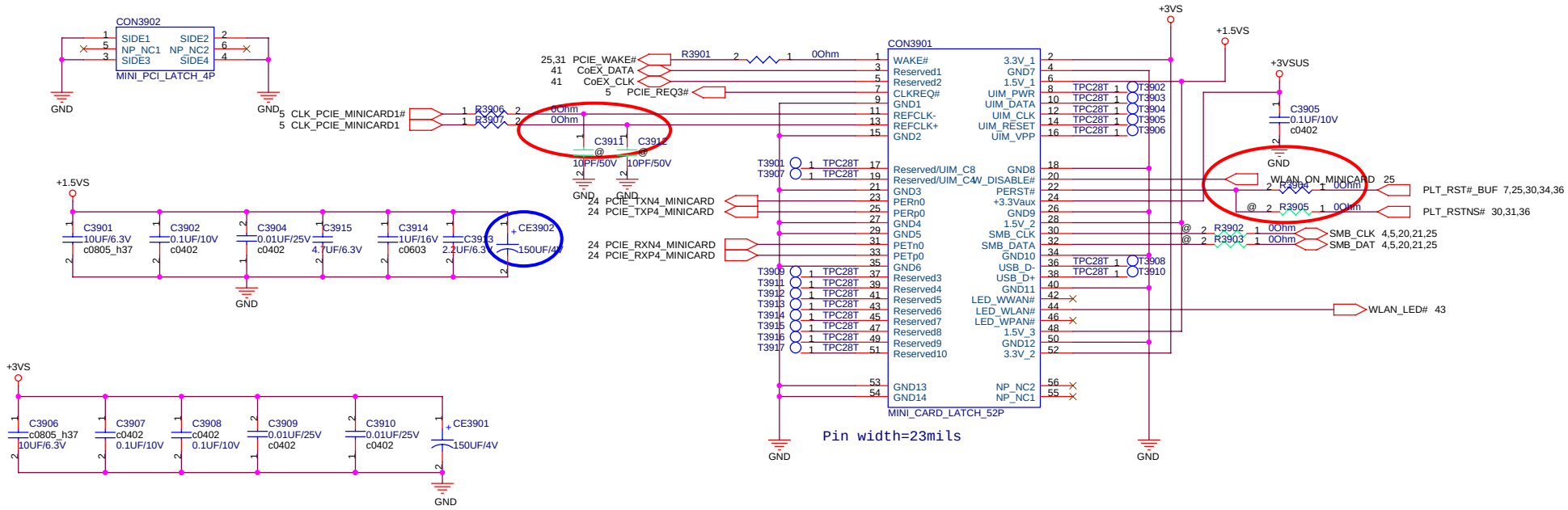
ASUSTeK COMPUTER INC

Title : 1394 & 3 IN 1 CON

Engineer: Marco Chen

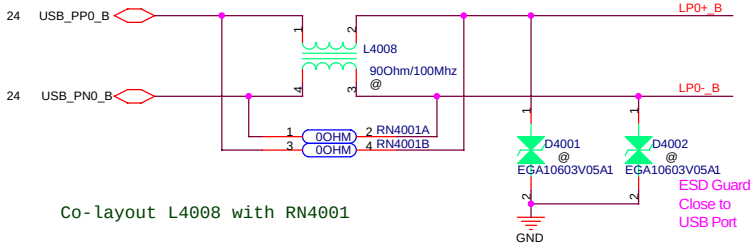
Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 38 of 63

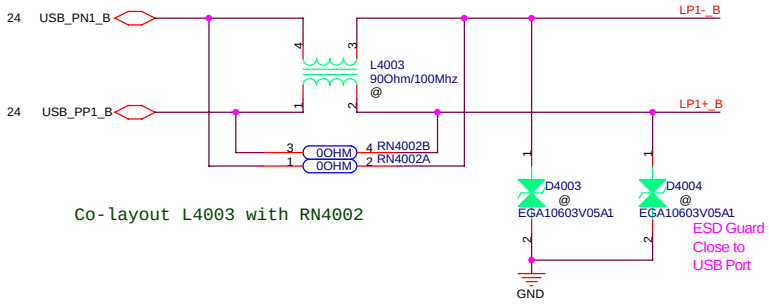


<Variant Name>

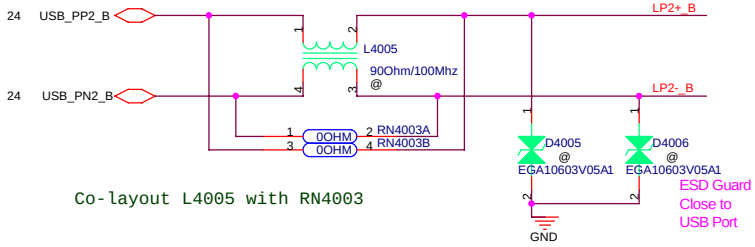
ASUSTeK COMPUTER INC	Title : MINICARD (Golan)	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 39 of 63	



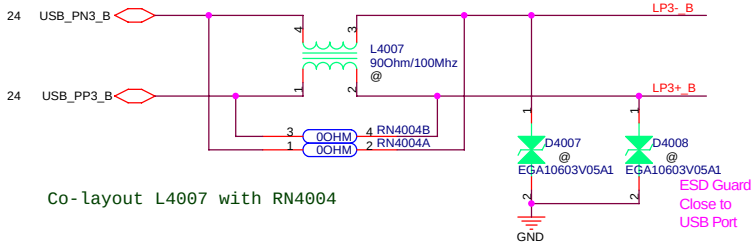
Co-layout L4008 with RN4001



Co-layout L4003 with RN4002

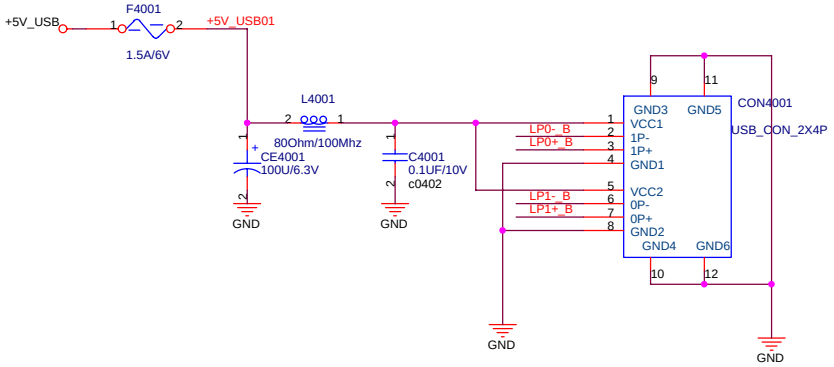


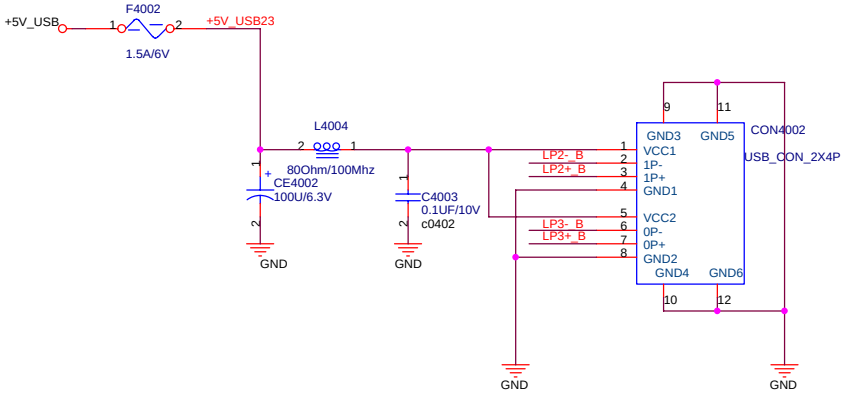
Co-layout L4005 with RN4003

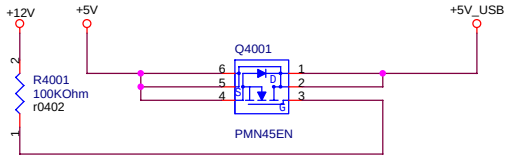


Co-layout L4007 with RN4004

4P2R array resister
co-layout with comman choke







<Variant Name>

ASUSTeK COMPUTER INC

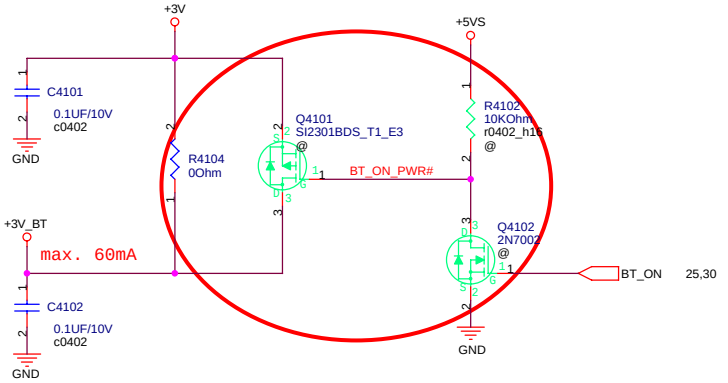
Title : USB CONN X 4

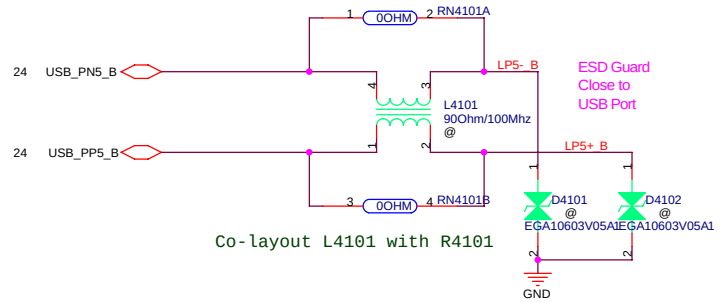
Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6Jc	2.1

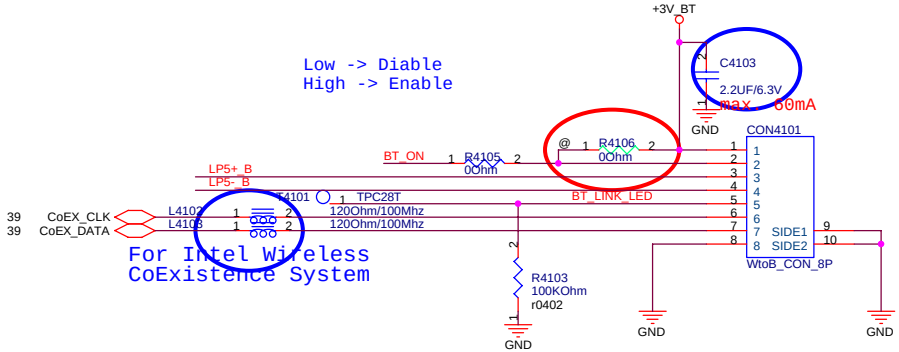
Date: Thursday, January 19, 2006 Sheet 40 of 63

BT ON/OFF Control





Bluetooth Module



<Variant Name>

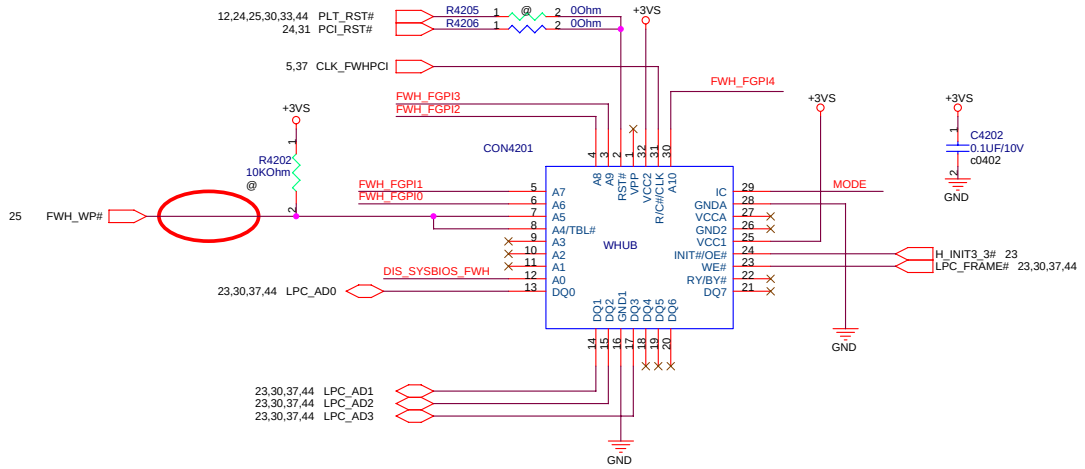
Title : Blue Tooth

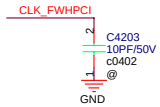
ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

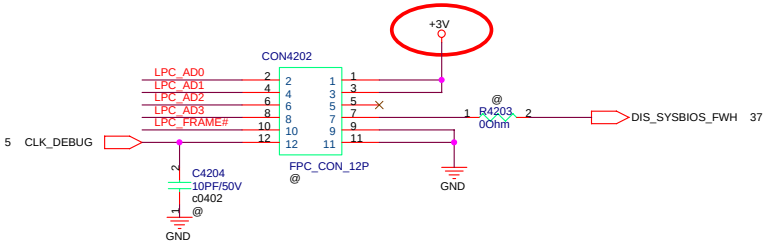
Size	Project Name	Rev
Custom	A6Jc	2.1

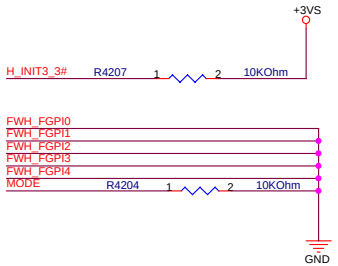
Date: Thursday, January 19, 2006 Sheet 41 of 63





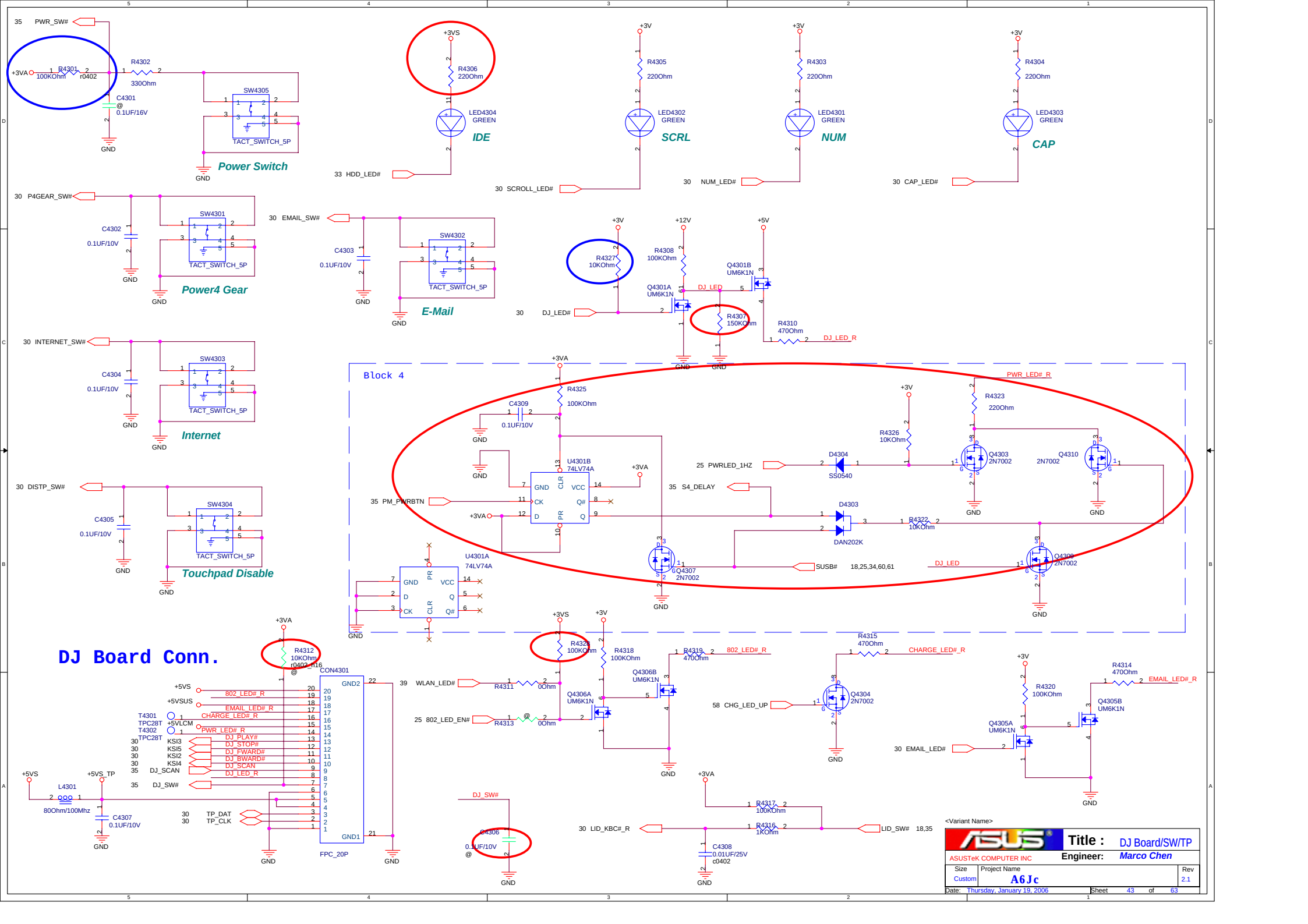
PLCC32 Socket Part Number : 12-043000323
SST FWH/LPC Part Number : 05G00101712L(燒)





<Variant Name>

ASUSTeK COMPUTER INC	Title : Startup Circuit	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 42 of 63	


35 PWR_SW#
+3VA
R4301 100KOhm r0402
R4302 330Ohm
C4301 @ 0.1UF/16V
SW4305
TACT_SWITCH_5P
GND
Power Switch
+3VS
R4306 220Ohm
LED4304 GREEN
IDE
33 HDD_LED#
+3V
R4305 220Ohm
LED4302 GREEN
SCRL
30 SCROLL_LED#
R4303 220Ohm
LED4301 GREEN
NUM
30 NUM_LED#
R4304 220Ohm
LED4303 GREEN
CAP
30 CAP_LED#
30 P4GEAR_SW#
C4302 0.1UF/10V
SW4301
TACT_SWITCH_5P
Power4 Gear
30 EMAIL_SW#
C4303 0.1UF/10V
SW4302
TACT_SWITCH_5P
E-Mail
R4327 10KOhm
+12V
R4308 100KOhm
Q4301A UM6K1N
Q4301B UM6K1N
DJ_LED
R4307 150KOhm
R4310 470Ohm
DJ_LED_R
30 DJ_LED#
30 INTERNET_SW#
C4304 0.1UF/10V
SW4303
TACT_SWITCH_5P
Internet
30 DISTP_SW#
C4305 0.1UF/10V
SW4304
TACT_SWITCH_5P
Touchpad Disable
Block 4
+3VA
R4325 100KOhm
C4309 0.1UF/10V
U4301B 74LV74A
35 PM_PWRBTN
25 PWRLED_1HZ
D4304 SS0540
R4326 10KOhm
R4323 220Ohm
PWR_LED#_R
Q4303 2N7002
Q4310 2N7002
35 S4_DELAY
D4303 DAN202K
R4322 10KOhm
U4301A 74LV74A
Q4307 2N7002
SUSB# 18,25,34,60,61
Q4309 2N7002
DJ_LED
DJ Board Conn.
R4312 10KOhm r0402_n16
CON4301
FPC_20P
+5VS
+5VSUS
+5VLCM
802_LED#_R
EMAIL_LED#_R
CHARGE_LED#_R
PWR_LED#_R
DJ_PLAY#
DJ_STOP#
DJ_FWARD#
DJ_BWARD#
DJ_SCAN
DJ_LED_R
DJ_SW#
TP_DAT
TP_CLK
L4301 80Ohm/100Mhz
+5VS_TP
C4307 0.1UF/10V
R4321 100KOhm
R4318 100KOhm
R4319 470Ohm
802_LED#_R
39 WLAN_LED#
R4311 0Ohm
25 802_LED_EN#
R4313 @ 0Ohm
Q4306A UM6K1N
Q4306B UM6K1N
R4315 470Ohm
CHARGE_LED#_R
58 CHG_LED_UP
Q4304 2N7002
R4320 100KOhm
R4314 470Ohm
EMAIL_LED#_R
Q4305A UM6K1N
Q4305B UM6K1N
30 EMAIL_LED#
C4306 0.1UF/10V @
R4317 100KOhm
R4316 1KOhm
30 LID_KBC#_R
LID_SW# 18,35
C4308 0.01UF/25V c0402
<Variant Name>
Title : DJ Board/SW/TP
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
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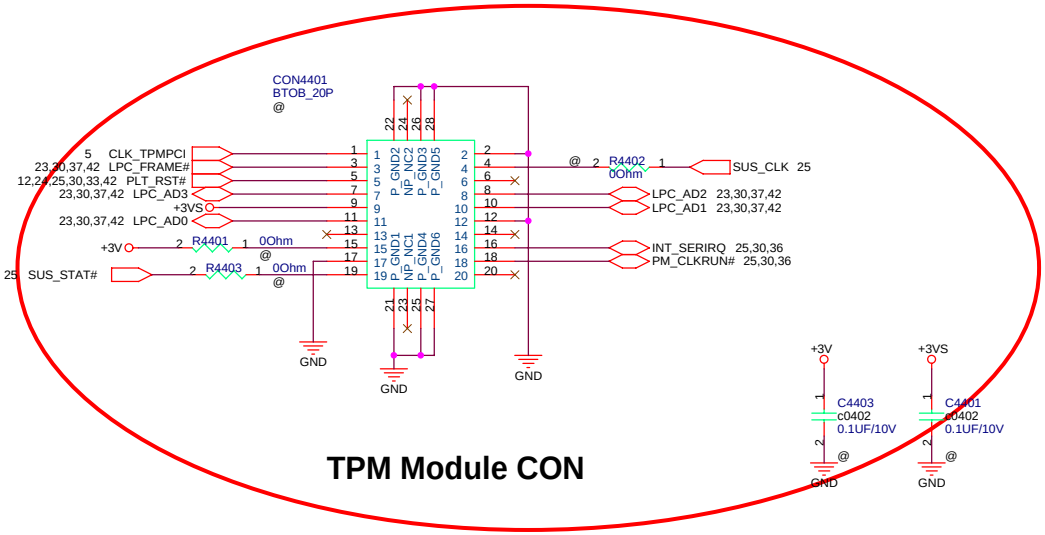
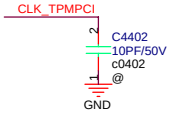
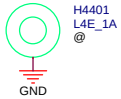


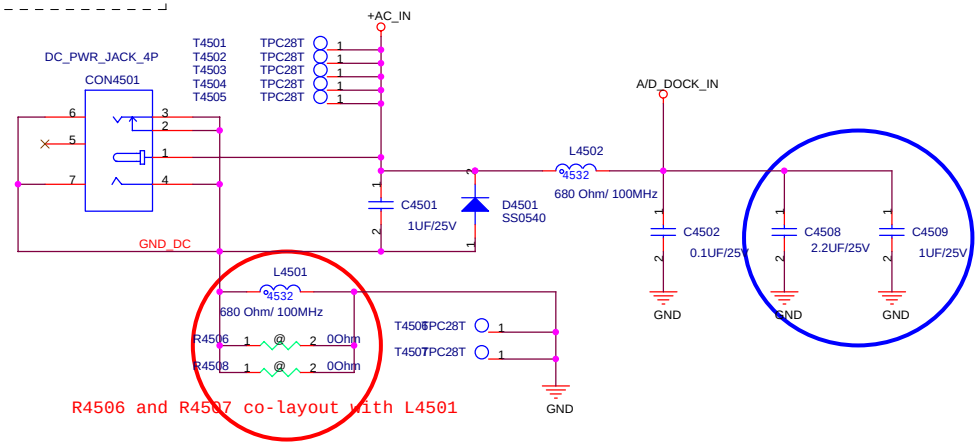


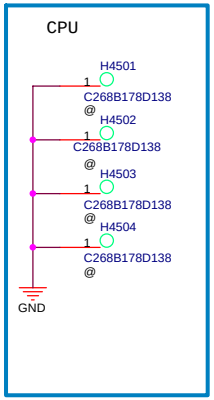


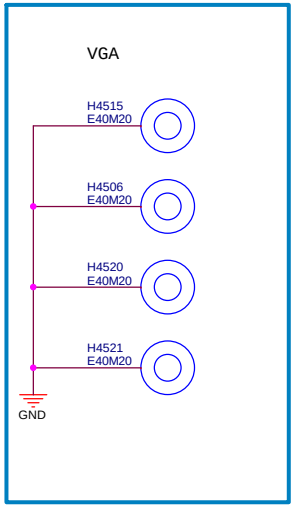
<Variant Name>

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: *Marco Chen*	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 44 of 63	

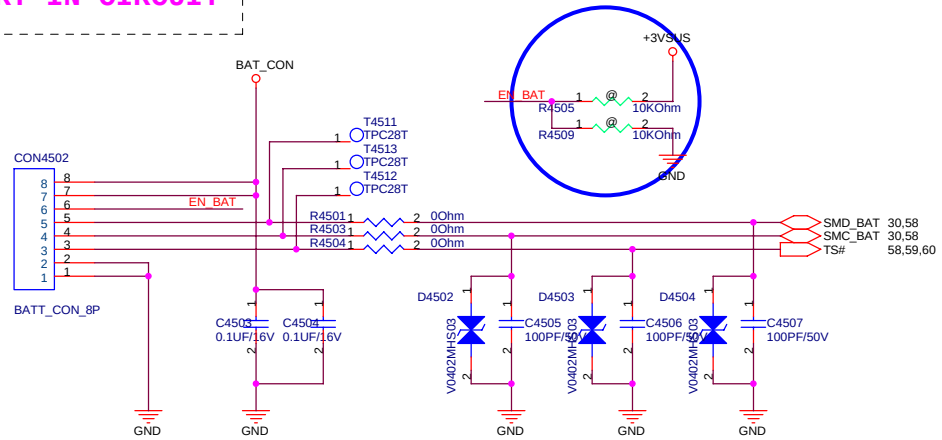
Adaptor IN Circuit

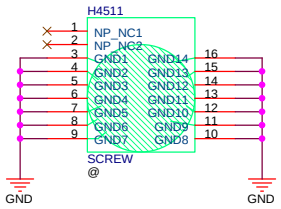


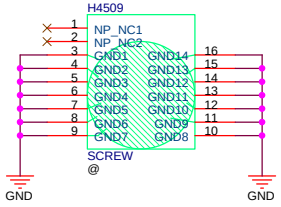


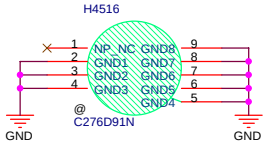


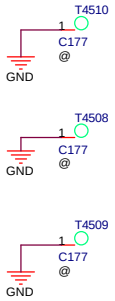
BATTERY IN CIRCUIT

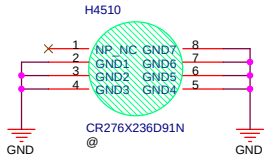


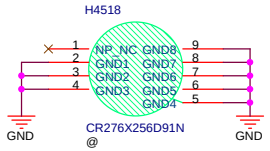


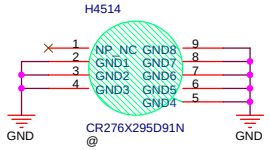


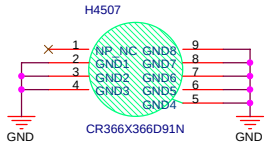


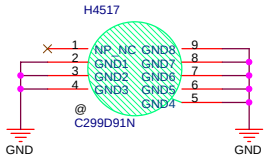


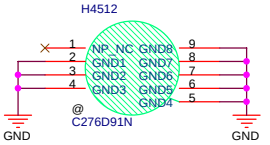


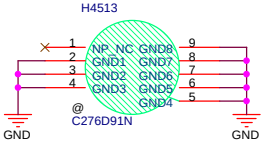


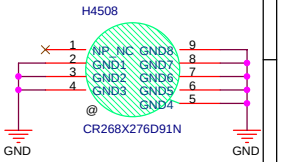




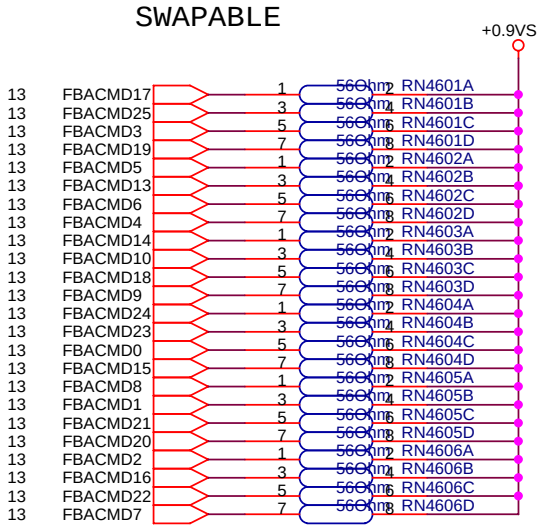




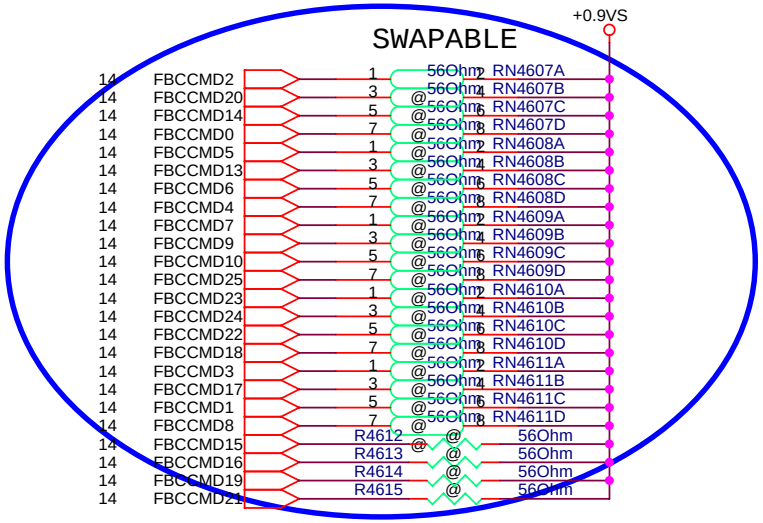




FBA CMD/ADDR Termination



FBC CMD/ADDR Termination



<Variant Name>

ASUS	Title : G73M-Termination	
<OrgName>	Engineer: Charles Lee	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 46 of 63	

Host	SM-Bus Device	SM-Bus Address	Device
ICH7-M	Clock Generator	1101001x (D2)	ICS954310
ICH7-M	SO-DIMM 0	1010000x (A0)	DDR SOCKET1
ICH7-M	SO-DIMM 1	1010001x (A4)	DDR SOCKET2
ICH7-M	Thermal Sensor	0101110x (5C)	ADT7463 (Optinal)

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D

<Variant Name>

Title : SYSTEM

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6Jc	2.1

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R1.0 -> R1.1

1. Page2: Add test points T215 and T216 for H_ADS# and H_CPURST#

2. Page4: Modify FAN solution from DA to PWM and change R-C delay timing.

   A. Mount R416 and DNI R415
   B. Change C404 to 1uF

3. Page4: Connect +3VS_FAN(R419*3.3K ohm and R420*2.2K ohm 分壓 from +V5S_FAN) to U401.3 because FAN_DA level is 3V and FAN_PWM# is open-drain, change pull-up to +3VS and U401.3 level shift from 5V to 3V

4. Page4: Add pull-down resister R418*10M ohm to protect noise when power-on

5. Page5: Add (R579*33 ohm and C529*10pF) for TPM PCI 33MHz clock

6. Page5: Change R531 from 10 ohm to 22ohm to eliminate swing.

7. Page5: DNI R510 to disable ITP enable.

8. Page7: Delete R715 because it duplicate with R529.

9. Page9: Change L905 to P/N:09G012030000 and L905 to P/N:09G013120409 because +1.5VS_PCIE consume about 1.3A and +1.5VS_3GPLL consume 200mA only.

10. Page13: VGA_GPIO5 add pull-up 10K ohm to +3VS for ATI recommendation.

11. Page13: DNI R1320 and mount R1321 to change back light enable from DC level to PWM and meet VBIOS support.

12. Page13: Add R1343*0 ohm for reserving bead to ground.

13. Page15: Change L1504.2 to connect from +VGA_VCORE to +1.2VSP for ATI recommendation.

14. Page15: Change bead L1506 from 120Ohm/100Mhz to 30Ohm/100Mhz type.

15. Page19: Add bead L1913 between TV_GND and GND.

16. Page23: Change High Definition damping resisters*R2312, R2314, R2316, R2318, R2320, R2322, R2324, R2325 from 22 ohm to 39 ohm for reducing reflection.

17. Page29: Add Line-in solution, please commt Black 2.

18. Page31, 32: Change LAN chip from Marvell 88E8053 to Realtek RTL8111B.

19. Page34: Add Q3401 and R3414 to replace U3402B.

20. Page34,35: Modify reset circuits to meet Intel specification, please commt Black 3.

21. Page35,43 : DNI R4312 and change R3509 from 4.7M ohm to 2.2 M ohm to short SWDJ_EN# detected to 2secends for BIOS requirement and add INIT# solution(please comment Block 7).

22. Page37: Change R3706 from 10K ohm to 100K ohm to enlarge R-C delay time.

23. Page39: Reserve R3905 to PLT_RSTNS# Wire-Or with PLT_RST#_BUF.

24. Page41: Short CON4101.1 and CON4101.2 and delete R4105, R4104, and C4103 because no timing issue between power and enable signal.

25. Page42: Delete D4201 and DNI R4202 because no power loss issue exist.

26. Page43: Modify S4 strech circuits, please comment Block 4.

27. Page44: Add TPM connecter.

28. Page45: Add C4508, C4509, R4506 and R4507 for EMI requirment.

29. Page42: Change CON4202.1 and CON4202.3 power from +3VSUS to +3V.

30. Page18: Change L1806.2 power from AC_BAT_SYS to AC_BAT_SYS_CPU for EMI requirement.

31. Page7: Change from VRM_PWRGD to ICH7_PWROK to enable MCH_PWROK for Intel requirement(Mount R721 and DNI R722).

32. Page23,34: Change thermal-trip solution.

   A. Mount R2315 and DNI R4507

   B. Remove the circuits.(please comment Block 5)

   C. Mount thermal protection circuits.(please comment Block 6)

33. Page5, 23, 37: Change capacitor values for TXC recommendations(C513,C514 from 33pF to 27pF, C2302, C2304 from 12pF to 22pF ,Change X3701 to 07G010S22450*30 ppm and C3725 and C3726 to 22pf).

34. Page15, 47: Add Back Bias circuits for ATI recommendations.

35. Page5, 23, 33: Add SATA circuits for OEM requirement.

36. Page12: Remove R1205 for ATI recommendations.

37. Page39: Reserve R-C to tune waveform quanlity.(R3906,R3907,C3911,C3912)

38. Page41: Reserve R4104, R4105, R4106 to modify enable blue tooth solution.

R1.1 -> R2.0

1. Page4, 34: Add power limit solution and change thermal protection solution.

   A. Add R421*0 ohm and connect to H_PROCHOT_S#
   B. DNI R417*0 ohm
   C. Add R422*0 ohm and connect to OVERTEMP# that is wire-or with FORCE_OFF#.
   D. DNI OTP solution.

2. Page15: Add BBIAS_CNTL pull-down resister R1508*10K ohm to GND.

3. Page19: Modify parts (D1912 and F1901).

4. Page24: Add 3 pcs decoupling CAPs(C2410, C2411, C2412) to short return path because PCI Bus(IN1) reference +1.8VS(Vcc).

5. Page25, 44: Add BT_LED solution to co-layout with Scroll Lock for Epson requirement.

6. Page27: Change R2704 from 0 ohm to 150 ohm.

7. Page27: Change R2707 from 47K ohm to 332K ohm.

8. Page27, 28: Add MUTE_POP# solution for Epson requirements. Please comment PR BlOCK 1.

9. Page30: Add LID switch solution.

   A. Change BAT_SEL# push-pull resister from +3V to GND.
   B. DNI Q3002*2N7002.

10. Page31: Change LAN chip reset signal from PLT_RSTNS# to PCI_RST#. (Mount R3107 and DNI R3106).

11. Page35: Change KBCRSM solution to connect to PM_PWRBTN# directly, please comment PR BLOCK 2.

12. Page36: Change CARDBUS chip reset signal from PLT_RST#_BUF to PLT_RST#. (Mount R3618 and DNI R3617).

13. Page39: Add WLAN_LED# pull-high resister R3908*100K ohm to solve LED was lighted when miniCARD was un-plug in.

<Variant Name>

ASUSTeK COMPUTER INC	Title : History (1)	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6Jc	Rev: 2.1
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14. Page40: Remove L4003, L4005, L4007, L4008 for EMI requirement.

15. Page43: Mount R4301*100K ohm to avoid PWR_SW# is floating.

16. Page43: Mount R4327*10K ohm to fix DJ_LED light soon issue when power on.

VGA NV G72M-V R1.0 -> R1.1

1. Page15: Change R1507 from 121 ohm to 0 ohm and Remove R1511 for SSC 3.3V requirment.
2. Page13: Change VRAM CLK Terminators R1303, R1304 from 120 ohm to 100 ohm for NV recommendation.
3. Page14: Change VRAM CLK Terminators R1402, R1403 from 120 ohm to 100 ohm for NV recommendation.
4. Page16: Change DACX_RSET R1605, R1607 to 124 ohm and remove R1604, R1606 for NV recommendation.
5. Page17: Mount 3GIO_PADCFG R1720 and DNI R1721 for NV recommendation.
6. Page17: Change RN1701 from 4R8P 0603 to 4R8P 0402 for BOM issue
7. Page19: Change D1913 from LM385M3 to BAV99.
8. Page19: Change L1901, L1905, L1906 to 180NH.
9. Page43: DJ_LED# Pull high to +3V via R4327 10Kohm.
10. Page35: Add D3509 (DNI) in parallel to R3532 for C3506 discharge path.
11. Page34: Change U3404 RN5VD to CMOS Topology and R3402(DNI).
12. Page04: Change R420 from 22K ohm to 10K ohm and change R419 from 33K ohm to 20K ohm for Volt divide.
13. Page43 :DNI C4306.
14. Page05: Change R519,R546 from 1 ohm to 2.7 ohm.
15. Page27: Change CE2701 from 47uF to 22uF and rename to C2727.
16. Page32: Change CE3301, CE3302 from 47uF to 22uF and rename to C3314, C3315.
17. Page17: Add U3003, Q3008(DNI) for 4S1P Battery detected.
18. Page23: Change X2301 to PN:07G010303270.
19. Page31: Change X3101 to PN:07G010S22500 for cost issue.
20. Page37: Change con3701 footprint to "nb_pcmcia_84p_6hold_a3n_lf2" for factory issue.
21. Page45: Change H4506, H4515, H4520, H4521 footprint to "nb_smt_nut_e40m20_lf2" for factory issue.
22. Page43: WLAN_LED# Pull-high to +3VS via R4328.
23. Page29: Change U2902 to PN 06G010147010.
24. Page14: Add R1415 and DNI L1403 for NV recommendation.
25. Page28: Change R2832 from 10K to 100K and R2806(DNI).
26. Page27: Change R2704 from 0 ohm to 100ohm.
27. Page35: Change R3509 from 2.2M ohm to 1Mohm and C3504 change from 1uF to 4.7uF.
28. Page31: Change R3106 DNI and R3107 stuff .
29. Page27: Change R2707 from 47k ohm to 332K ohm.
30. Page43:Mount R4301
31. Page35: Modify KBCRSM Circuit.
32. Page30:Add D3003 and C3007.

VGA NV G72M-V R1.1 -> R2.0

1. Page19: Change L1901, L1905, L1906 to 09G013120409 120ohm/100MHz.
2. Page31: Change C3133,C3134 from 22PF to 27PF.
3. Page46: Change ChipResistor RN4607~RN4612 to Single Resistor R4607 ~ R4630.
4. Page45: Change C4509 from 10uF to 2.2uf.
5. Page19: Change R1910 from 33Kohm to 47Kohm for BOM reduction.
6. Page15: Change R1501 from 71.5ohm to 81.6ohm for BOM reduction.
7. Page25: Add R2550 ,R 2553, R2555 for BT_ON.
8. Page14: Mount R1414 for NV recommendation.

C2827	MLCC 2.2UF/10V(0603)Y5V+80-20%	-->	MLCC 2.2UF/6.3V(0603)X5R 10%
C3007	CAP 2.2UF/6.3V(0603) Y5V (225)	-->	MLCC 2.2UF/6.3V(0603)X5R 10%
C3503	MLCC 2.2UF/6.3V(0603)Y5V+80-20	-->	MLCC 2.2UF/6.3V(0603)X5R 10%
C3506	MLCC 2.2UF/6.3V(0603)Y5V+80-20	-->	MLCC 2.2UF/6.3V(0603)X5R 10%
C3502	MLCC 4.7UF/6.3V(0805) X5R 20%	-->	MLCC 4.7U/6.3V(0805) X7R 10%
C3405	MLCC 2.2UF/6.3V(0603)X5R 10%	不變	
C3411	MLCC 0.22UF/10V(0603)X7R 10%	不變	
C3504	MLCC 4.7UF/6.3V(0603)X5R 10%	不變	

<Variant Name>

Title : History(2)

<OrgName> Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6Jc	2.1

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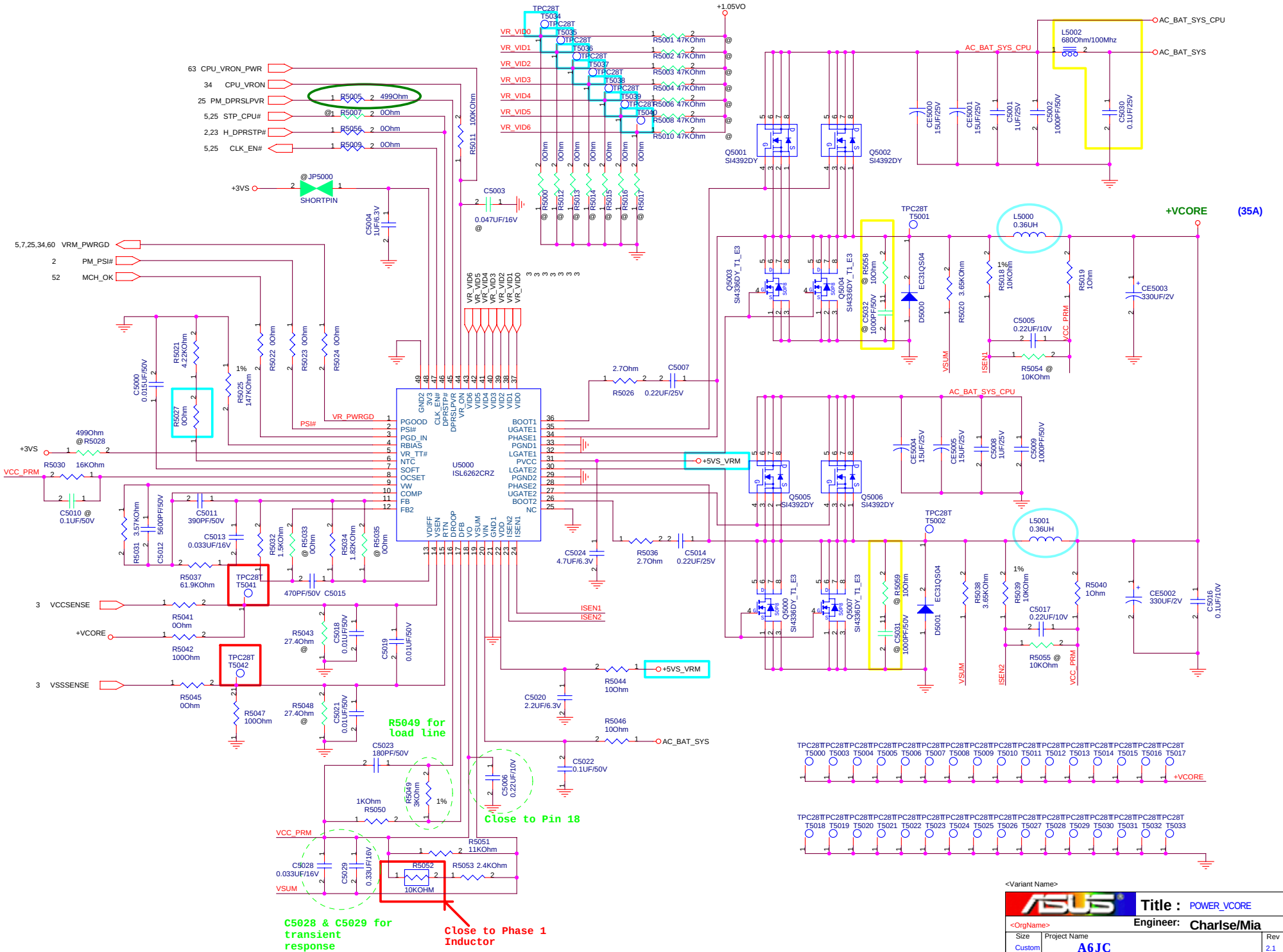
+VCORE (35A)
U5000 ISL6262CRZ
Q5001 SI4392DY
Q5002 SI4392DY
Q5005 SI4392DY
Q5006 SI4392DY
Q5003 SI4336DY_T1_E3
Q5004 SI4336DY_T1_E3
Q5000 SI4336DY_T1_E3
Q5007 SI4336DY_T1_E3
L5000 0.36UH
L5001 0.36UH
L5002 680Ohm/100Mhz
AC_BAT_SYS_CPU
AC_BAT_SYS
+5VS_VRM
+3VS
VCC_PRM
VSUM
ISEN1
ISEN2
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
63 CPU_VRON_PWR
34 CPU_VRON
25 PM_DPRSLPVR
5,25 STP_CPU#
2,23 H_DPRSTP#
5,25 CLK_EN#
5,7,25,34,60 VRM_PWRGD
2 PM_PSI#
52 MCH_OK
3 VCCSENSE
3 VSSSENSE
SHORTPIN
R5049 for load line
Close to Pin 18
C5028 & C5029 for transient response
Close to Phase 1 Inductor
Title : POWER_VCORE
Engineer: Charlse/Mia
Project Name A6JC
Size Custom
Rev 2.1
Date: Thursday, January 19, 2006
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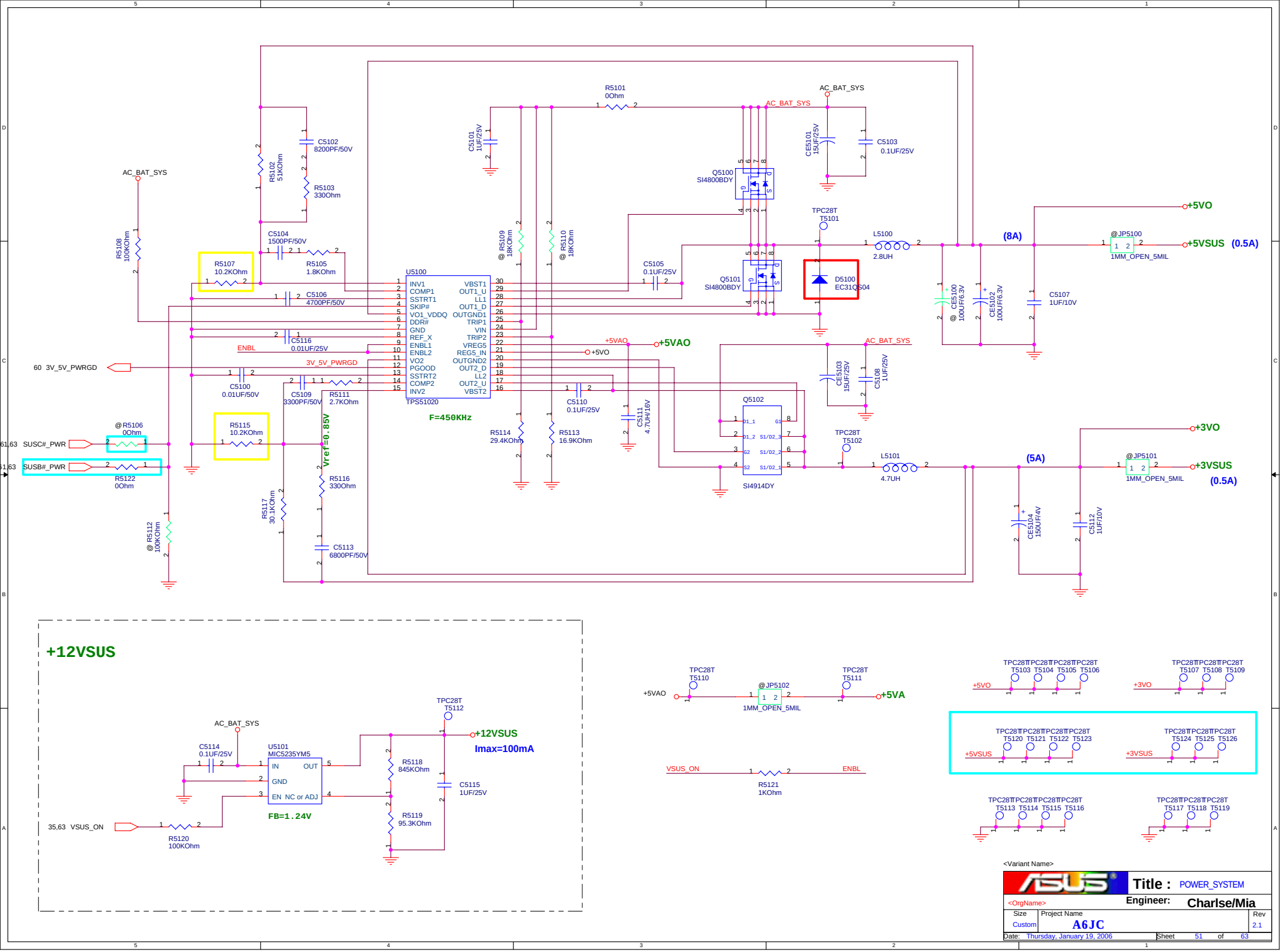

<Variant Name>

Title : POWER_SYSTEM

<OrgName>

Engineer: Charlse/Mia

Size	Project Name	Rev
Custom	A6JC	2.1

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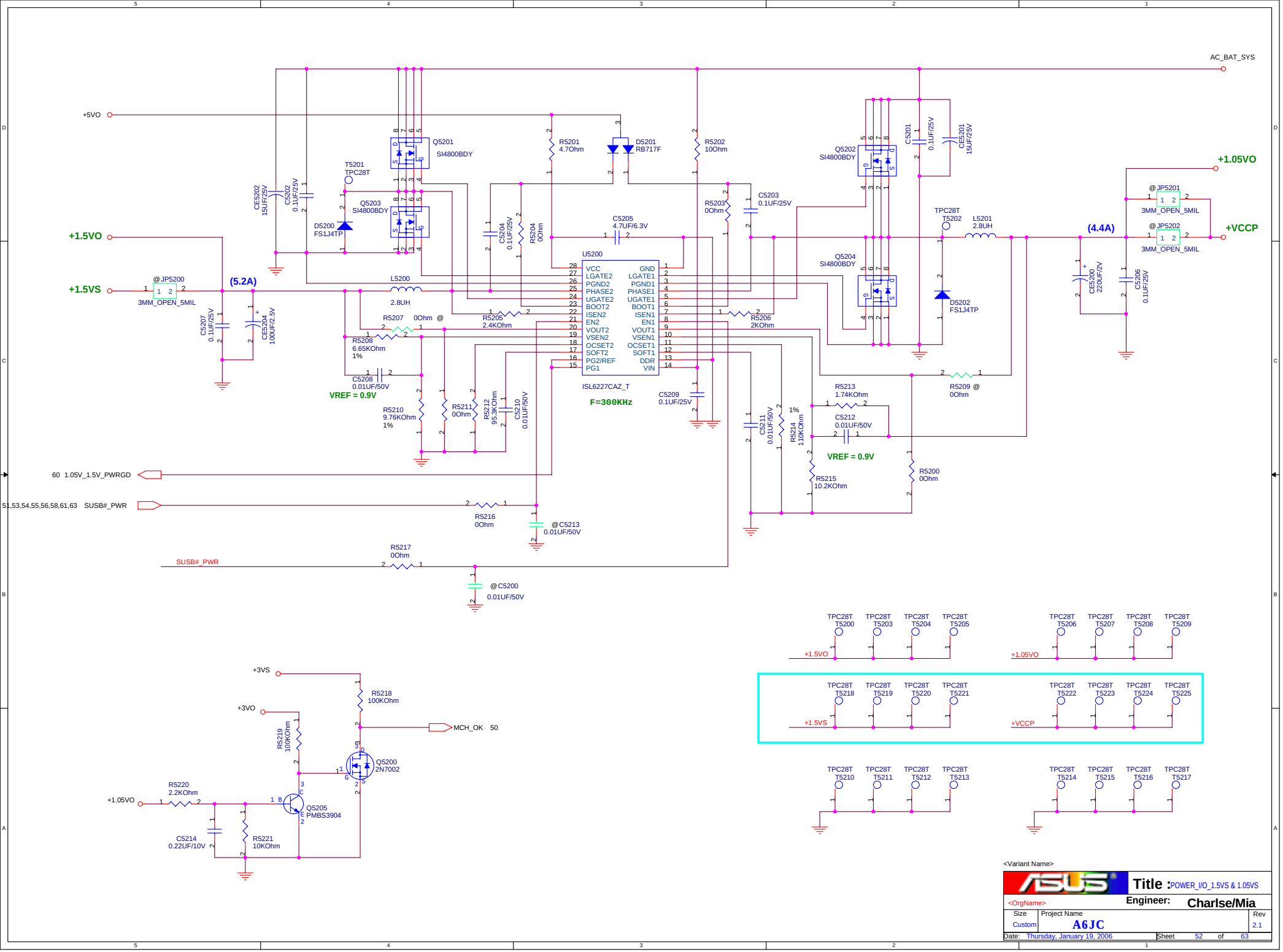
AC_BAT_SYS
+5VO
+1.5VO
+1.5VS
+1.05VO
+VCCP
(5.2A)
(4.4A)
Q5201
SI4800BDY
Q5203
SI4800BDY
Q5202
SI4800BDY
Q5204
SI4800BDY
T5201
TPC28T
D5200
FS1J4TP
D5201
RB717F
D5202
FS1J4TP
R5201
4.7Ohm
R5202
10Ohm
R5203
0Ohm
R5204
0Ohm
R5205
2.4KOhm
R5206
2KOhm
R5207
0Ohm
R5208
6.65KOhm
1%
R5209
0Ohm
R5210
9.76KOhm
1%
R5211
0Ohm
R5212
95.3KOhm
R5213
1.74KOhm
R5214
110KOhm
R5215
10.2KOhm
R5216
0Ohm
R5217
0Ohm
R5200
0Ohm
C5201
0.1UF/25V
CE5201
15UF/25V
C5202
0.1UF/25V
CE5202
15UF/25V
C5203
0.1UF/25V
C5204
0.1UF/25V
C5205
4.7UF/6.3V
C5206
0.1UF/25V
C5207
0.1UF/25V
CE5204
100UF/2.5V
CE5200
220UF/2V
C5208
0.01UF/50V
C5209
0.1UF/25V
C5210
0.01UF/50V
C5211
0.01UF/50V
C5212
0.01UF/50V
@JP5200
3MM_OPEN_5MIL
@JP5201
3MM_OPEN_5MIL
@JP5202
3MM_OPEN_5MIL
L5200
2.8UH
L5201
2.8UH
U5200
VCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
ISEN2
EN2
VOUT2
VSEN2
OCSET2
SOFT2
PG2/REF
PG1
GND
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISEN1
EN1
VOUT1
VSEN1
OCSET1
SOFT1
DDR
VIN
ISL6227CAZ_T
F=300KHz
VREF = 0.9V
VREF = 0.9V
60 1.05V_1.5V_PWRGD
51,53,54,55,56,58,61,63 SUSB#_PWR
SUSB#_PWR
@C5213
0.01UF/50V
@C5200
0.01UF/50V
+3VS
+3VO
+1.05VO
R5218
100KOhm
R5219
100KOhm
R5220
2.2KOhm
R5221
10KOhm
C5214
0.22UF/10V
Q5200
2N7002
Q5205
PMBS3904
MCH_OK 50
TPC28T T5200
TPC28T T5203
TPC28T T5204
TPC28T T5205
TPC28T T5206
TPC28T T5207
TPC28T T5208
TPC28T T5209
TPC28T T5218
TPC28T T5219
TPC28T T5220
TPC28T T5221
TPC28T T5222
TPC28T T5223
TPC28T T5224
TPC28T T5225
TPC28T T5210
TPC28T T5211
TPC28T T5212
TPC28T T5213
TPC28T T5214
TPC28T T5215
TPC28T T5216
TPC28T T5217
<Variant Name>
Title : POWER_I/O_1.5VS & 1.05VS
<OrgName>
Engineer: Charlse/Mia
Size Custom
Project Name A6JC
Rev 2.1
Date: Thursday, January 19, 2006
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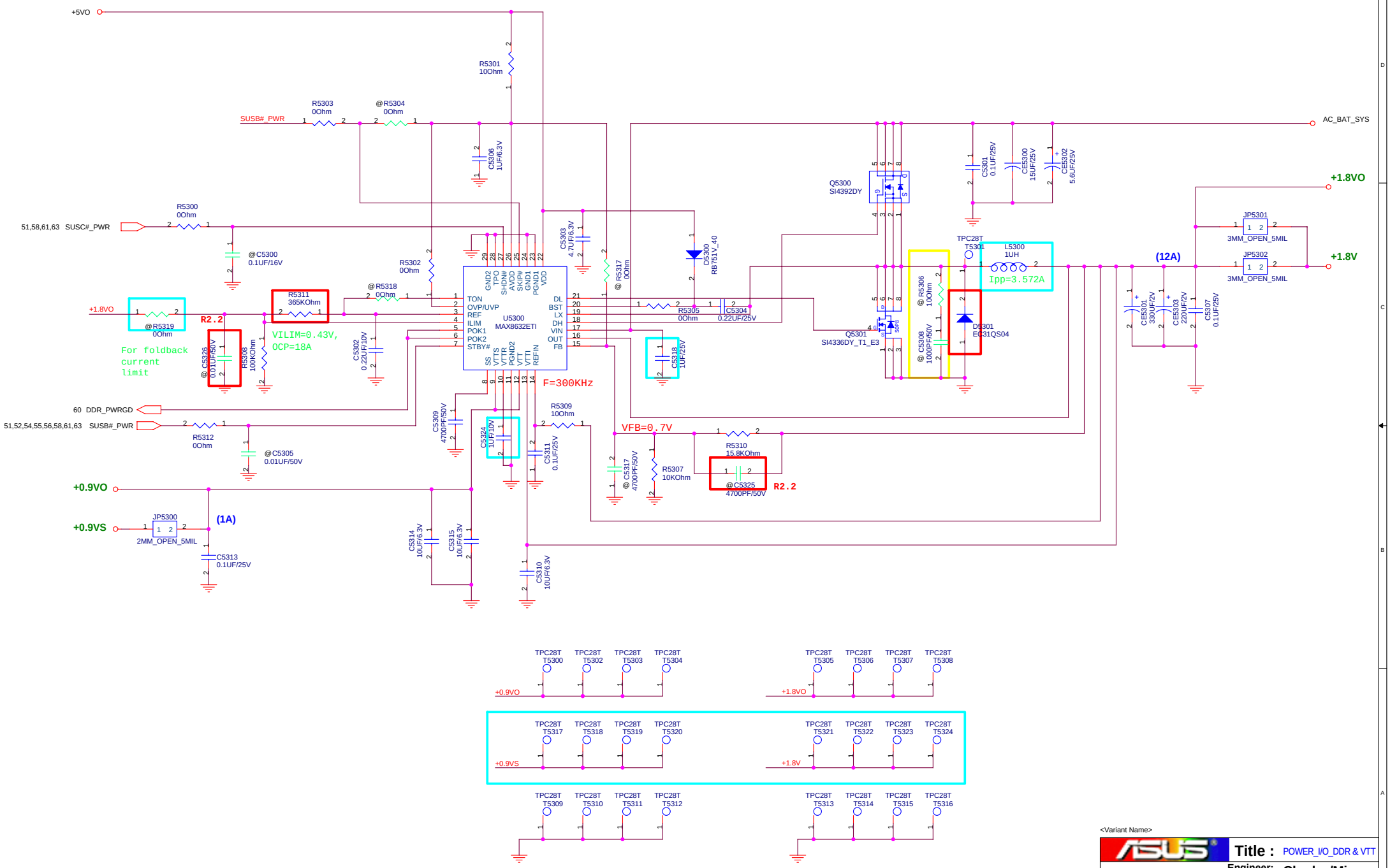


<Variant Name>

Title : POWER_I/O_DDR & VTT

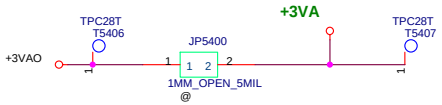
<OrgName>

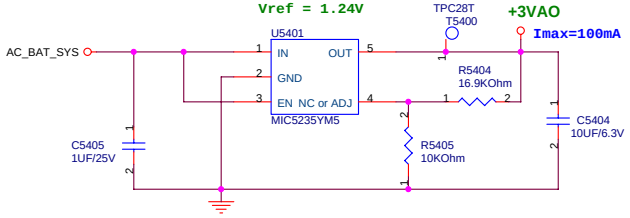
Engineer: Charlse/Mia

Size	Project Name	Rev
Custom	A6JC	2.1

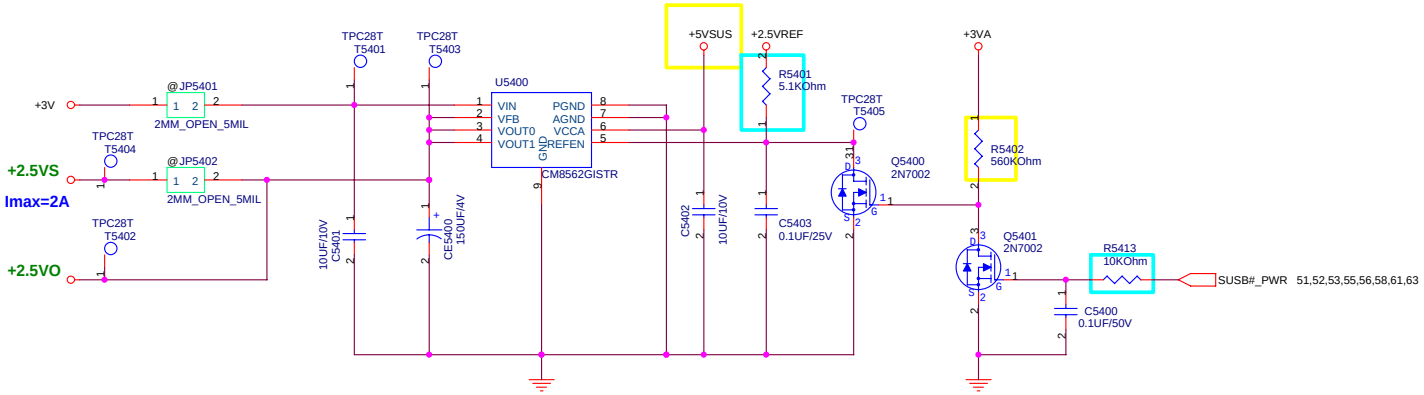
Date: Thursday, January 19, 2006 Sheet 53 of 63

+3VA0



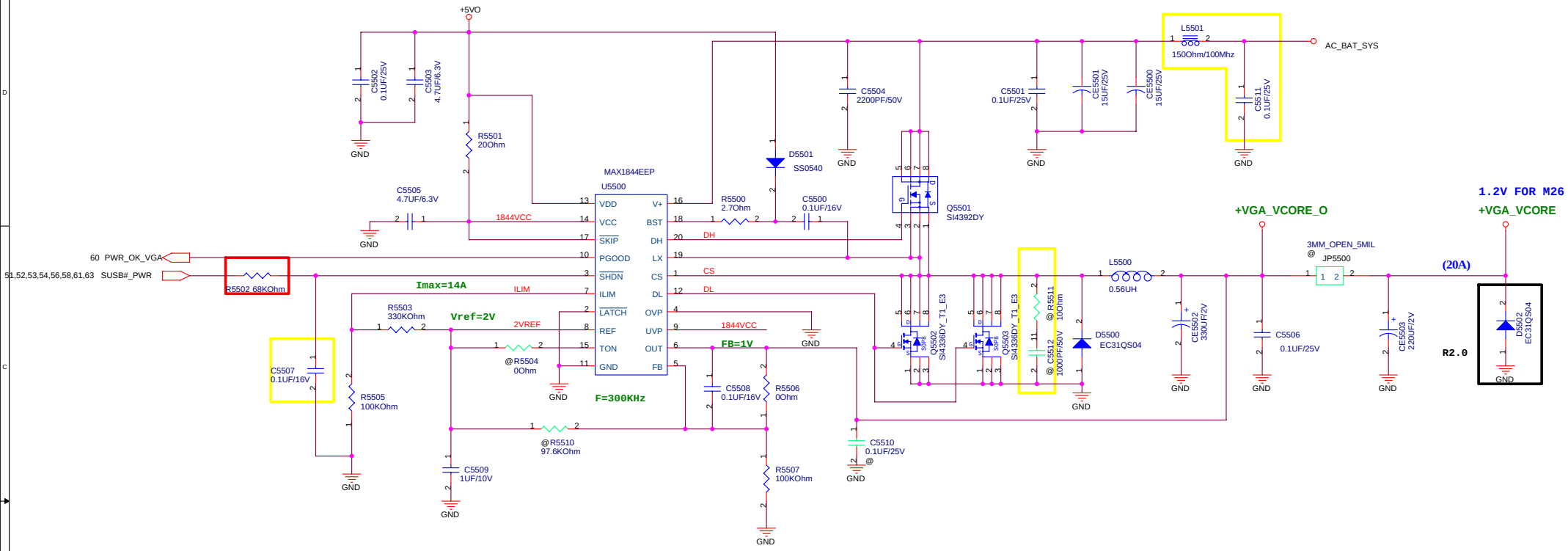


+2.5VS

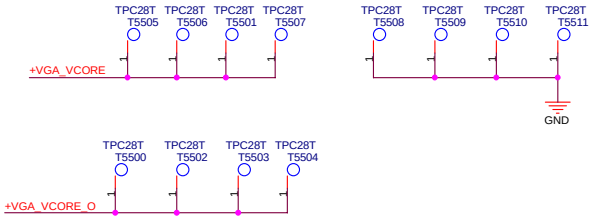


<Variant Name>

<OrgName>	Title : POWER_I/O_+3VA & +2.5V	
	Engineer: Charlse/Mia	
Size: Custom	Project Name: A6JC	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 54 of 63	



Model	VGA	+VGA_CORE	R5506	R5507	R5510
A6JC	G72M-V	1.0V	0	100K	@
A6JM	G73M	1.1V	10K	100K	@



<Variant Name>

Title : +VGA_CORE

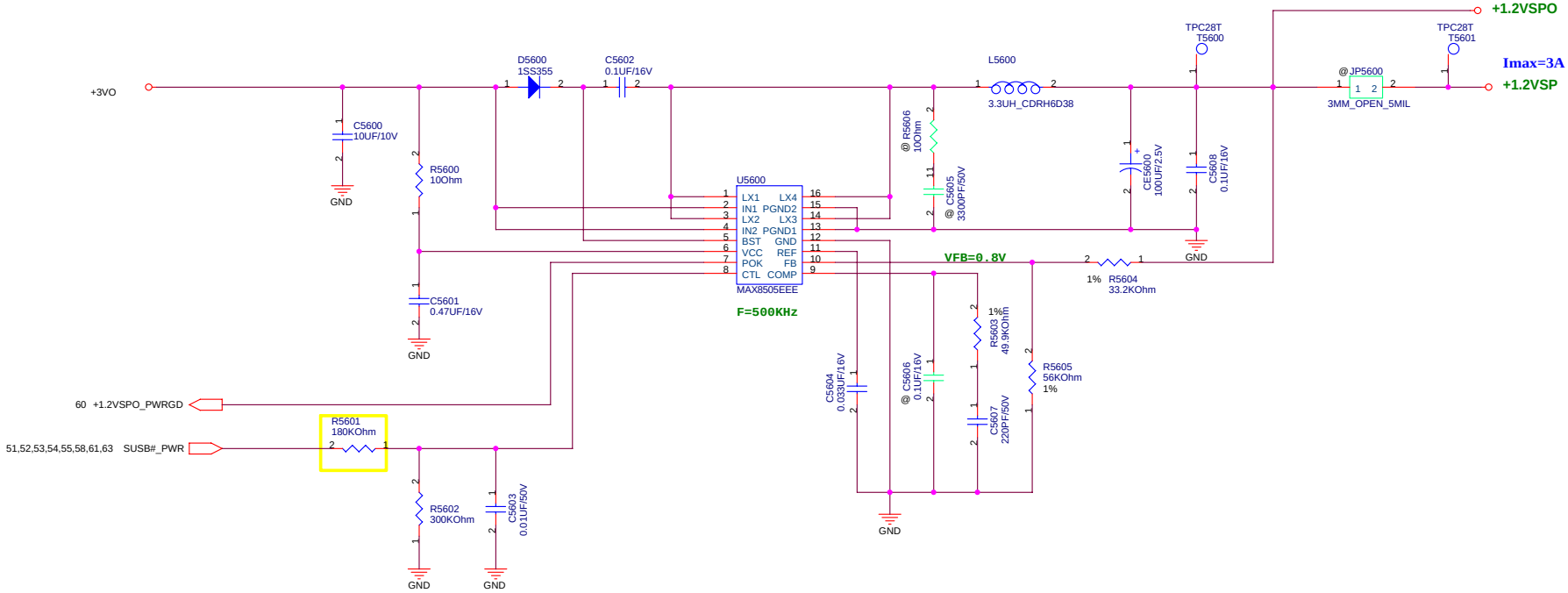
<OrgName>

Engineer: Charlse/Mia

Size	Project Name	Rev
Custom	A6JC	2.1

Date: Thursday, January 19, 2006 Sheet 55 of 63

+1.2VSP



<Variant Name>

Title : POWER_VGA_+1.2VSP

<OrgName> Engineer: Charlse/Mia

Size	Project Name	Rev
Custom	A6JC	2.1

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TOTAL POWER=65W
-->3.42A

BATSEL_2P# = "H" (1P)			
BAT cpapcity	R5712	VICTL(V)	ICHG(A)
2000mAH	41.2K	1.8976	1.39
2200mAH	52.3K	2.0989	1.537
2400mAH	66.5K	2.2918	1.679
2600mAH	86.6K	2.4871	1.822

45,59,60 A/D_DOCK_IN
A/D_DOCK_IN
TPC28T T5700 TPC28T T5701 TPC28T T5702 TPC28T T5703
Q5700 TPC8107
Q5718 TPC8107
R5700 100KOhm
R5701 100KOhm
Q5719 2N7002
AC_APR_UC
CSSP
CSSN
C5701 0.1UF/25V
CE5700 5.6UF/25V
CE5705 15UF/25V
Q5701 SI4336DY_T1_E3
C5702 0.1UF/50V
D5701 1SS355
R5702 2.70hm
VIINP
R5703 100KOhm
C5703 0.1UF/25V
MAX8724_REF
MAX8724_LDO
R5708 40.2KOhm
D5700 1SS355
Vref = 4.096V
VLDO = 5.4V
TPC28T T5725
TPC28T T5726
U5700 MAX8724ETI
DCIN LDO CLS REF CCS CCI CCV SHDN# ICHG ACOK# REFIN VCTL GND1 GND2 INP CSSN DH BST LX DLOV DLO PGND CSIP CSIN CELLS BATT VCTL
R5712 41.2KOhm 0.1%
Q5705 2N7002
30,58 BATSEL_2P#
R5715 220KOhm 1%
C5700 1UF/25V
C5705 1UF/16V
C5706 1UF/16V
C5708 22PF/50V
R5713 10KOhm
C5707 100PF/50V
R5714 1KOhm 1%
C5709 100PF/50V
MAX8724_LDO
TPC28T T5728
VCTL= LDO
=> Vbatt = 4.2V X CELLS
R5737 0Ohm
TPC28T T5727
R5716 57.6KOhm 0.1%
MAX8724_REF
VICTL= 3.325V => 3S
VICTL= 2.506V => 4S
A/D_DOCK_IN
R5717 100KOhm
R5719 13.3KOhm
VICHG
R5720 10KOhm 0.1%
C5710 0.1UF/25V
@D5703 1SS355
R5718 40.2KOhm 0.1%
R5721 75KOhm 0.1%
C5722 1UF/16V
Q5723 PMBS3904
@D5710 RB751V_40
R5738 16.5KOhm
R5723 20KOhm 0.1%
R5739 35.7KOhm
Charge Current Ichg =
[0.075V/Rsense(CHG)]*[VCLS/4.096V]
Rsense(CHG)=0.025 ohm
VICTL= 3.4632V => Ichg = 2.53A
+5VCHG
R5722 100KOhm
D5706 1SS355
60 A/D_SD#
30 BAT_LEARN
58 AC_APR_UC
Q5708 2N7002
Q5710 2N7002
@R5747 100KOhm
R5725 100KOhm
AC_BAT_SYS
59 ACOK#
ACOK#

L5704 150Ohm/100Mhz
L5700 150Ohm/100Mhz
BAT
BAT_S
TPC28T T5708
L5701 1KOhm/100Mhz
TPC28T T5704 TPC28T T5705 TPC28T T5706 TPC28T T5707
BAT_CON
TPC28T T5709 TPC28T T5710 TPC28T T5711 TPC28T T5712
AC_BAT_SYS
CE5701 15UF/25V
TPC28T T5713 TPC28T T5714 TPC28T T5715 TPC28T T5716
L5702 3.3UH
R5704 10mOHM_3720
R5705 25mOhm
Q5702 TPC8107
TPC28T T5717 TPC28T T5718
BAT
CE5702 15UF/25V
R5706 100KOhm
CSSN_G
Q5703 SI4392DY
D5702 EC31QS04

AC_BAT_SYS
+5VA
R5709 100KOhm
Q5704 2N7002
R5710 100KOhm
R5711 100KOhm
C5721 0.1UF/25V
D5704 1SS355
CHG_EN# 58
Q5706 2N7002
58 PRECHG
Q5707 2N7002
AC_APR_UC
D5705 1SS355

CHG_EN#	AC_APR_UC	SWITCH
H	H	OFF
H	L	ON
L	H	ON
L	L	ON

A/D_DOCK_IN
@R5728 200KOhm
Vfb=1.25V
@U5701 MAX1836EUT33
T5722 TPC28T
T5721 TPC28T
PRECHG
T5720 TPC28T
+PREBAT
@L5703 22UH
@D5707 FS1J4TP
BAT
T5724 TPC28T
+PREBAT
T5723 TPC28T
@D5708 FS05J10TP
@C5703 560UF/25V
@R5732 22KOhm
@C5704 150UF/25V
@C5713 0.1UF/25V

PRE_CHARGE CIRCUIT
Pre-charge voltage 12.6V

Q5722 SI2301BDS_T1_E3
AC_BAT_SYS
R5746 4.7OHM
BAT
R5745 100KOhm
R5744 150KOhm
PRECHG
Q5721 2N7002

Adaptor error circuit for 4S battery
Vth = 17.5V (MAX. 17.8V & MIN. 17.2V)

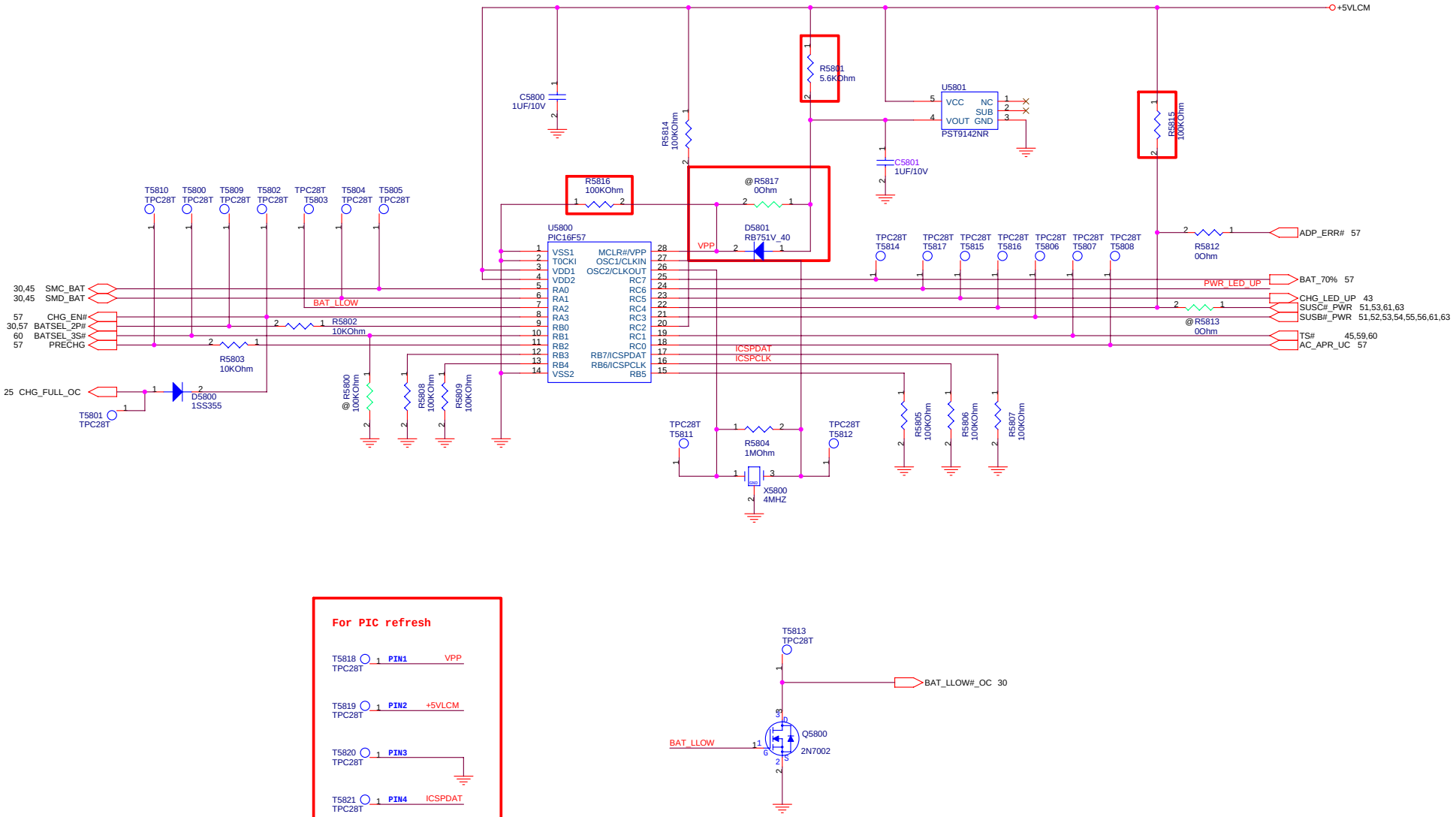
A/D_DOCK_IN
R5730 120KOhm
+2.5VREF
U5705 LMV321IDBVR
R5731 20KOhm
C5718 0.1UF/25V
+5VLCM
D5711 1SS355
R5729 100KOhm
C5719 0.1UF/25V
C5720 1UF/6.3V
+5VCHG
U5704 NL17SZ08XV5T2
R5733 100KOhm
Q5712 2N7002
TPC28T T5729
ADP_ERR#
ADP_ERR# 58
Q5711 2N7002

Power Limit Circuit

+5VLCM
U5706 NC7SZ14P5X
TPC28T T5730
4.25 PWRLMT#
R5736 10KOhm
C5717 47UF/6.3V
C5716 0.1UF/25V
D5709 1SS355
R5748 470KOhm
U5702 LMV358IDR
VICHG
C5715 0.1UF/25V
+2.5VREF
R5742 107KOhm 0.1%
C5712 0.1UF/25V
R5741 75KOhm 0.1%
Q5716 2N7002
U5707 NC7SZ14P5X
Q5717 2N7002
BAT_70% 58

<Variant Name>
Title : POWER_CHARGER
<OrgName>
Engineer: Charlse/Mia
Size C | Project Name A6JC | Rev 2.1
Date: Thursday, January 19, 2006 | Sheet 57 of 63

PIC16F57



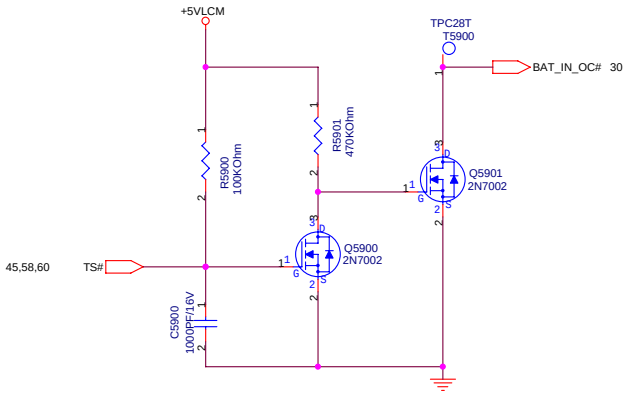
For PIC refresh

- T5818 TPC28T — PIN1 — VPP
- T5819 TPC28T — PIN2 — +5VLCM
- T5820 TPC28T — PIN3
- T5821 TPC28T — PIN4 — ICSPDAT
- T5822 TPC28T — PIN5 — ICSPCLK

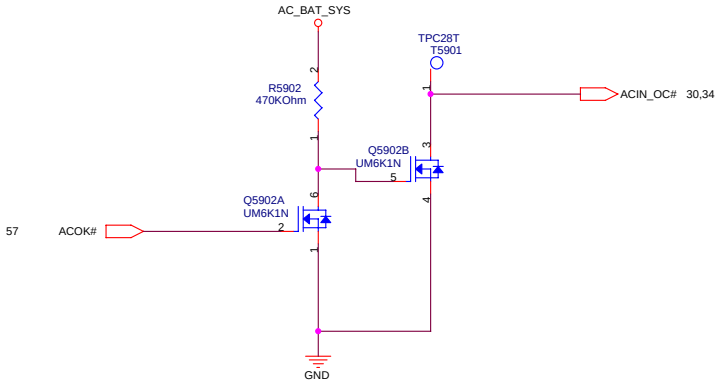
<Variant Name>

Title : POWER_PIC		
<OrgName>	Engineer: Charlse/Mia	
Size: Custom	Project Name: A6JC	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 58 of 63	

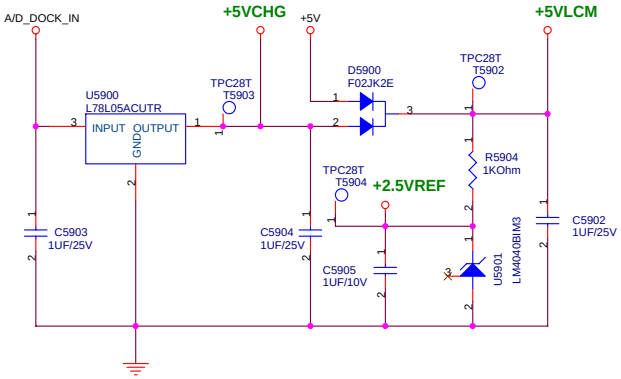
BATTERY IN DETECT



ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF



<Variant Name>

Title : POWER_DETECT

<OrgName>

Engineer: Charlse/Mia

Size	Project Name	Rev
Custom	A6JC	2.1

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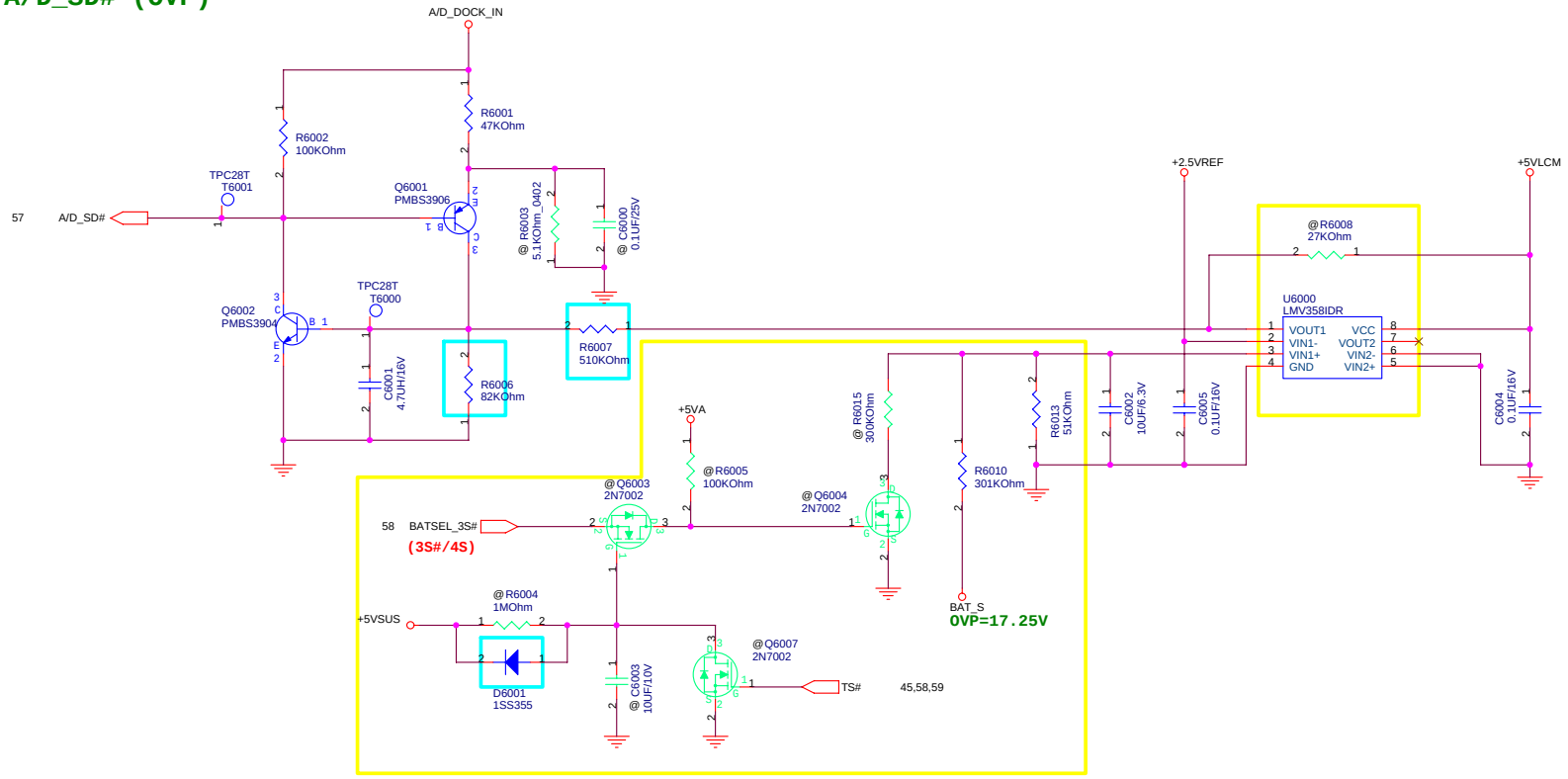
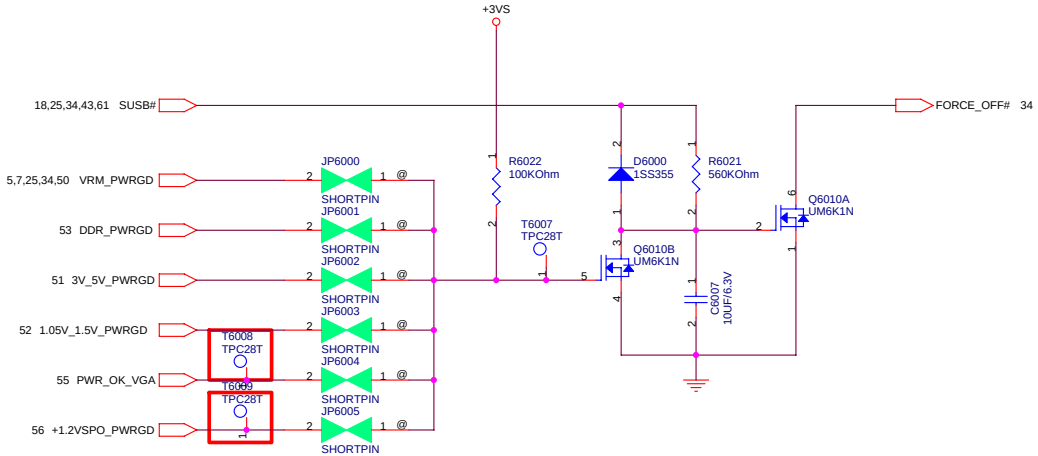
BATTERY A/D_SD# (OVP)



POWER GOOD DETECTER

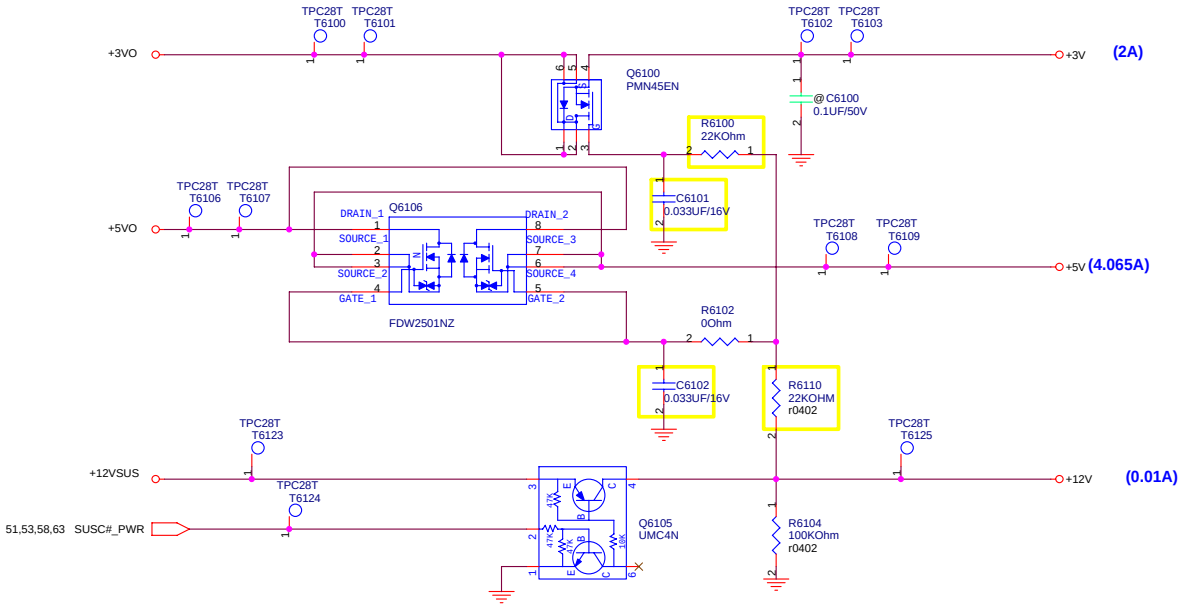


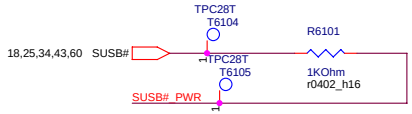
TPC28T T6002 1 VRM_PWRGD
TPC28T T6003 1 DDR_PWRGD
TPC28T T6004 1 3V_5V_PWRGD
TPC28T T6005 1 1.05V_1.5V_PWRGD

<Variant Name>

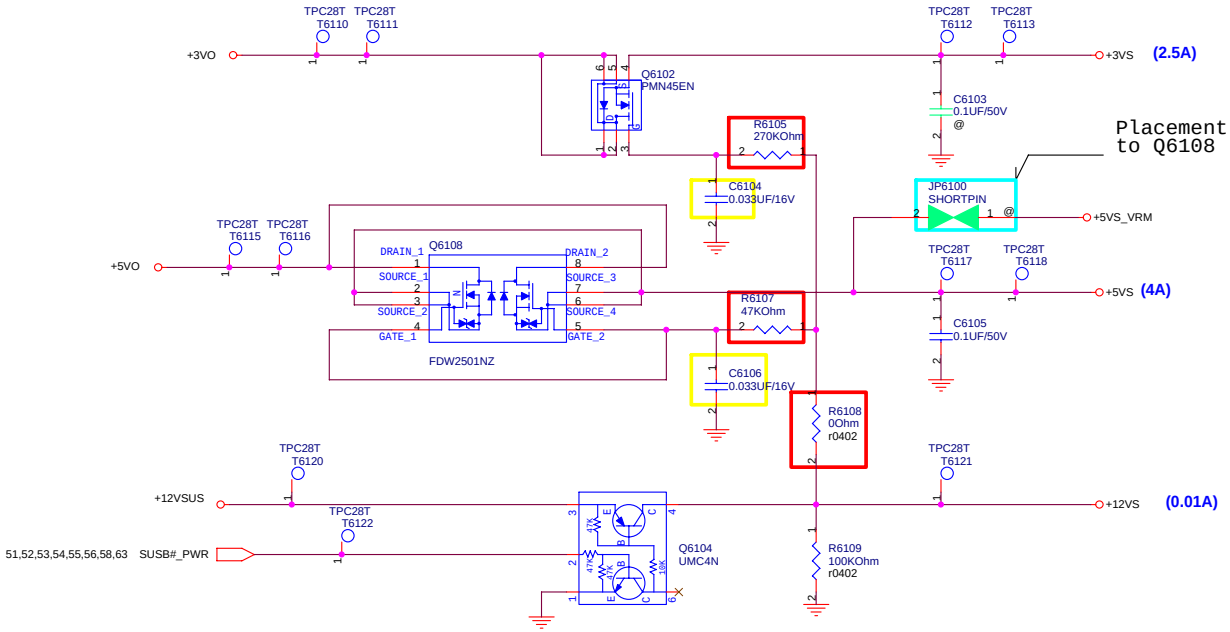
Title : POWER_PROTECT
<OrgName>
Engineer: Charlse/Mia
Size: Custom | Project Name: A6JC | Rev: 2.1
Date: Thursday, January 19, 2006 | Sheet 60 of 63

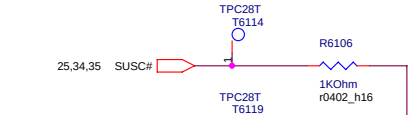
SUSC#_PWR POWER

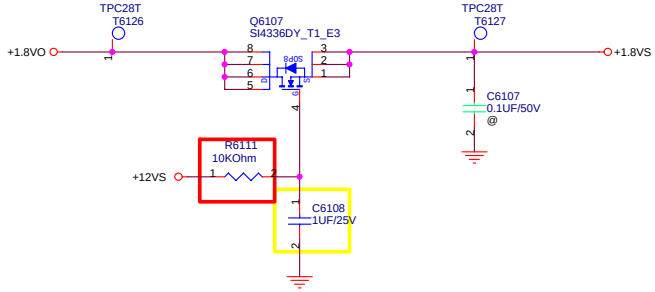




SUSB#_PWR POWER

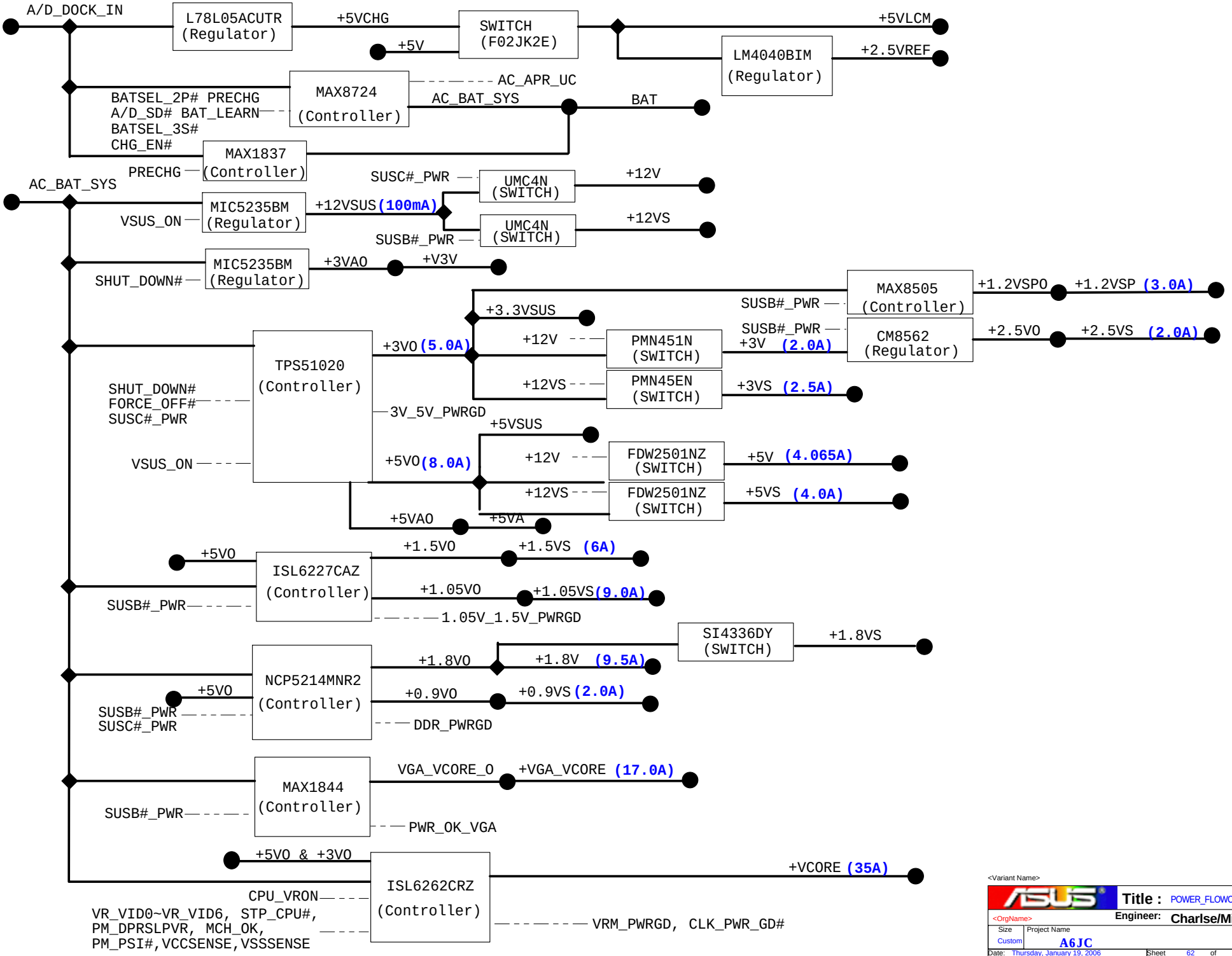






<Variant Name>

<OrgName>	Title : POWER_LOAD SWITCH	
	Engineer: Charlse/Mia	
Size: Custom	Project Name: A6JC	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 61 of 63	



<Variant Name>

Title : POWER_FLOWCHART

<OrgName>

Engineer: Charlse/Mia

Size	Project Name	Rev
Custom	A6JC	2.1

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AC_BAT_SYS → AC_BAT_SYS 50,51,52,53,54,55,57,59

+3VA → +3VA 18,23,34,35,43,54

+5VA → +5VA 34,51,57,60

+5VO → +5VO 51,52,53,55,61

+3VO → +3VO 51,52,56,61

+3V → +3V 25,30,31,32,35,36,37,38,41,42,43,44,54,61

+3VS → +3VS 4,5,7,9,11,12,16,17,18,19,20,21,25,26,27,28,30,31,33,34,35,36,39,42,43,44,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 4,28,35,40,43,61

+12VS → +12VS 18,19,35,61

+5V → +5V 18,30,35,37,40,43,59,61

+5VS → +5VS 4,19,22,26,27,30,33,35,41,43,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 9,15,16,19,35,54

+1.8VO → +1.8VO 53,61

+1.8V → +1.8V 7,10,20,21,35,53

+1.8VS → +1.8VS 13,14,15,16,22,35,61

+0.9VS → +0.9VS 14,15,22,35,46,53

BAT → BAT 57

+5VCHG → +5VCHG 57,59

+5VLCM → +5VLCM 30,43,57,58,59,60

+2.5VREF → +2.5VREF 54,57,59,60

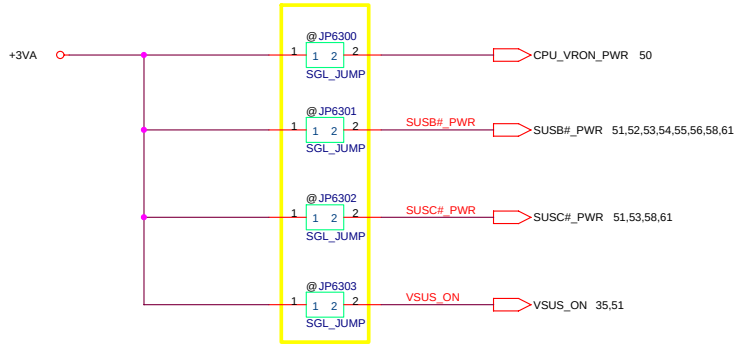
+VCORE → +VCORE 3,4,50

+VGA_VCORE → +VGA_VCORE 12,55

+1.2VSP → +1.2VSP 12,13,14,35,56

BAT_CON → BAT_CON 45,57

FOR POWER TEST



<Variant Name>

Title : POWER_SIGNAL

<OrgName> Engineer: Charlse/Mia

Size	Project Name	Rev
Custom	A6JC	2.1

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