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N68SC-M3S

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AM3 & MCP68S

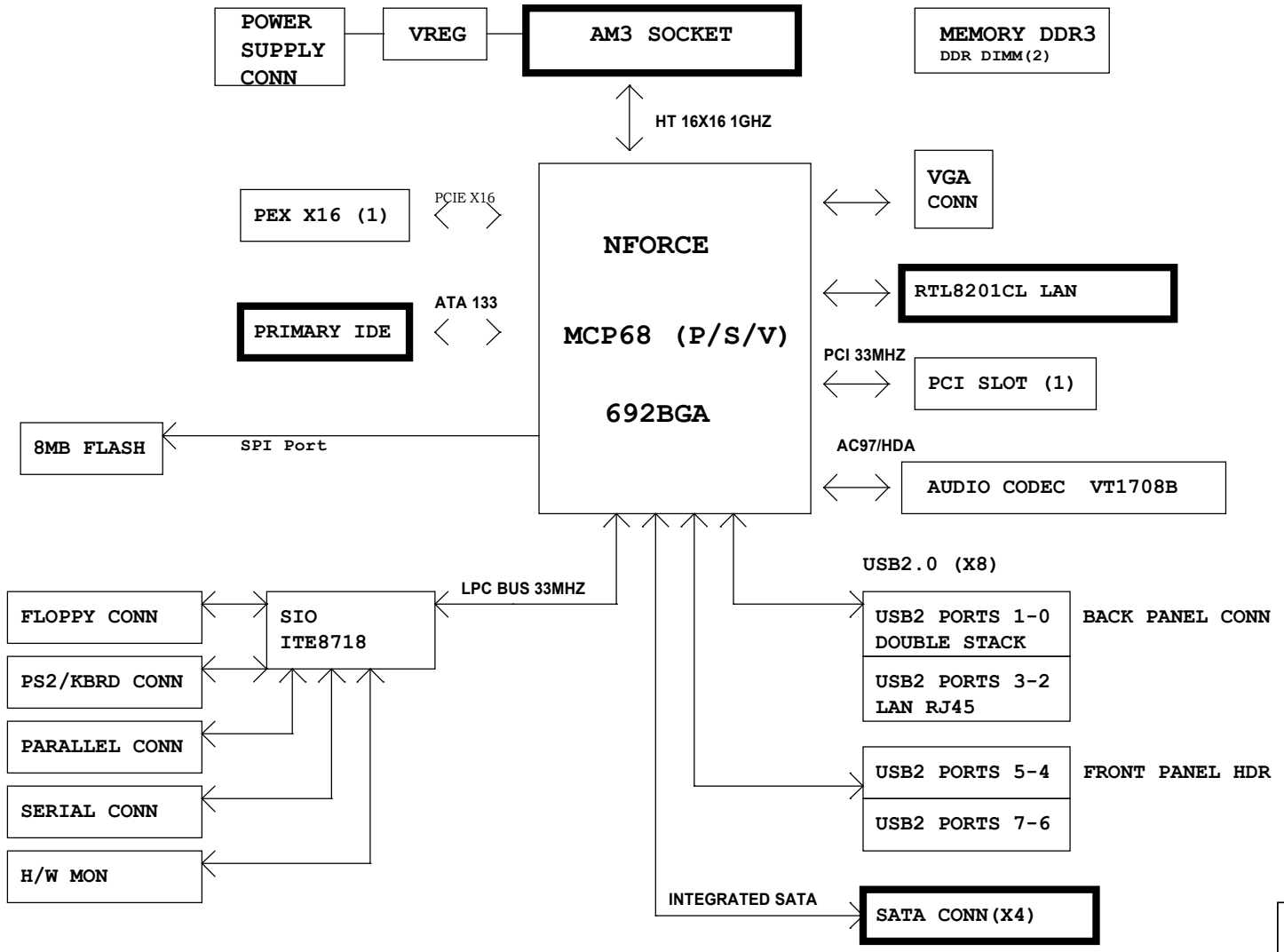
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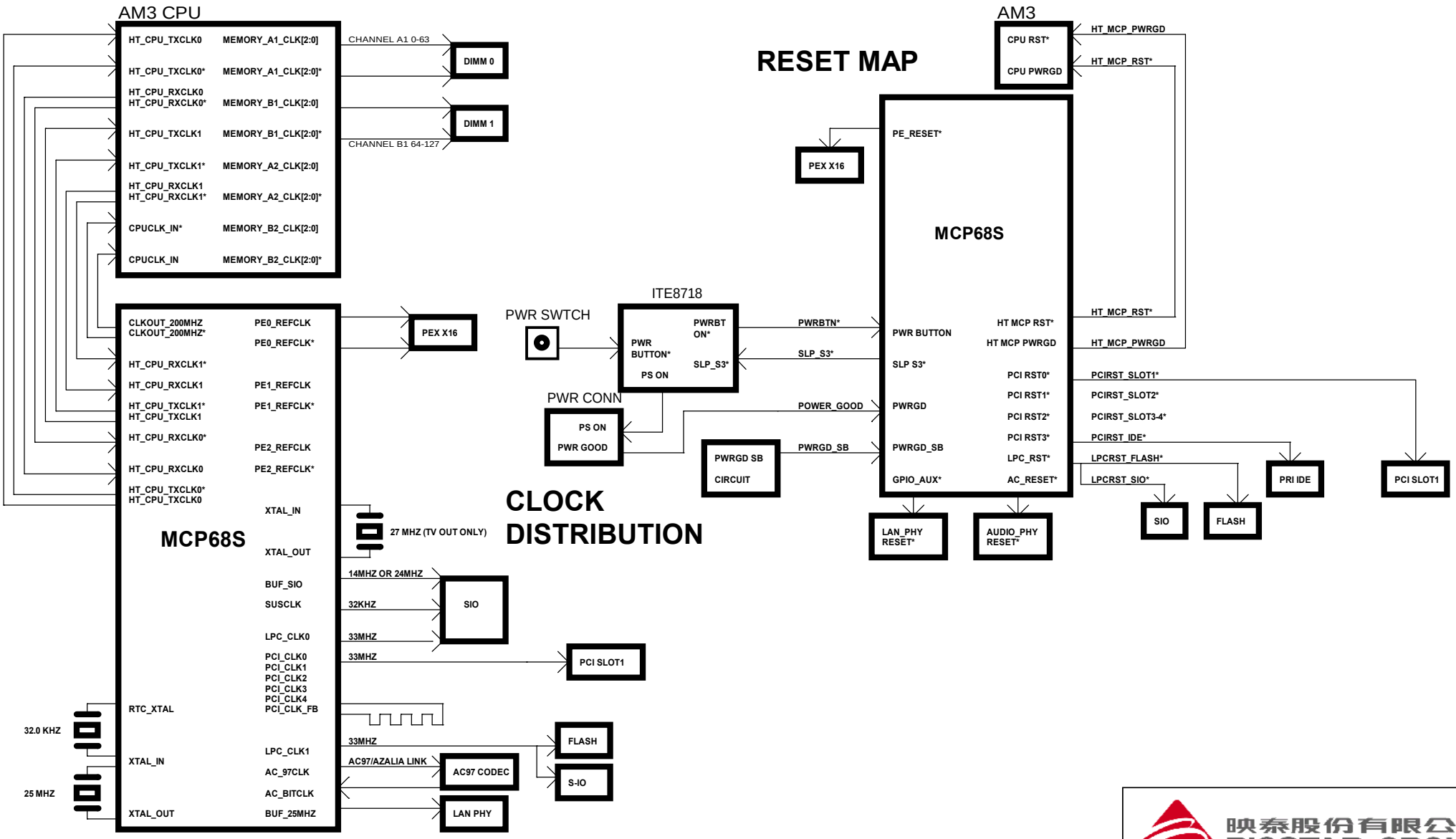
Title: COVER SHEET		
Size: B	Document Number: N68SC-M3S	Rev: 6.1
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N68SC-M3S Block Diagram



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Title	SYSTEM BLOCK	
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Title	RESET&CLOCK MAP	
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CPU VID TABLE

VID [4..0]	VDD	VID [4..0]	VDD
0X00000	1.550V	0X10000	1.150V
0X00001	1.525V	0X10001	1.125V
0X00010	1.500V	0X10010	1.100V
0X00011	1.475V	0X10011	1.075V
0X00100	1.450V	0X10100	1.050V
0X00101	1.425V	0X10101	1.025V
0X00110	1.400V	0X10110	1.000V
0X00111	1.375V	0X10111	0.975V
0X01000	1.350V	0X11000	0.950V
0X01001	1.325V	0X11001	0.925V
0X01010	1.300V	0X11010	0.900V
0X01011	1.275V	0X11011	0.875V
0X01100	1.250V	0X11100	0.850V
0X01101	1.225V	0X11101	0.825V
0X01110	1.200V	0X11110	0.800V
0X01111	1.175V	0X11111	OFF

SMBUS ADDRESS MAP

DEVICE	SMBUS #	ADDRESS
SLOT		
DIMM 0	0	1010 000 = 0X50
DIMM 1	0	1010 001 = 0X51
DIMM 2	0	1010 010 = 0X52
DIMM 3	0	1010 011 = 0X53
SIO	1	0101 101 = 0X2D
PCI SLOT 1	1	ARP
PCI SLOT 2	1	ARP
PCI SLOT 3	1	ARP
PCI SLOT 4	1	ARP
DDC BUS	A	?
DDC BUS	B	?

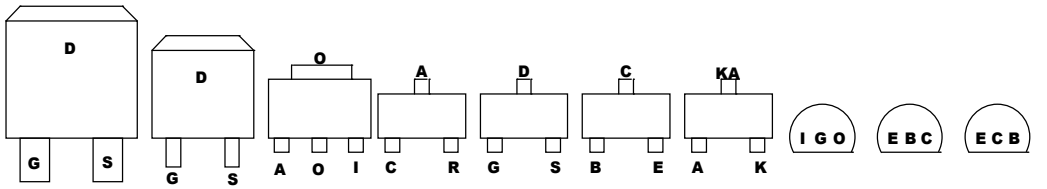
22U/25DE	5*7 mm
100U/16DE	6.3*11 mm
220U/10DE	6.3*11 mm
470U/16DE	8*11 mm
1000U/10DE	8*14 mm
1500U/16DE	10*25 mm
3300U/25DE	10*25 mm

PCI INTERRUPT/IDSEL MAP

BACK PANEL SLOT	PCI BUS#	DEVICE#	IDSEL PIN	PCI SLOT INTA*	PCI SLOT INTB*	PCI SLOT INTC*	PCI SLOT INTD*	REQ/GNT
1	01	0X05	22	P_INTY*	P_INTZ*	P_INTW*	P_INTX*	1/1
2	01	0X06	24	P_INTW*	P_INTX*	P_INTY*	P_INTZ*	2/2
3	01	0X07						
4	01	0X08						
5	01	0X09						
6	01	0X0A						

PCI DEVICE MAP

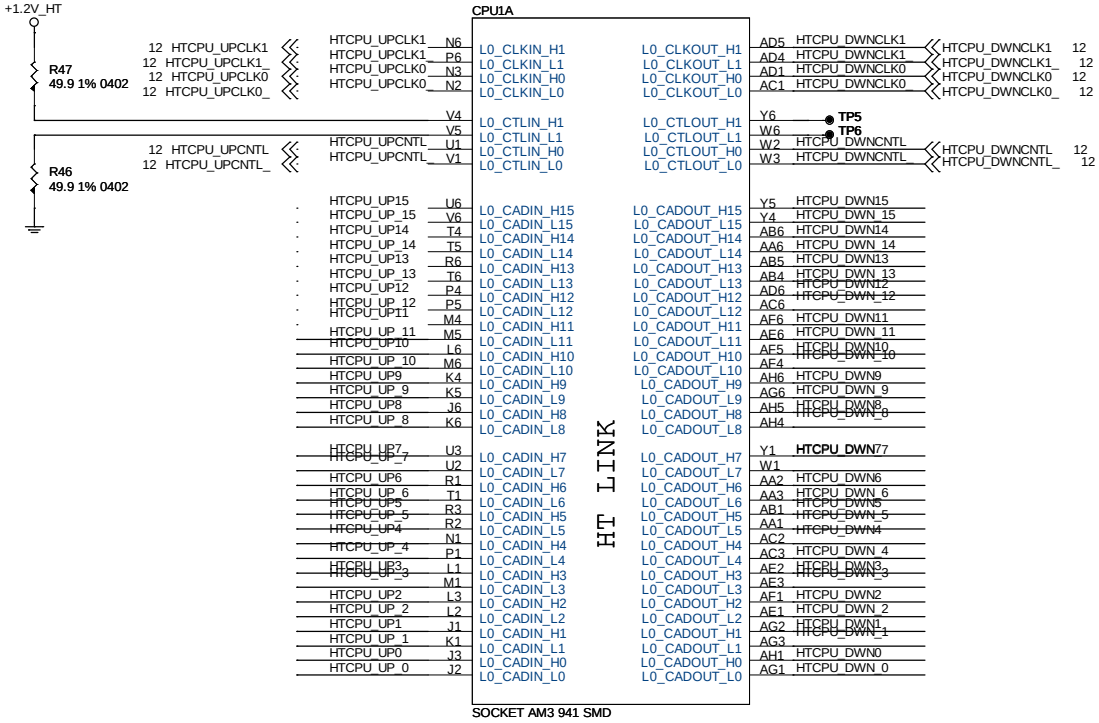
DEVICE	PCI BUS#	FUNCTION	IDSEL PIN	DEVICE ID
MCP61P	MCP61 LOGICAL PCI BUS 0	0X01-0X0F	--	--
MAC /MAC	0	XA	0	0X56/57
PCI-PCI BRIDGE	0	X9	0	0X005C
SATA1	0	X8	0	0X0055
SATA0	0	X8	0	0X0054
IDE	0	X6	0	0X0053
MODEM CODEC	0	X4	1	0X0058
AUDIO CODEC	0	X4	0	0X0059
USB 2.0	0	X2	1	0X005B
USB 1.1	0	X2	0	0X005A
SHAPE TRIM	0	X1	2	0X005F
LDT	0	X0	0	0X005E
SMBUS2	0	X1	1	0X0052
LEGACY SLAVE	0	?	?	0X00D3
LPC	0	X1	0	0X0050/51
LOGICAL PCI BUS	1	?	?	?
PCI SLOT 1				
PCI SLOT 2				
PCI SLOT 3				
PCI SLOT 4				
PCI SLOT 5				



TO-263	TO-252	SOT-223	SOT-23	SOT-23	SOT-23	SOT-23	TO-92	TO-92	TO-92
PHB55N03 90N02	20N03 TM3055TL-S PHD55N03	AMS1117	LM431	2N7002 SI2303S SI2301S	2N3904 2N3906 MMBT2907A 2N2222A	BAT54C BAT54S	LM431 78L05-D LM432	2N2222A 2N2097A	HSD882-D

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Title: SPEC&CHANGE LIST		
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12 HTCPU_UP[15..0] HTCPU_UP[15..0]

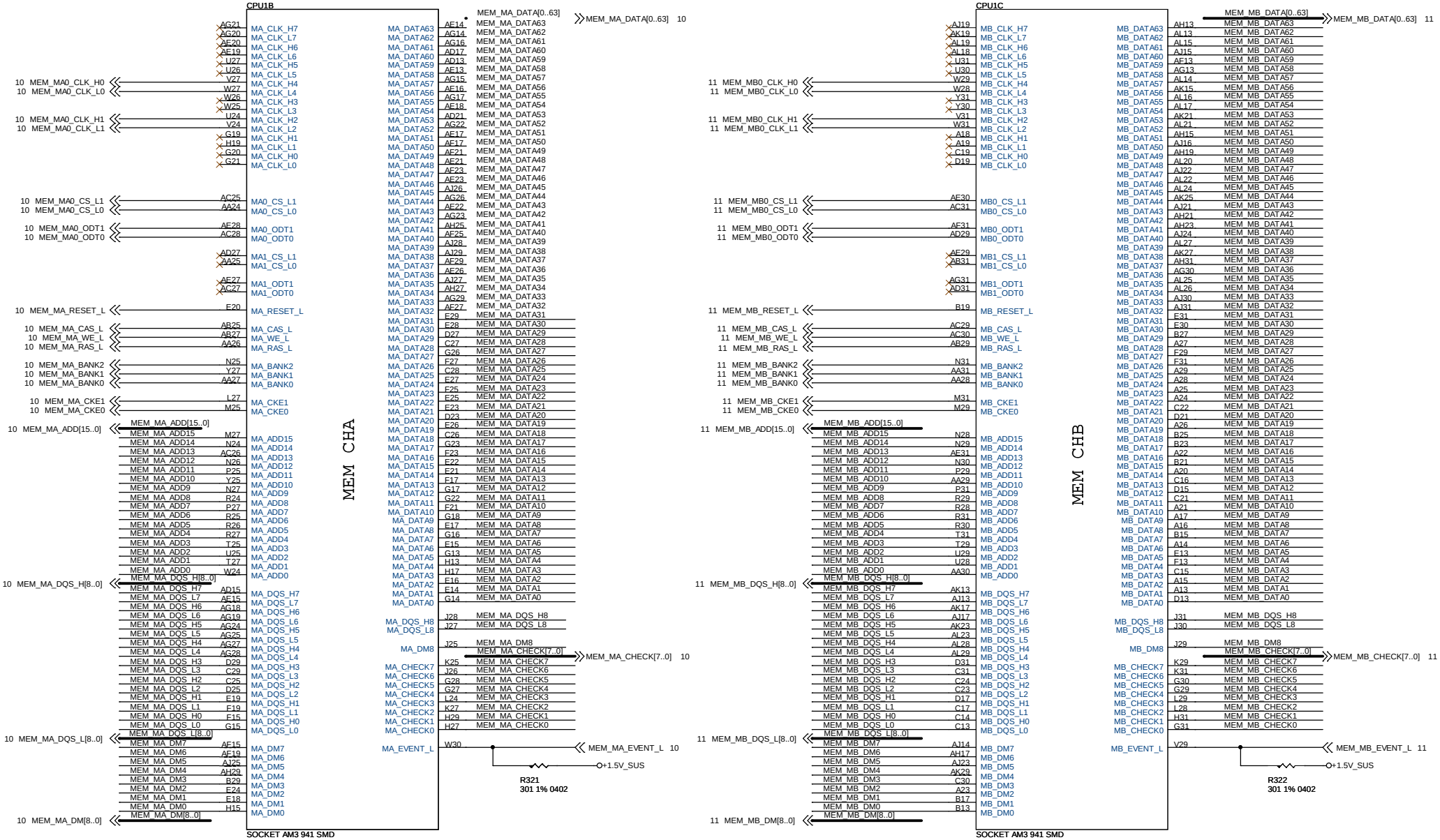
12 HTCPU_UP_[15..0] HTCPU_UP_[15..0]

HTCPU_DWN[15..0] HTCPU_DWN[15..0] 12

HTCPU_DWN_[15..0] HTCPU_DWN_[15..0] 12

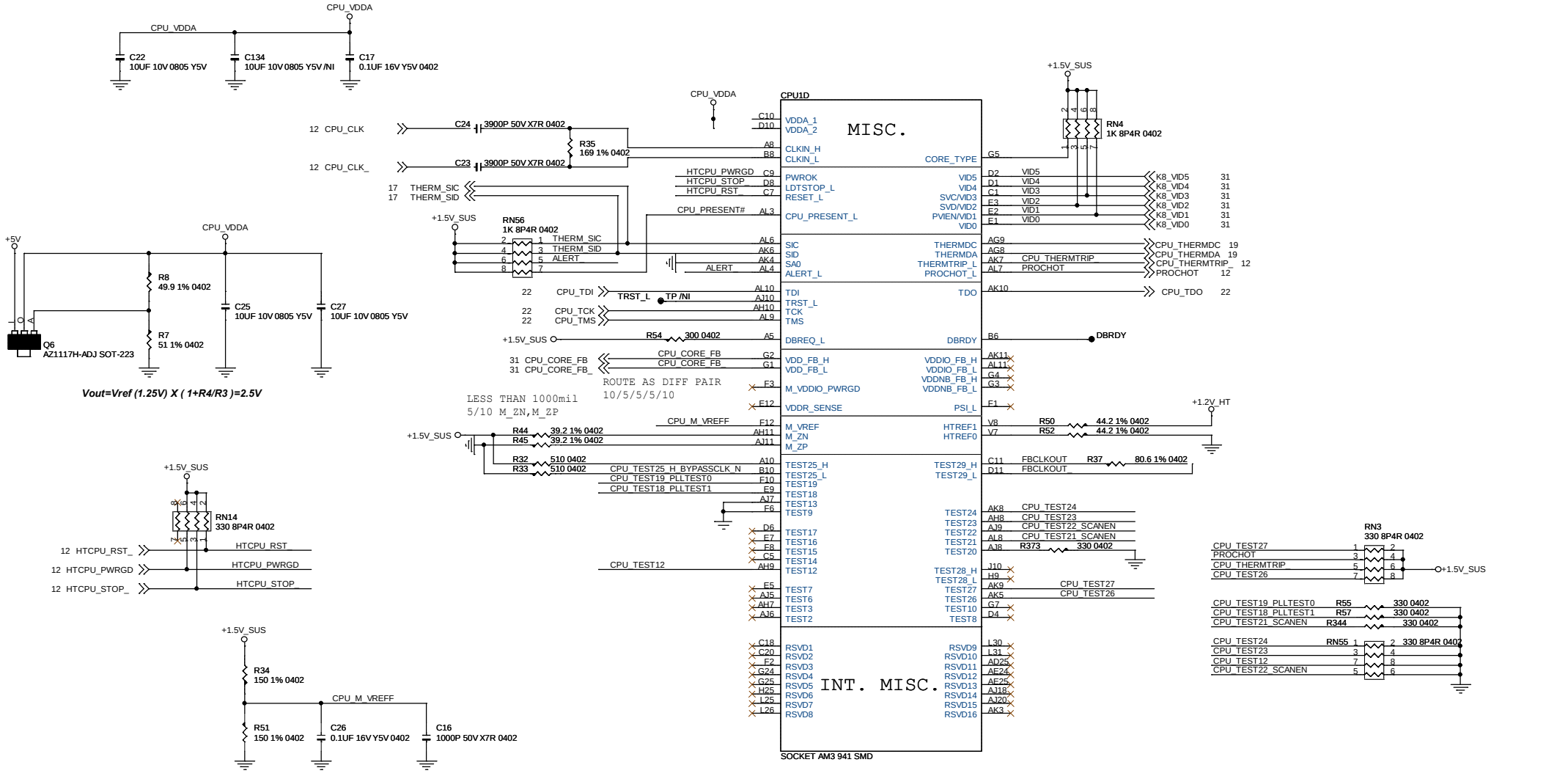
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Title: M2 HT/DDR 0-63		
Size: B	Document Number: N68SC-M3S	Rev: 6.1
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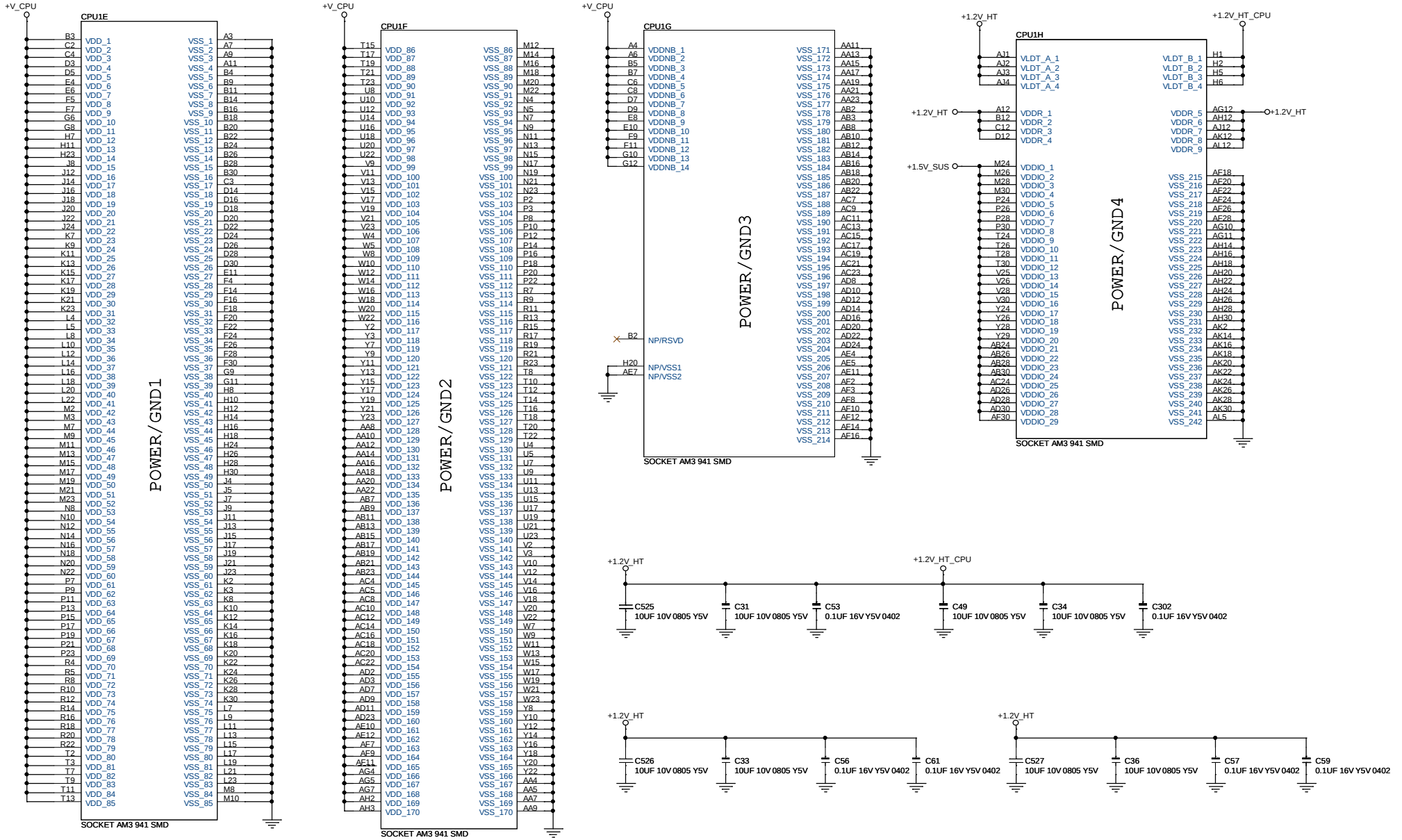
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Title	M2 DDR 64-127	
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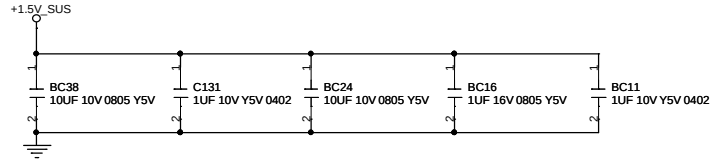
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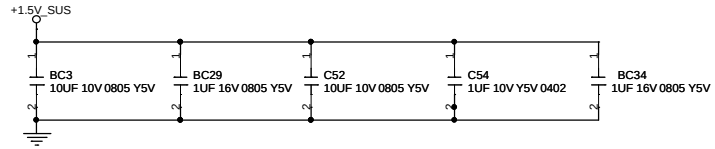
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Size: Custom	Document Number: N68SC-M3S	Rev: 6.1
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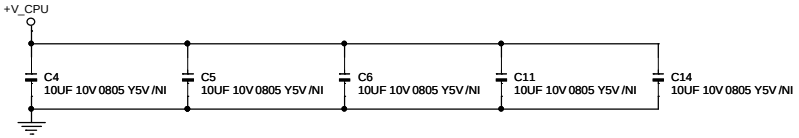


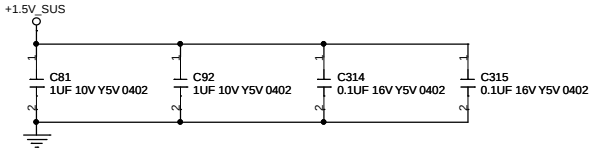
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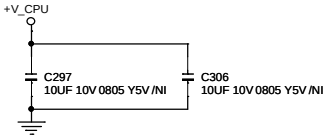
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Size: Custom	Document Number: N68SC-M3S	Rev: 6.1
Date: Monday, November 08, 2010	Sheet 8 of 36	

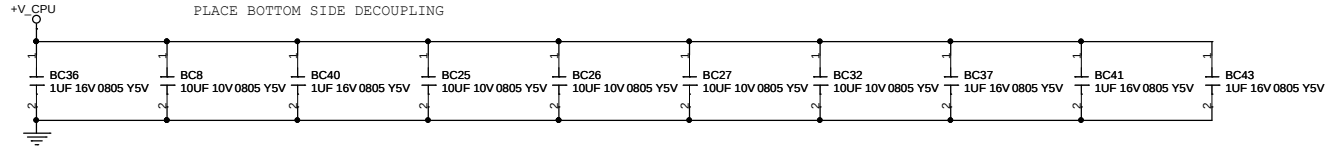


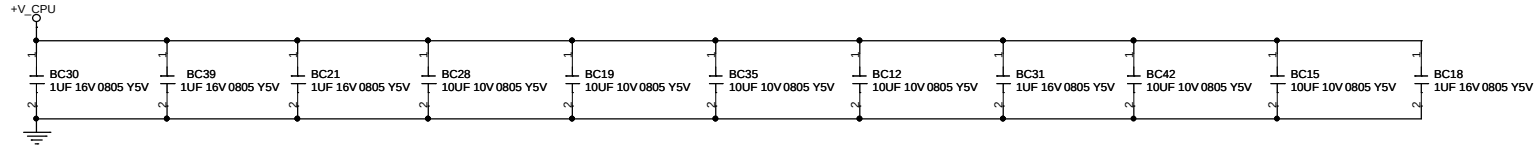


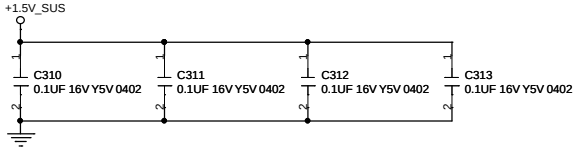








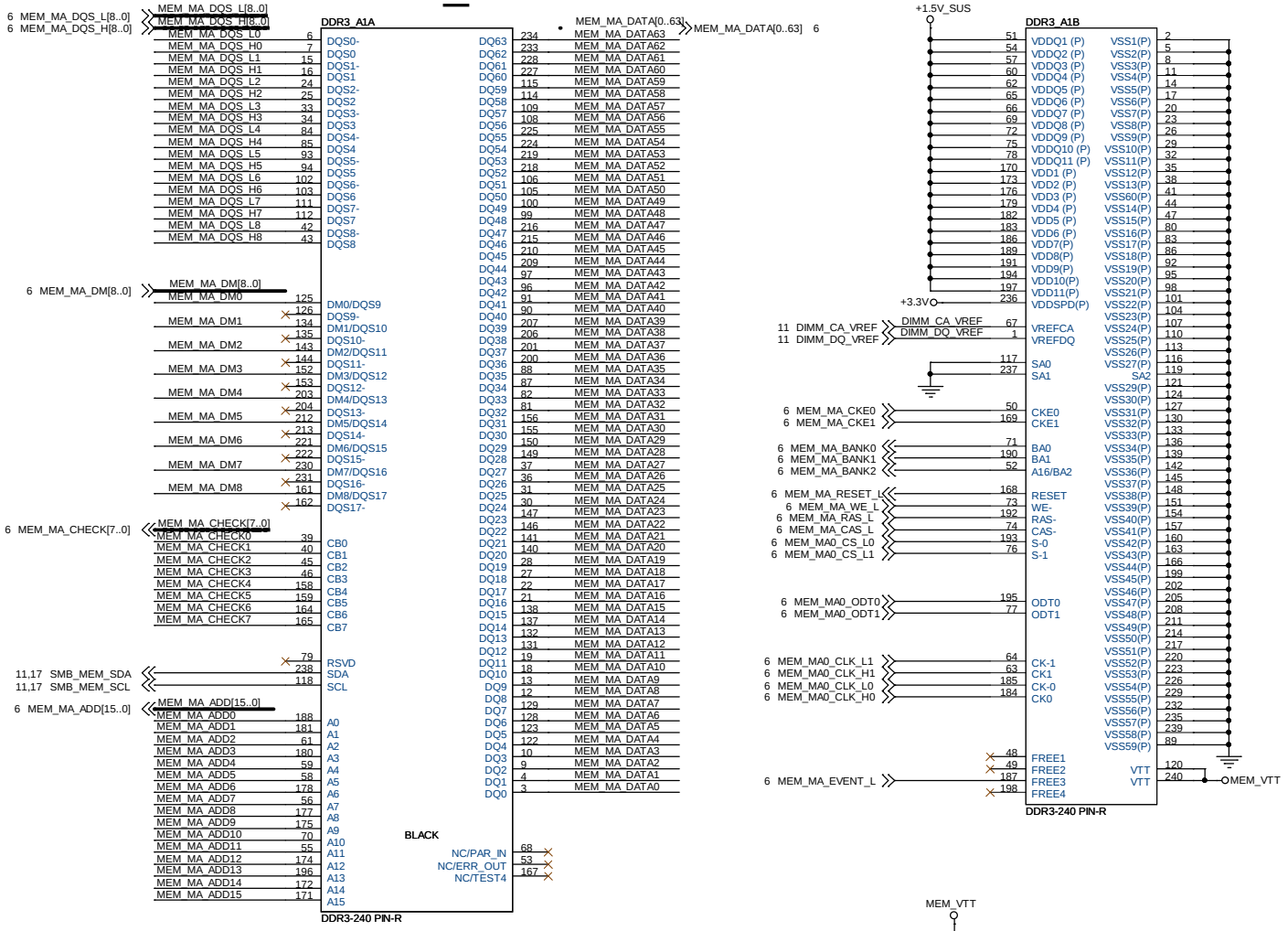


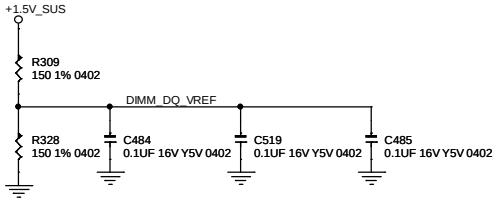


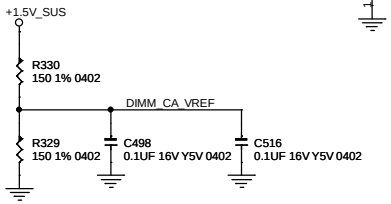
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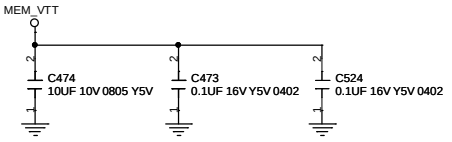
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DDR3_A1





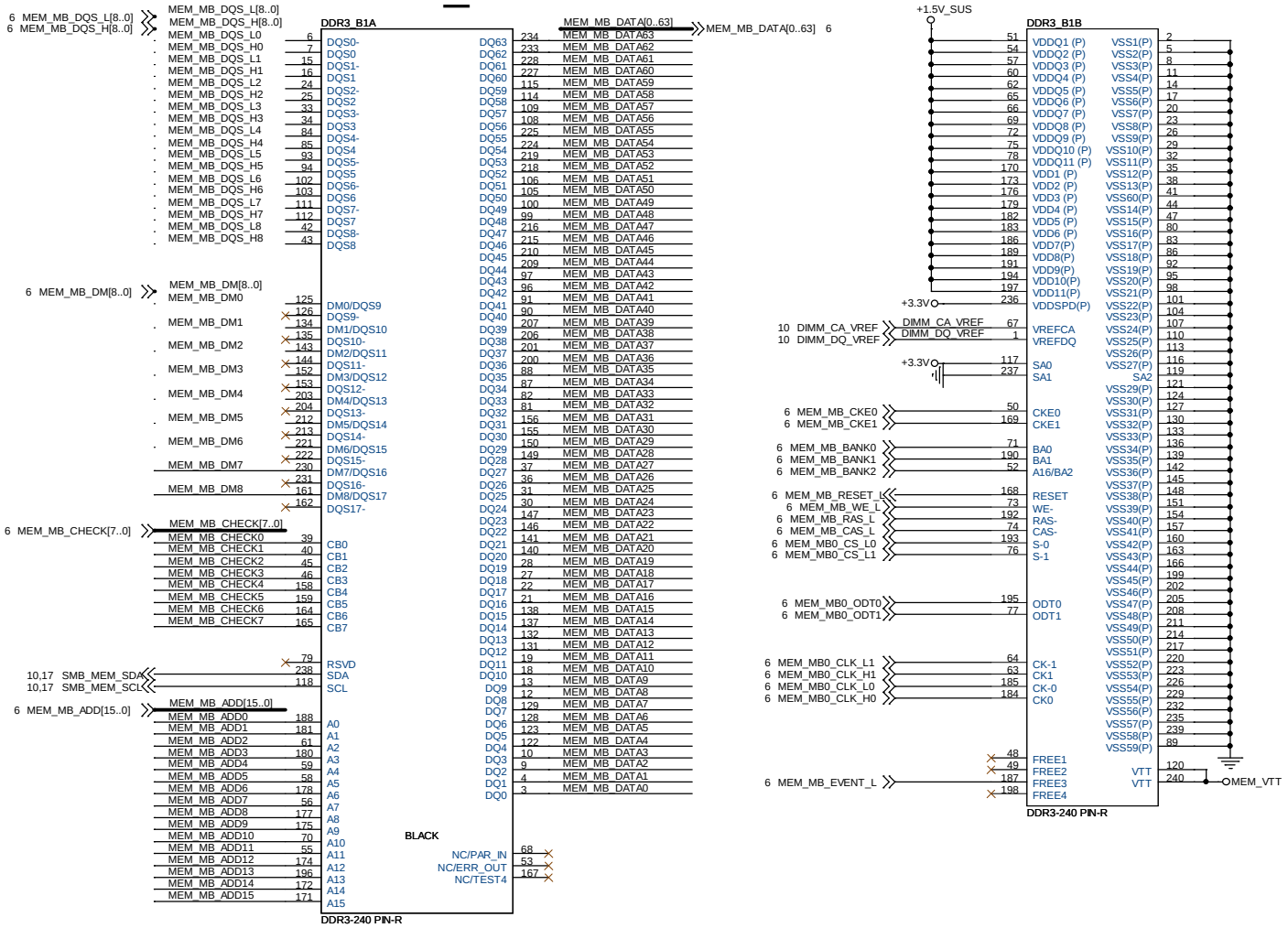




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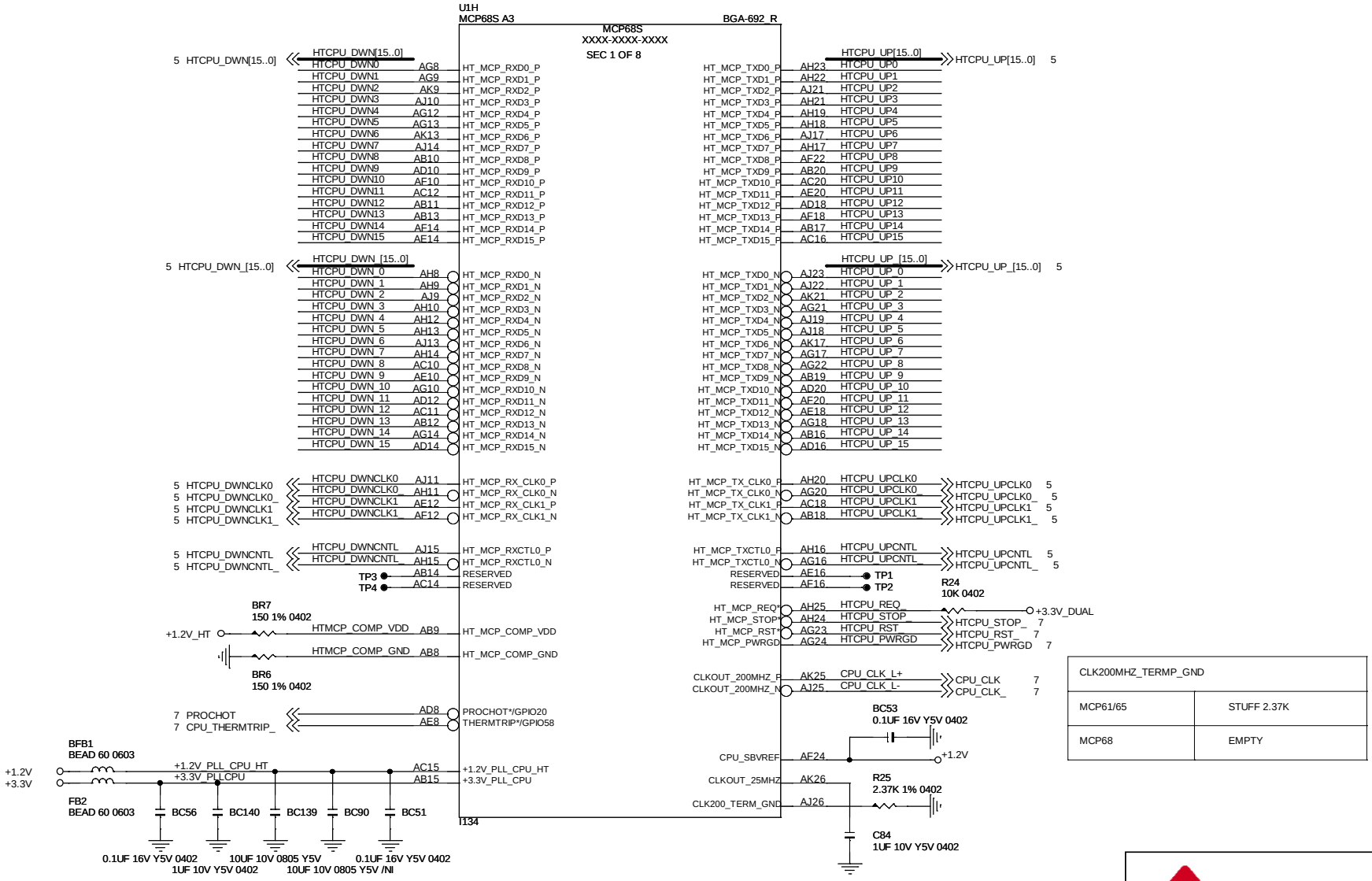
Title	DDR DIMMA1	
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DDR3_B1



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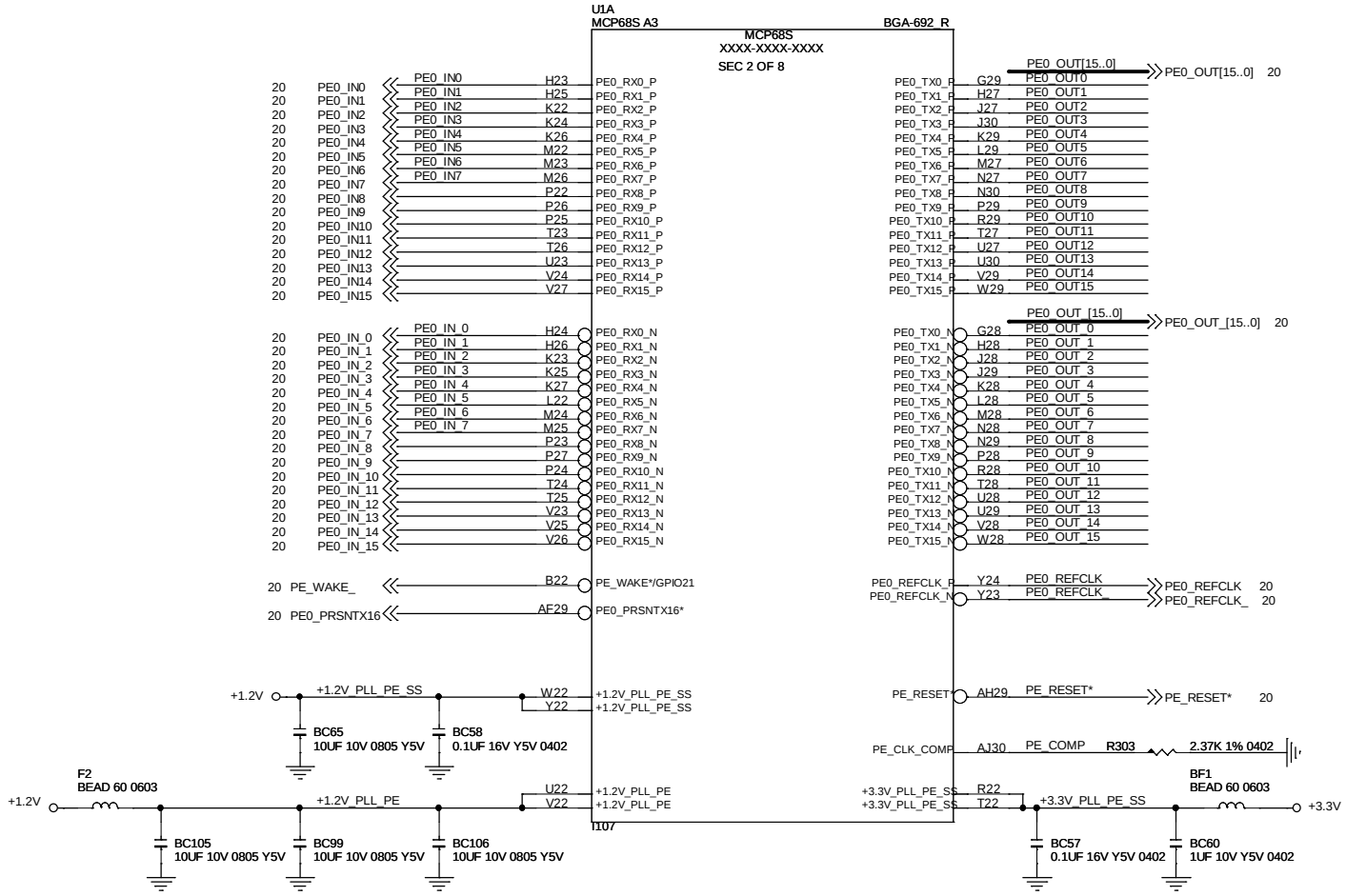
Title	DDR DIMMB1	
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CLK200MHZ_TERMP_GND	
MCP61/65	STUFF 2.37K
MCP68	EMPTY

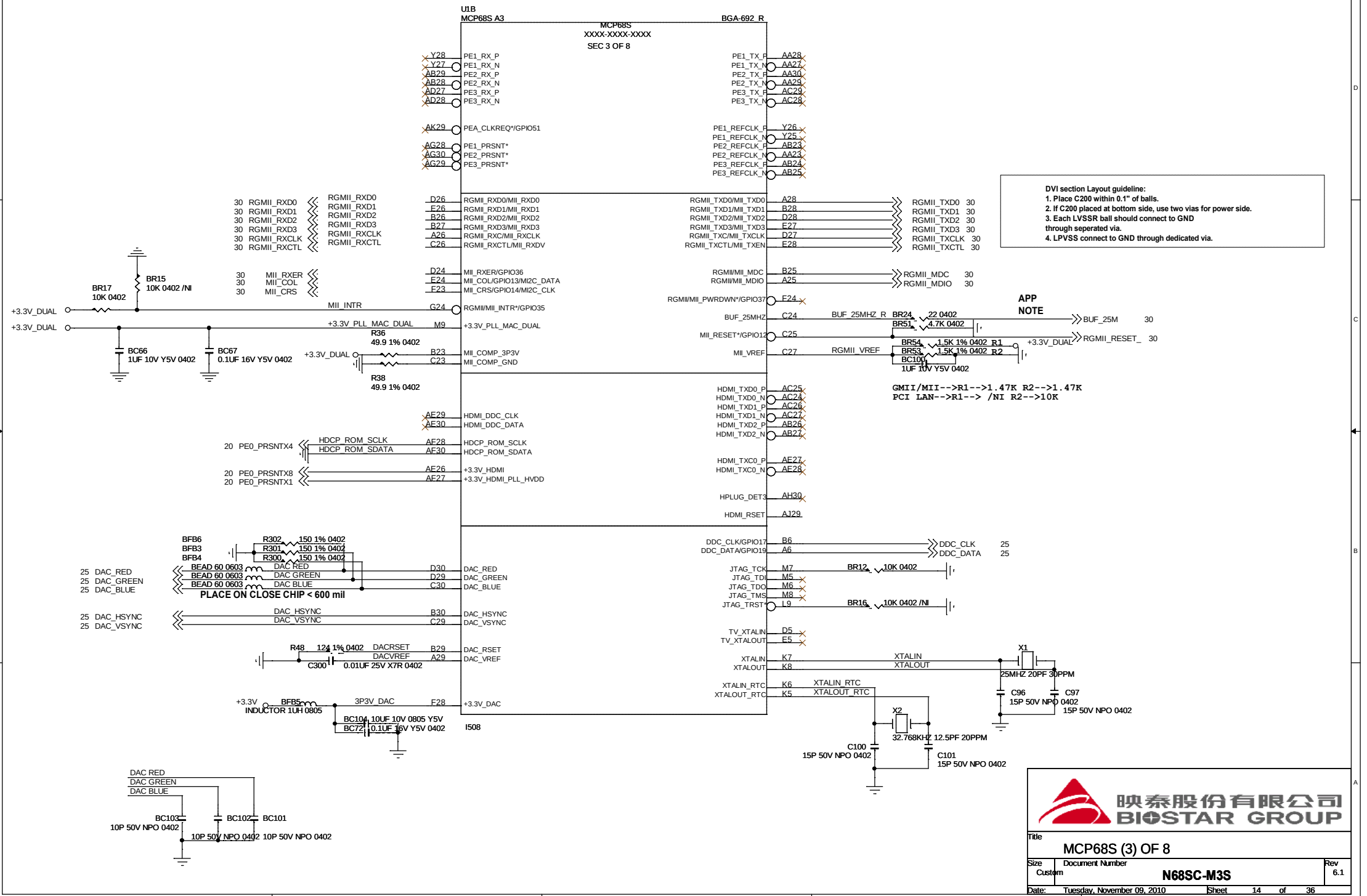
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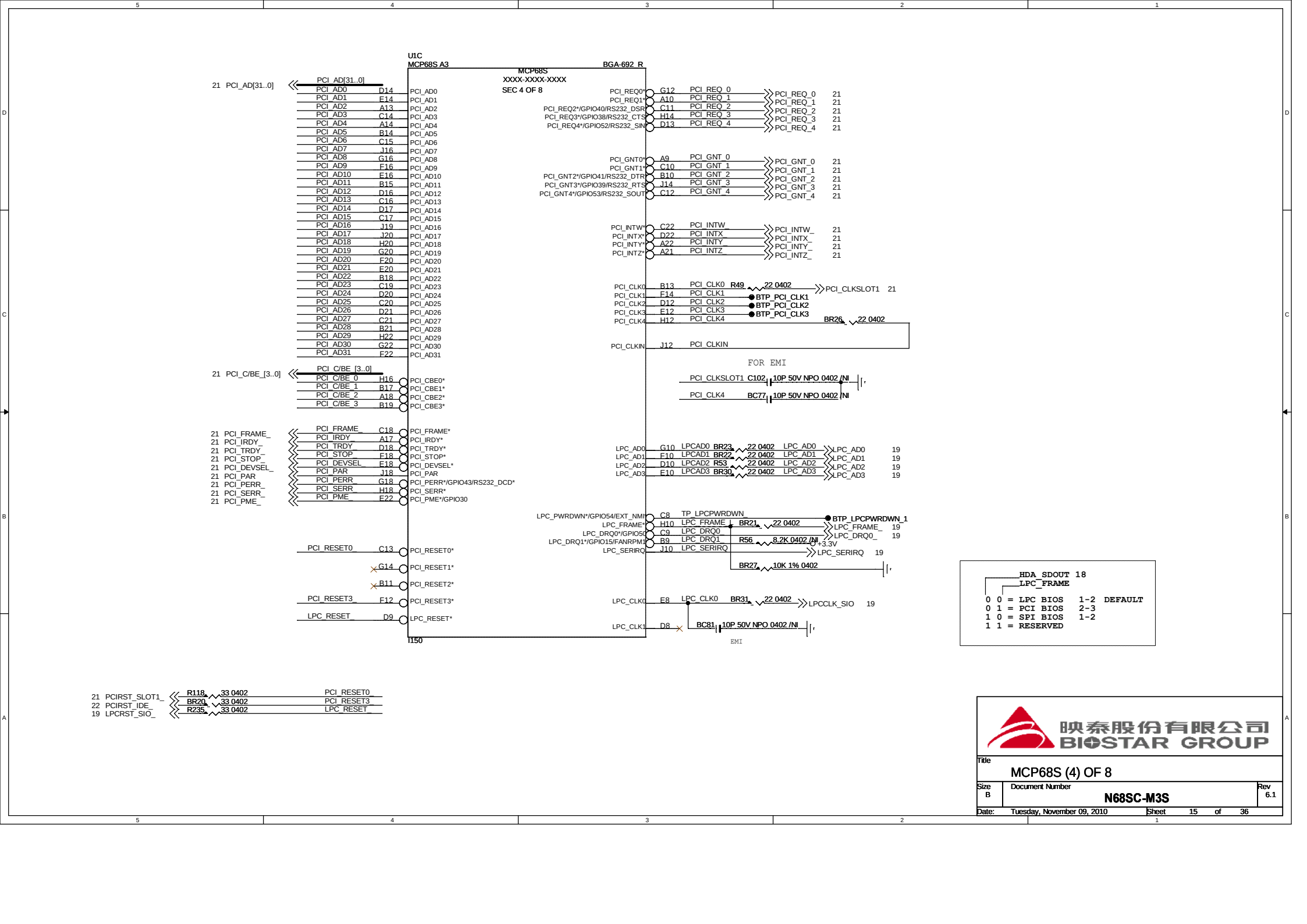
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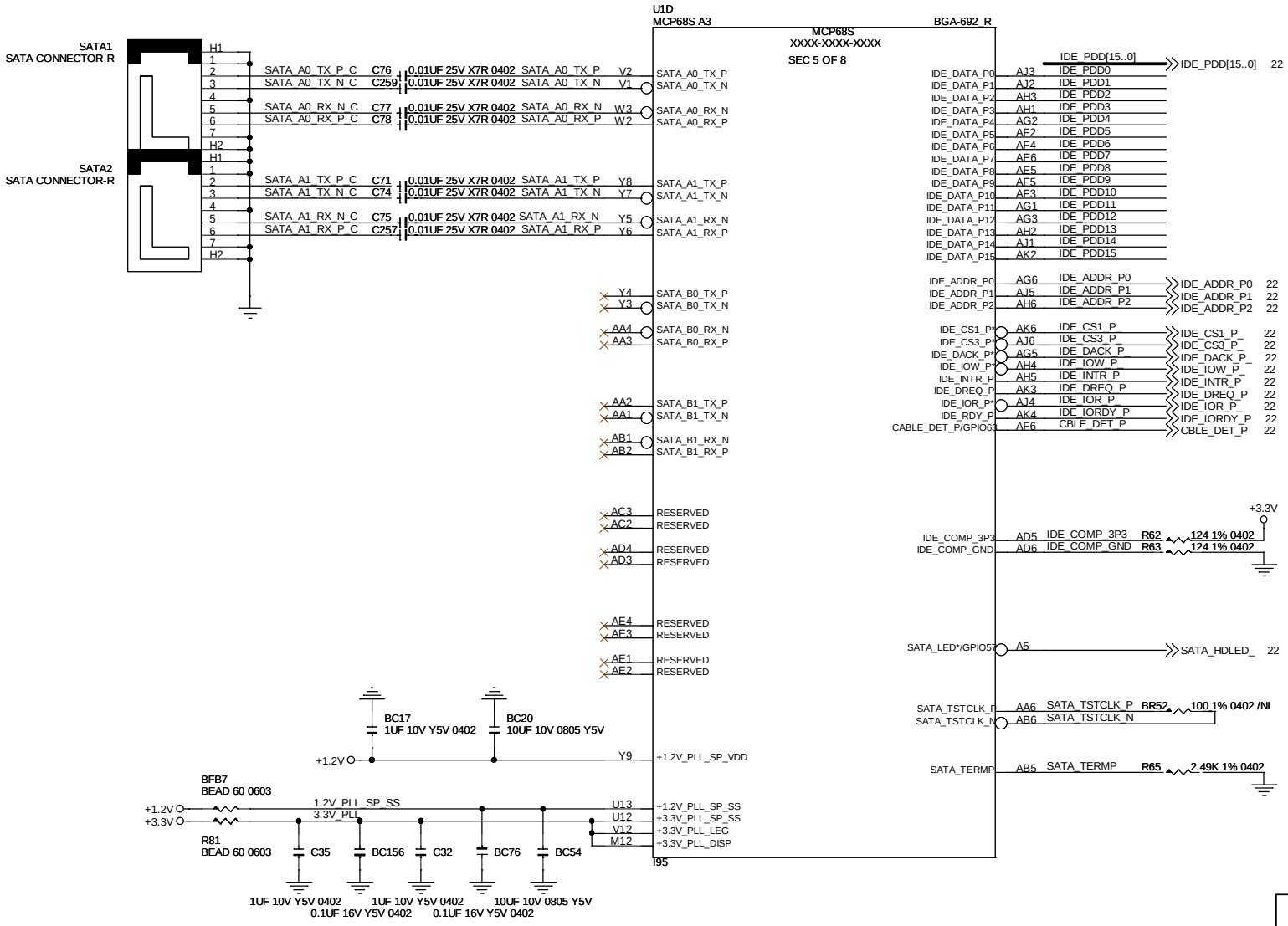
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U1B
MCP68S A3
MCP68S
XXXX-XXXX-XXXX
SEC 3 OF 8
BGA-692_R
PE1_RX_P
PE1_RX_N
PE2_RX_P
PE2_RX_N
PE3_RX_P
PE3_RX_N
PEA_CLKREQ*/GPIO51
PE1_PRSNT*
PE2_PRSNT*
PE3_PRSNT*
PE1_TX_P
PE1_TX_N
PE2_TX_P
PE2_TX_N
PE3_TX_P
PE3_TX_N
PE1_REFCLK_P
PE1_REFCLK_N
PE2_REFCLK_P
PE2_REFCLK_N
PE3_REFCLK_P
PE3_REFCLK_N
RGMII_RXD0/MII_RXD0
RGMII_RXD1/MII_RXD1
RGMII_RXD2/MII_RXD2
RGMII_RXD3/MII_RXD3
RGMII_RXC/MII_RXCLK
RGMII_RXCTL/MII_RXDV
RGMII_TXD0/MII_TXD0
RGMII_TXD1/MII_TXD1
RGMII_TXD2/MII_TXD2
RGMII_TXD3/MII_TXD3
RGMII_TXC/MII_TXCLK
RGMII_TXCTL/MII_TXEN
MII_RXER/GPIO36
MII_COL/GPIO13/MI2C_DATA
MII_CRS/GPIO14/MI2C_CLK
RGMII/MII_MDC
RGMII/MII_MDIO
RGMII/MII_PWRDWN*/GPIO37
RGMII/MII_INTR*/GPIO35
BUF_25MHZ
MII_RESET*/GPIO12
MII_VREF
MII_COMP_3P3V
MII_COMP_GND
HDMI_TXD0_P
HDMI_TXD0_N
HDMI_TXD1_P
HDMI_TXD1_N
HDMI_TXD2_P
HDMI_TXD2_N
HDMI_TXC0_P
HDMI_TXC0_N
HPLUG_DET3
HDMI_RSET
HDMI_DDC_CLK
HDMI_DDC_DATA
HDCP_ROM_SCLK
HDCP_ROM_SDATA
+3.3V_HDMI
+3.3V_HDMI_PLL_HVDD
DDC_CLK/GPIO17
DDC_DATA/GPIO19
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST*
TV_XTALIN
TV_XTALOUT
XTALIN
XTALOUT
XTALIN_RTC
XTALOUT_RTC
DAC_RED
DAC_GREEN
DAC_BLUE
DAC_HSYNC
DAC_VSYNC
DACRSET
DACVREF
DAC_RSET
DAC_VREF
3P3V_DAC
+3.3V_DAC
I508
DVI section Layout guideline:
1. Place C200 within 0.1" of balls.
2. If C200 placed at bottom side, use two vias for power side.
3. Each LVSSR ball should connect to GND through seperated via.
4. LPVSS connect to GND through dedicated via.
APP NOTE
GMII/MII-->R1-->1.47K R2-->1.47K
PCI LAN-->R1--> /NI R2-->10K
PLACE ON CLOSE CHIP < 600 mil
BR15 10K 0402 /NI
BR17 10K 0402
BR36 49.9 1% 0402
BR38 49.9 1% 0402
BR24 22 0402
BR51 4.7K 0402
BR54 1.5K 1% 0402 R1
BR53 1.5K 1% 0402 R2
BC100 1UF 10V Y5V 0402
BR12 10K 0402
BR16 10K 0402 /NI
BC66 1UF 10V Y5V 0402
BC67 0.1UF 16V Y5V 0402
R302 150 1% 0402
R301 150 1% 0402
R300 150 1% 0402
BEAD 60 0603
R48 124 1% 0402
C300 0.01UF 25V X7R 0402
BFB5 INDUCTOR 1UH 0805
BC104 10UF 10V 0805 Y5V
BC72 0.1UF 16V Y5V 0402
X1 25MHZ 20PF 30PPM
X2 32.768KHZ 12.5PF 20PPM
C96 15P 50V NPO 0402
C97 15P 50V NPO 0402
C100 15P 50V NPO 0402
C101 15P 50V NPO 0402
BC103 10P 50V NPO 0402
BC102 10P 50V NPO 0402
BC101 10P 50V NPO 0402
+3.3V_DUAL
+3.3V_PLL_MAC_DUAL
BUF_25M
RGMII_RESET_
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BOARDID TABLE: CRB STYLE

+3.3V_DUAL
R67 10K 1% 0402
AC_SDOUT
C86 10P 50V NPO 0402

HDA_SDOUT
LPC_FRAME 16
0 0 = LPC BIOS 1-2 DEFAULT
0 1 = PCI BIOS 2-3
1 0 = SPI BIOS 1-2
1 1 = RESERVED

+3.3V_DUAL
R205 10K 1% 0402 /NI
AC_RST_
R30 10K 1% 0402
C69 10P 50V NPO 0402

AC_RST*
1 = *RGMII OR PCI LAN
0 = MII

U1E
MCP68S A3
MCP68S
XXXX-XXXX-XXXX
SEC 6 OF 8
BGA-692_R

28 AC_BITCLK — AC_BITCLK — B7 GP_REFCLK; B4 HDA_BCLK
28 AC_SDOUT — A3 HDA_SDATA_OUT0/GPIO45
28 AC_SDIN_0 — A2 HDA_SDATA_IN0/GPIO22; B1 HDA_SDATA_IN1/GPIO23/MGPIO0; B2 HDA_SDATA_IN2/GPIO24

+3.3V
R190 10K 1% 0402
AC_SYNC
R29 10K 1% 0402 /NI
R43 10K 1% 0402 /NI

SPDIF0
(CLK)
1 = 24MHZ
0 = *14.318MHZ

28 AC_RST_ — R77 22 0402 — C3 HDA_RESET*
28 AC_SYNC — R27 22 0402 — B3 HDA_SYNC/GPIO44

GPIO_WPJ — F2 GPIO_1
F1 GPIO_2/NMI*
F6 GPIO_3/SMI*
J8 GPIO_4/SCI_INTR*
G3 GPIO_5/INIT*
29 GPI — G5 GPIO_6/FERR*/SYS_FERR*
G6 GPIO_7/NFERR*/SYS_PERR*

+3.3V_DUAL — R75 10K 1% 0402 — BOARD_ID0
R74 10K 1% 0402 /NI — BOARD_ID1

SPI_MISO — D3 GPIO_8/SPI_DI
SPI_MOSI — D4 GPIO_9/SPI_DO
SPI_CS0B — E4 GPIO_10/SPI_CS
SPI_CLK — E3 GPIO_11/SPI_CLK

+3.3V_DUAL — R73 10K 1% 0402 — R76 10K 1% 0402 /NI — H9 RESERVED

+3.3V_DUAL
C80 0.1UF 16V Y5V 0402
R26 1K 0402
R78 1K 0402

U2
SPI_CS0B
SPI_CLK
SPI_MOSI
SPI_MISO
GPIO_WPJ
VDD CE# HOLD# SO SCK WP# SI Vss
SPI SOCKET 8PIN

CLEAR CMOS CONTROL

1-2	NORMAL
2-3	CLEAR CMOS

CMOS CLEAR JUMPER

MCP61 SPI CLK STRAP
SPI_DO / SPI_CLK
00 = 500KHZ
01 = 1.8MHZ
10 = 2.5MHZ
*11 = 25MHZ
*DEFAULT

R79 49.9K 1% 0402
+3.3V_VBAT — K4 RTC_RST*

34 MEM_VLD — J3 MEM_VLD
34 HT_VLD — H3 MCPVDD/HT_VLD
33 MCPVDD_EN — J4 MCPVDD/HT_EN
31 CPU_VLD — J1 CPU_VLD
31 CPUVDD_EN — J2 CPUVDD_EN

BR19 1K 1% 0402 — L8 PKG_TEST; J8 TEST_MODE_EN

I189

USB0_P M3 USB_0 — USB_0 26
USB0_N M4 USB_0 — USB_0_ 26
USB1_P N3 USB_1 — USB_1 26
USB1_N N4 USB_1 — USB_1_ 26
USB2_P N1 USB_2 — USB_2 26
USB2_N N2 USB_2 — USB_2_ 26
USB3_P P1 USB_3 — USB_3 26
USB3_N P2 USB_3 — USB_3_ 26
USB4_P R2 USB_4 — USB_4 26
USB4_N R3 USB_4 — USB_4_ 26
USB5_P P3 USB_5 — USB_5 26
USB5_N P4 USB_5 — USB_5_ 26
USB6_P T3 USB_6 — USB_6 26
USB6_N T4 USB_6 — USB_6_ 26
USB7_P U3 USB_7 — USB_7 26
USB7_N U4 USB_7 — USB_7_ 26
USB8_P T6 USB_8
USB8_N T5 USB_8
USB9_P T8 USB_9
USB9_N T7 USB_9
USB10_P V5
USB10_N V4
USB11_P V7
USB11_N V6

USB_OC0*/GPIO25 P7 — USB_OC0 26
USB_OC1*/GPIO26 P8 — USB_OC1 26
USB_OC2*/GPIO27 P9 — USB_OC2 26
USB_OC3*/GPIO28/MGPIO1 P5 — USB_OC3 26
USB_OC4*/GPIO29 P6 — RST_GATE_GPIO2 20
USB_RBIAS_GND T9 — USB_GND BR10 1.1K 1% 0402 APP NOTE

CHIPSET	T9(USB_RBIAS_GND)
MCP61/65	1.1K
MCP68	732

A20GATE/GPIO55 F5 — A20GATE 19
INTRUDER* K2 — INTRUDER_
EXT_SMI*/GPIO32 F3 — SLEEPBTNJ — SLEEPBTNJ 22
RI*/GPIO33 H4 — SER_RI — SER_RI 27
SPKR C7 — SPEAKER — SPEAKER 22
PWRBTN* G4 — PWBTOUT — PWBTOUT_ 19
SIO_PME*/GPIO31 F4 — IO_PME — IO_PME_ 19
KBRDRSTIN*/GPIO56 A4 — SIO_KBRST — SIO_KBRST_ 19

SMB_CLK0 C2 — SMB_MEM_SCL 10,11
SMB_DATA0 C1 — SMB_MEM_SDA 10,11
SMB_CLK1/MSMB_CLK D2 — SMB_SCLL — SMB_SCL 20,21,31
SMB_DATA1/MSMB_DATA E2 — SMB_SDAL — SMB_SDA 20,21,31
+3.3V_VBAT K3 — +3.3V_VBAT
BUF_SIO_CLK B5 — BUF_SIO_CLK_R — BR29 22 0402 — BUF_SIO_CLK 19
SUS_CLK/GPIO34 E1 — SUS_CLK_R — R87 22 0402 — SUSCLK 19
THERM*/GPIO59 C6 — CHIP_THERM_ — CHIP_THERM_ 19
RSTBTN* H5 — FP_RESET — FP_RESET_ 22
SLP_S5 H8 — SLP_S5 — SLP_S5_ 19,32
SLP_S3 G8 — SLP_S3 — SLP_S3_ 19,32
PWRGD_SB H6 — PWRGD_SB — PWRGD_SB 34
PS_PWRGD G2 — MCP61_PWRGD — MCP61_PWRGD 34
FANRPM0/GPIO60 E6
FANCTL0/GPIO61 D6
FANCTL1/GPIO62 C5
THERM_SIC/GPIO48 AH7 — THERM_SIC 7
THERM_SID/GPIO49 AF8 — THERM_SID 7
THERM_SID1/GPIO47/PWR_LED* AE7

C139 10P 50V NPO 0402 /NI
BC80 22P 50V NPO 0402

USB_0 1 — USB_0 3 — USB_1 5 — USB_1 7 — RN21 15K 8P4R 0402
USB_3 1 — USB_3 3 — USB_2 5 — USB_2 7 — RN22 15K 8P4R 0402
USB_5 1 — USB_5 3 — USB_4 5 — USB_4 7 — RN23 15K 8P4R 0402
USB_6 1 — USB_6 3 — USB_7 5 — USB_7 7 — RN24 15K 8P4R 0402
USB_8 1 — USB_8 3 — USB_9 5 — USB_9 7 — RN25 15K 8P4R 0402

Q2
CM1293 SOT23-6 /NI
SMB_MEM_SDA 1
SMB_MEM_SCL 3
+3.3V_DUAL 5
NEAR TO DDR

+3.3V_DUAL
R83 1M 0402 — +3.3V_VBAT
RN2 2.7K 8P4R 0402 — +3.3V
+3.3V_VBAT
C141 1UF 10V Y5V 0402

SPEAKER
0 = USER MODE
1 = SAFE MODE
*0= DEFAULT

+3.3V
R84 1K 1% 0402 /NI
SPEAKER
R85 1K 1% 0402

+3.3V
R69 4.7K 0402 /NI
CHIP_THERM

BOARD ID define:
Bit2 Bit1 Bit0
X X X
1 1 ------> 6.0;
0 1 ------> next bios version;
1 0 ------> next bios version;
0 0 ------> next bios version.
1 ------> Without EUP function.
0 ------> With EUP function.

+3.3V
R39 10K 0402
BOARD_ID0
R40 1K 0402 /NI
+3.3V
R41 10K 0402
BOARD_ID1
R42 1K 0402 /NI

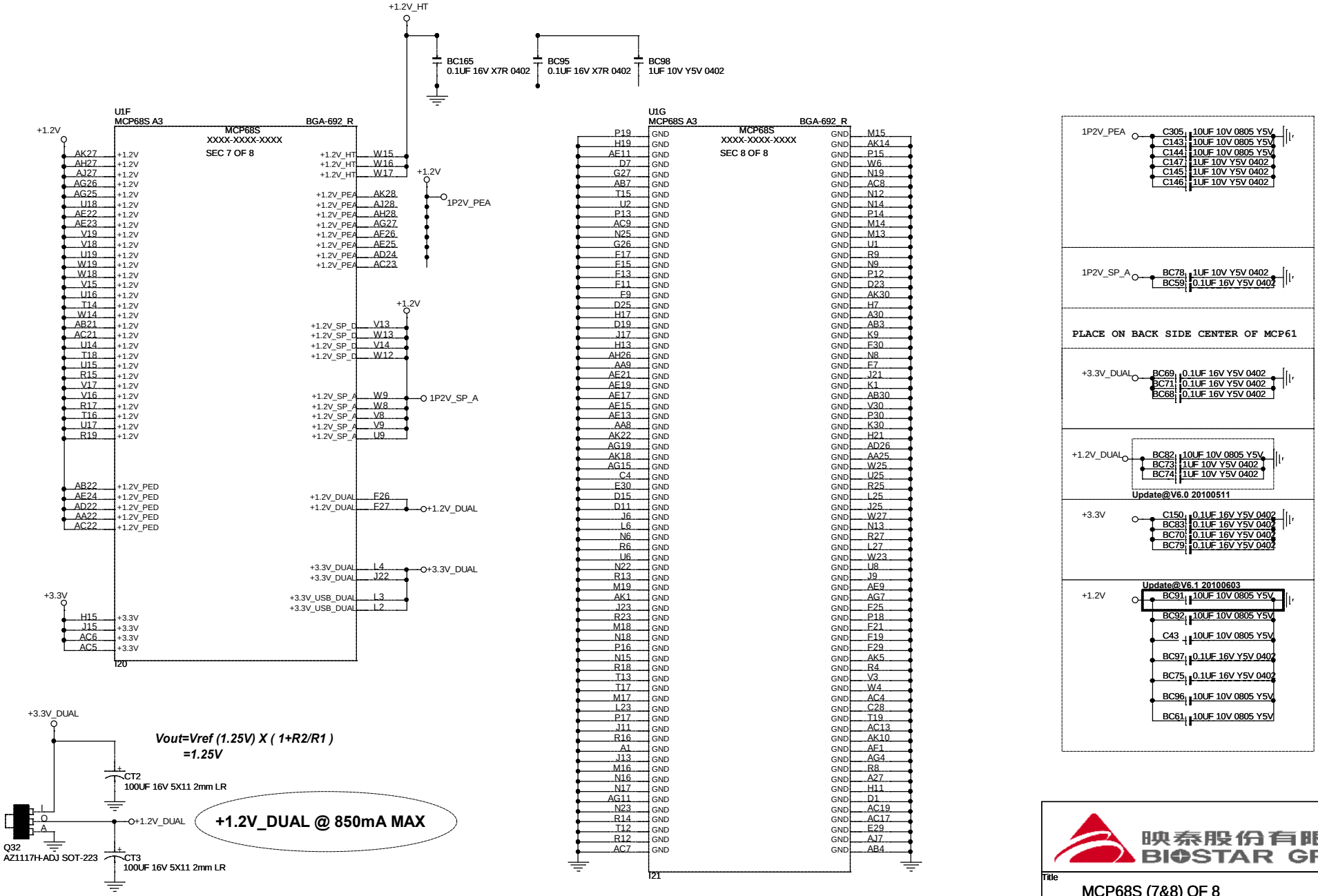
Update@V6.0 20100511

MCP61 SPI CLK STRAP		
SPI_DO	SPI_CLK	
0	0	500 KHz
0	1	1.8 MHz
1	0	2.5 MHz
1	1	25 MHz

MCP68 SPI CLK STRAP		
SPI_DO	SPI_CLK	
0	0	31Mhz
0	1	42Mhz Default
1	0	25Mhz
1	1	1Mhz

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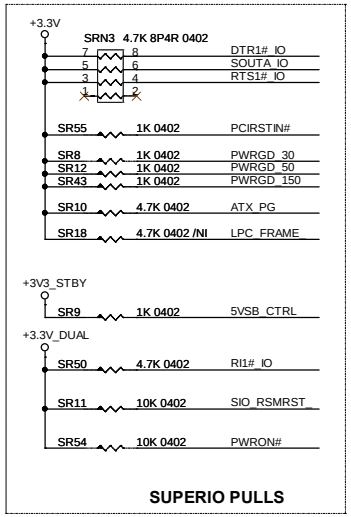
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Size: Custom
Document Number: N68SC-M3S
Rev: 6.1
Date: Tuesday, November 09, 2010
Sheet 17 of 36

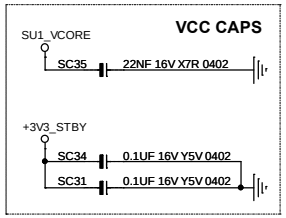


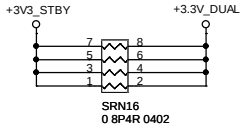
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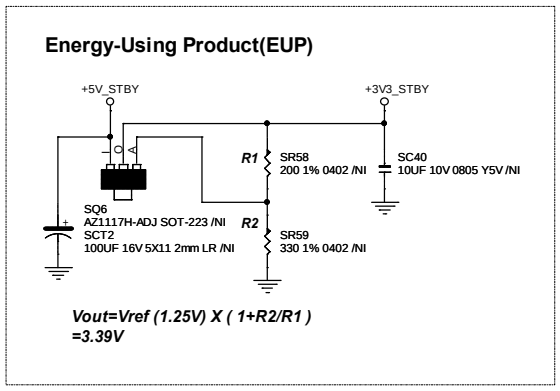
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Size B	Document Number N68SC-M3S	Rev 6.1
Date: Monday, November 08, 2010	Sheet 18 of 36	

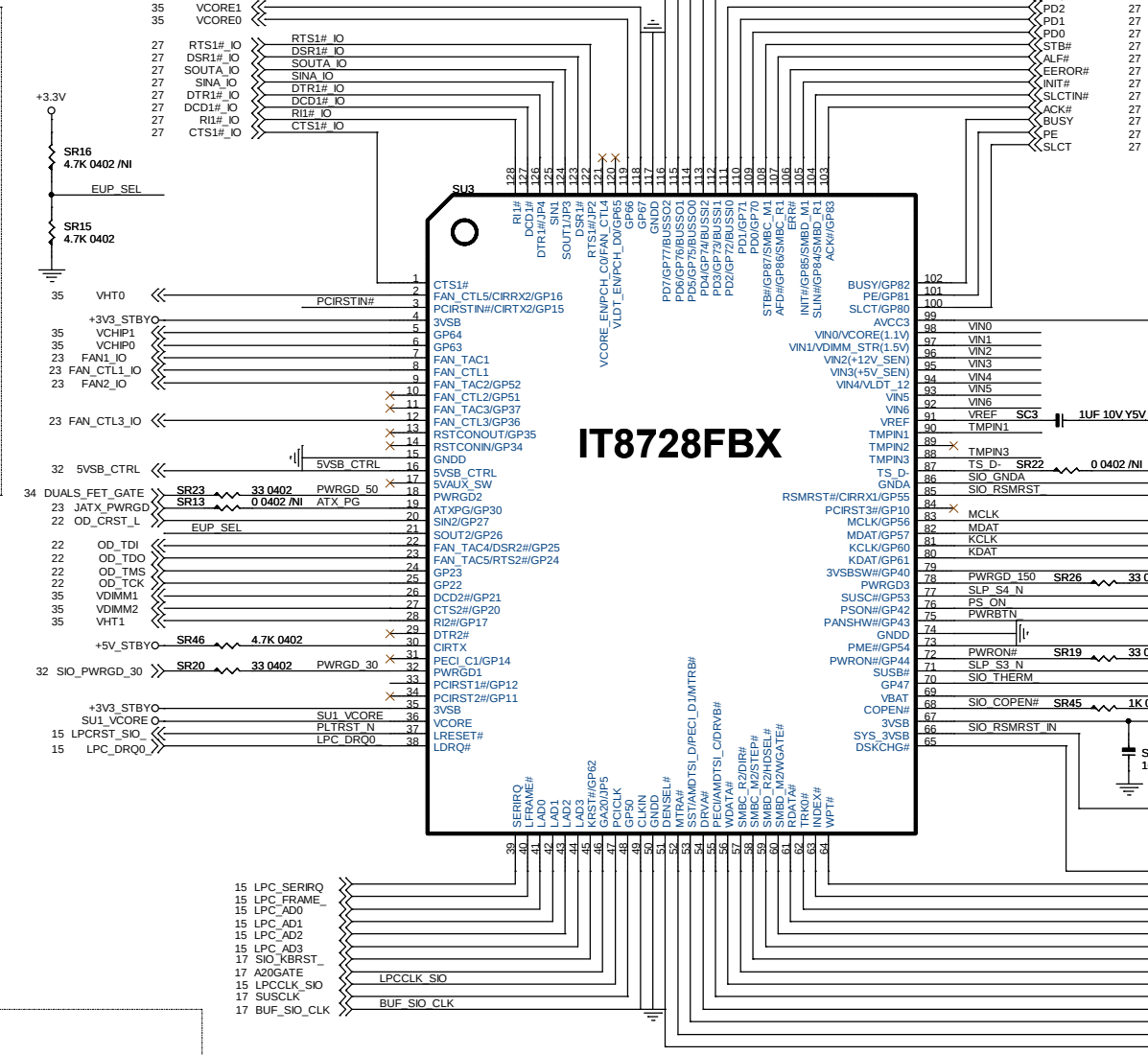
SUPERIO PART: S+Reference

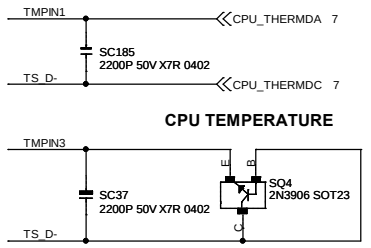




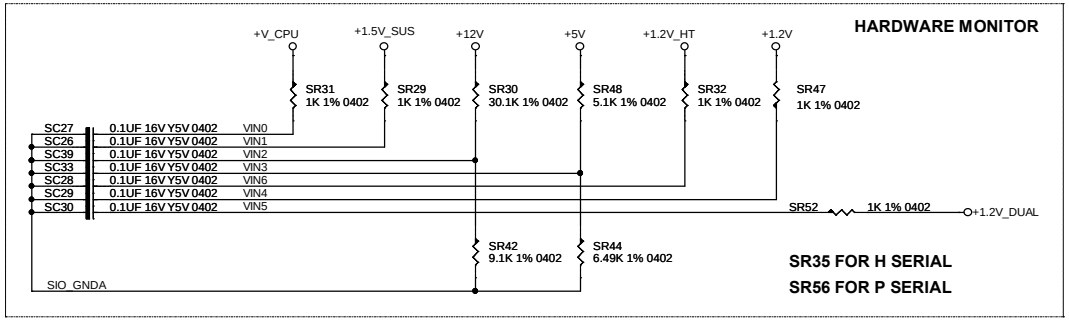










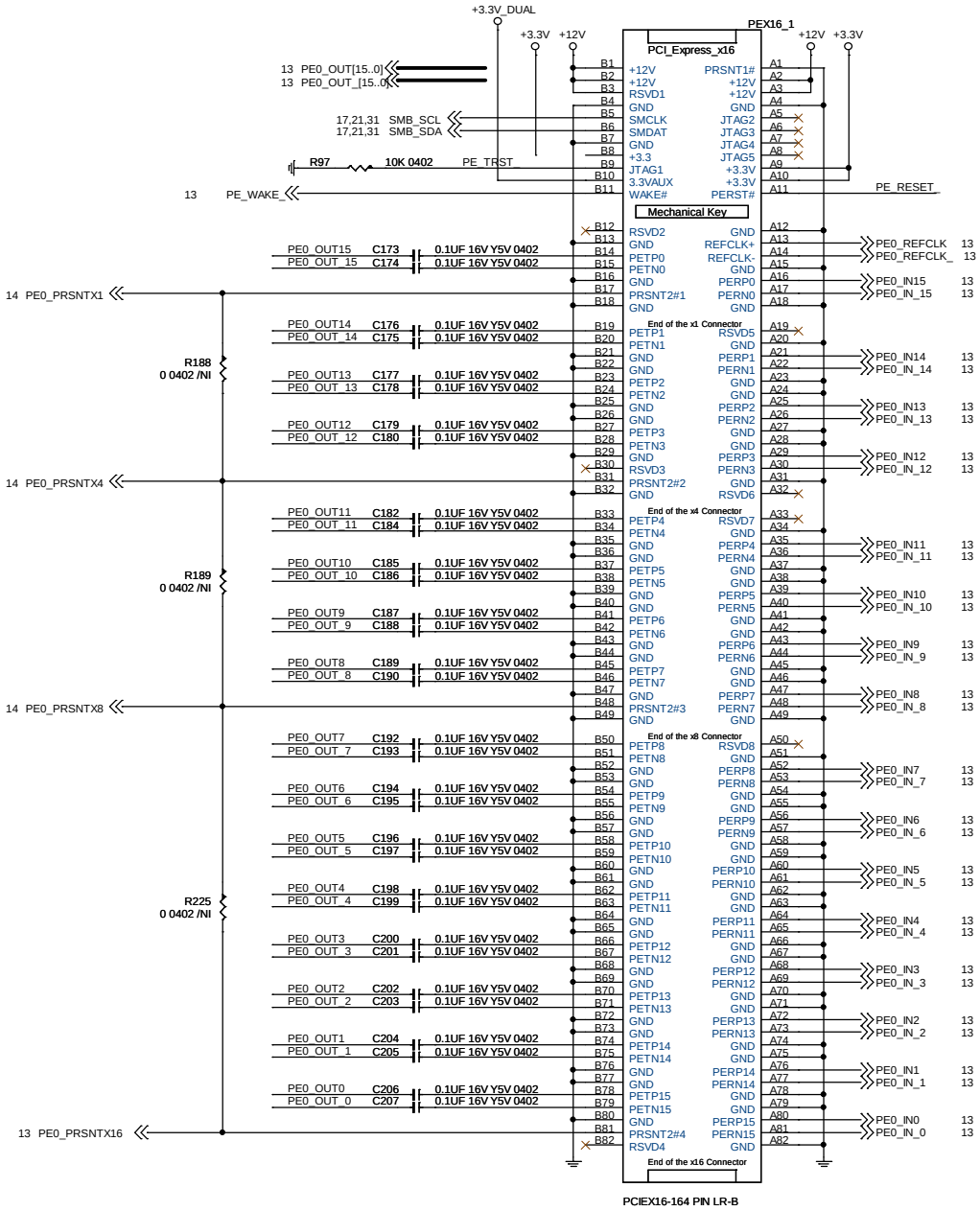


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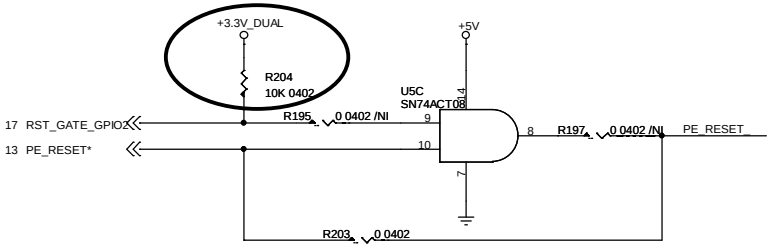
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Size: Custom | Document Number: N68SC-M3S | Rev: 6.1

Date: Tuesday, November 09, 2010 | Sheet 19 of 36

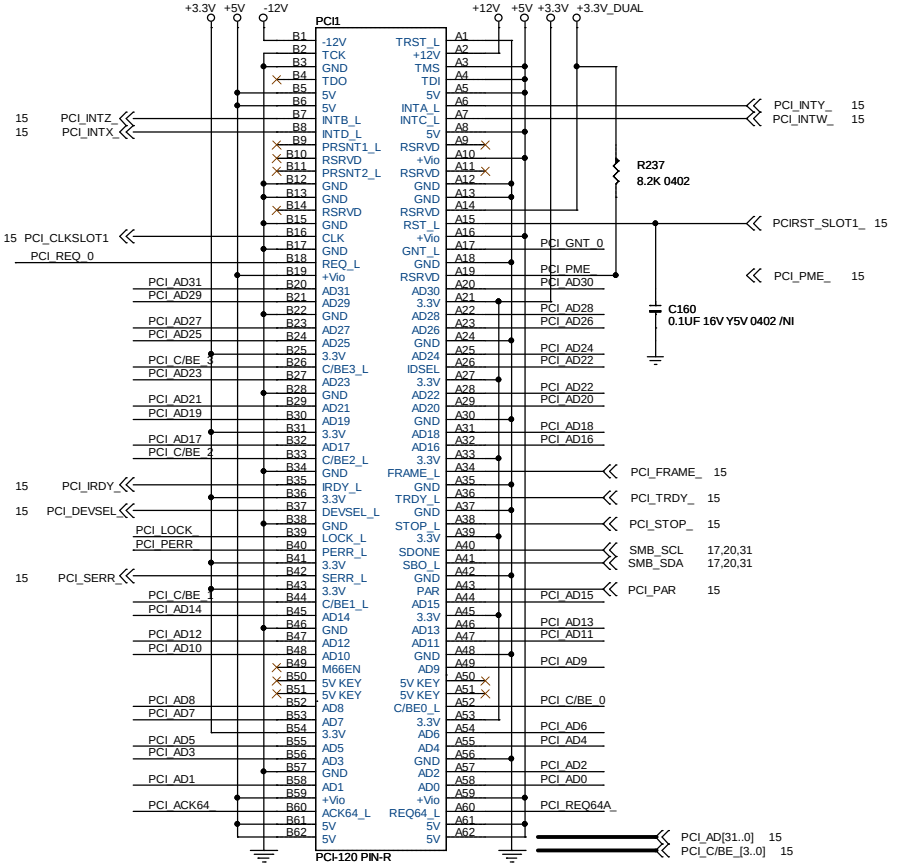


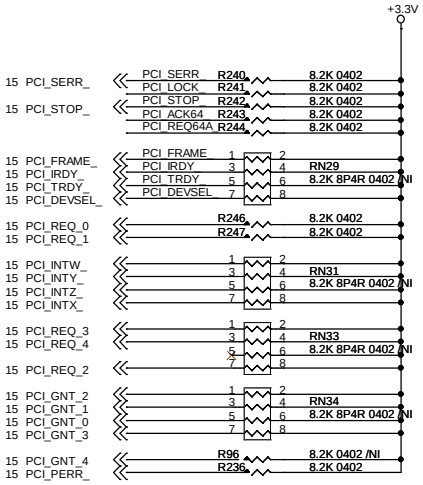
PCIEX16-164 PIN LR-B

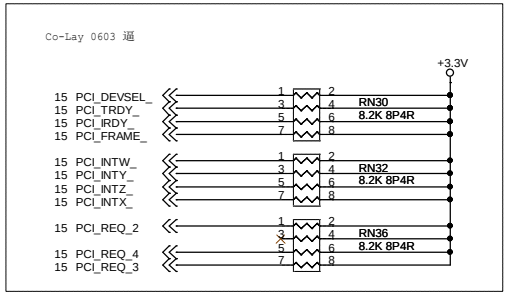


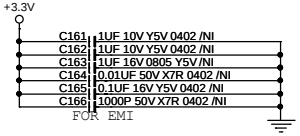
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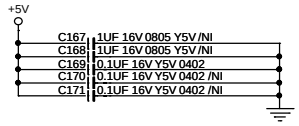
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Size: Custom	Document Number: N68SC-M3S	Rev: 6.1
Date: Tuesday, November 09, 2010	Sheet 20 of 36	

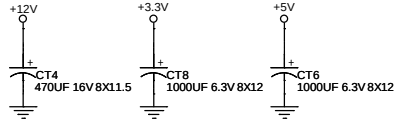








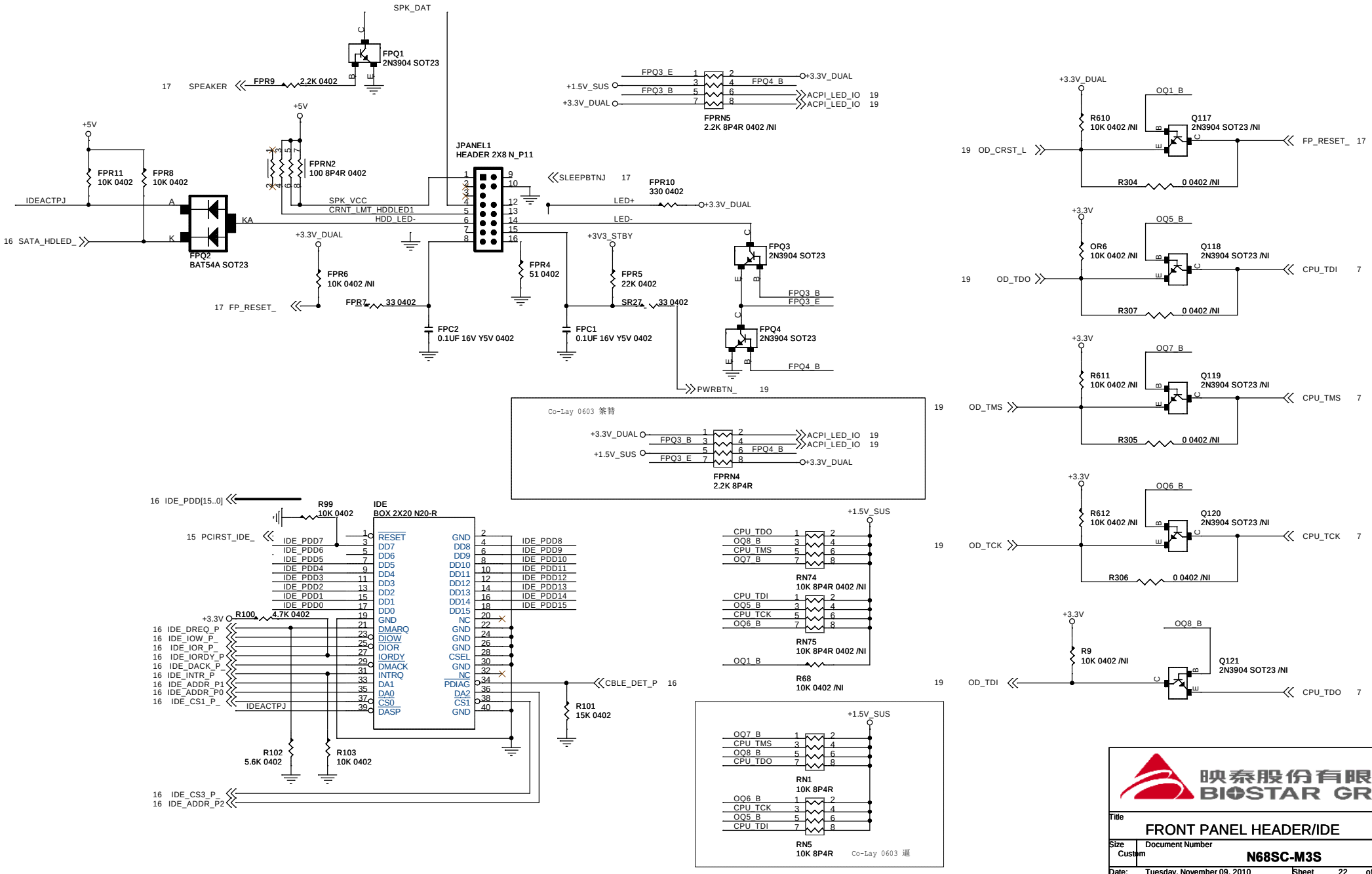




	PCI SLOT 1	PCI SLOT 2
PCICLK	PCI_CLKSLOT1	PCI_CLKSLOT2
INTR	PCI_INTY*	PCI_INTW*
IDSEL	PCI_AD22	PCI_AD24

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Title	PCI SLOT 1&2	
Size: Custom	Document Number: N68SC-M3S	Rev: 6.1
Date: Tuesday, November 09, 2010	Sheet 21 of 36	

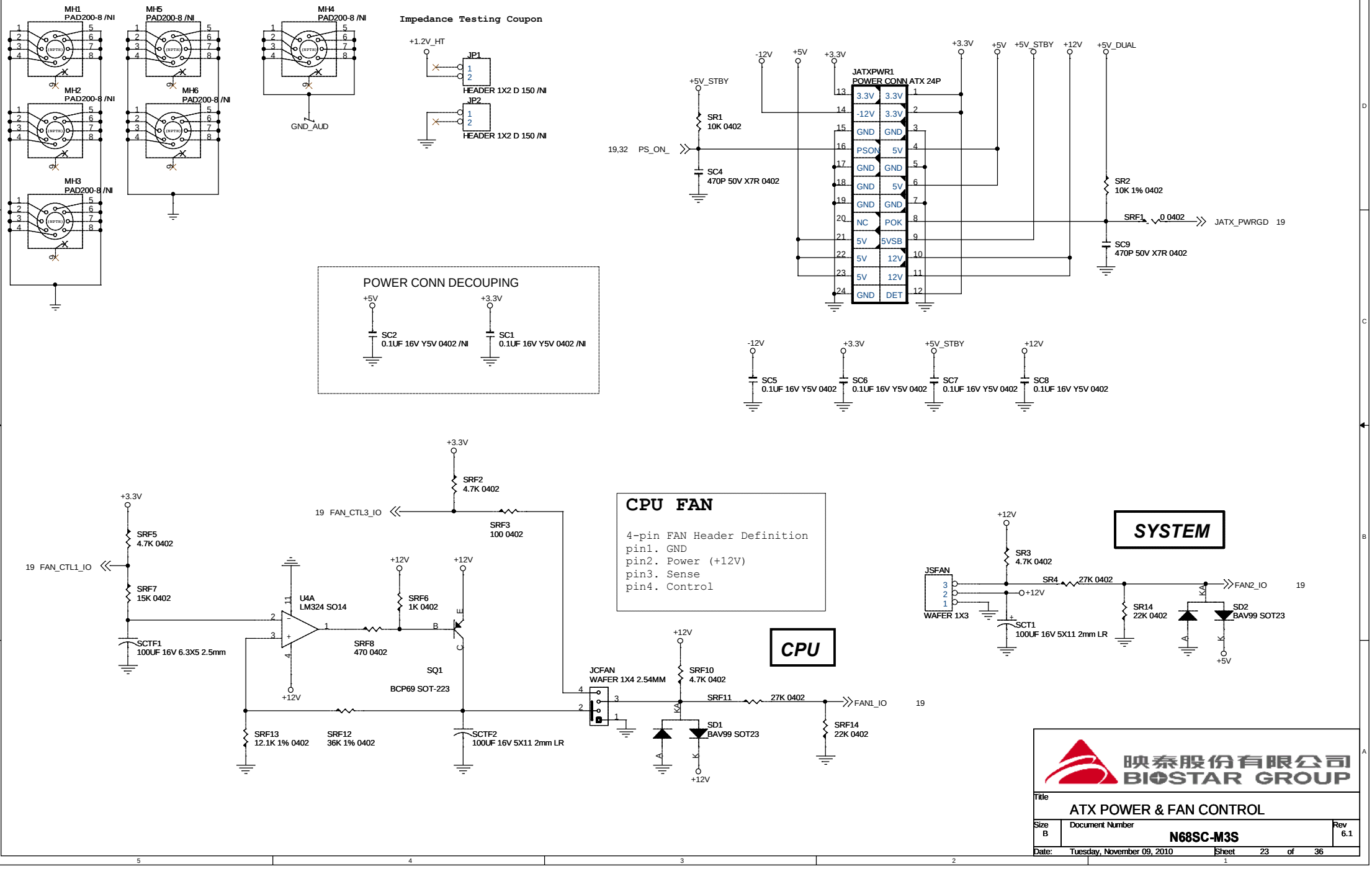


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Title
FRONT PANEL HEADER/IDE

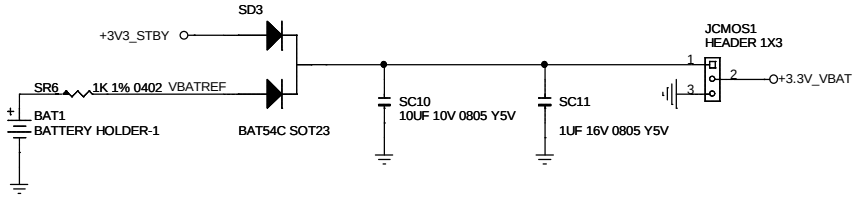
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Custom	N68SC-M3S	6.1

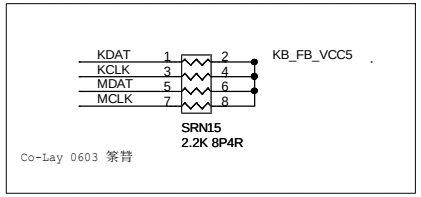
Date: Tuesday, November 09, 2010 Sheet 22 of 36

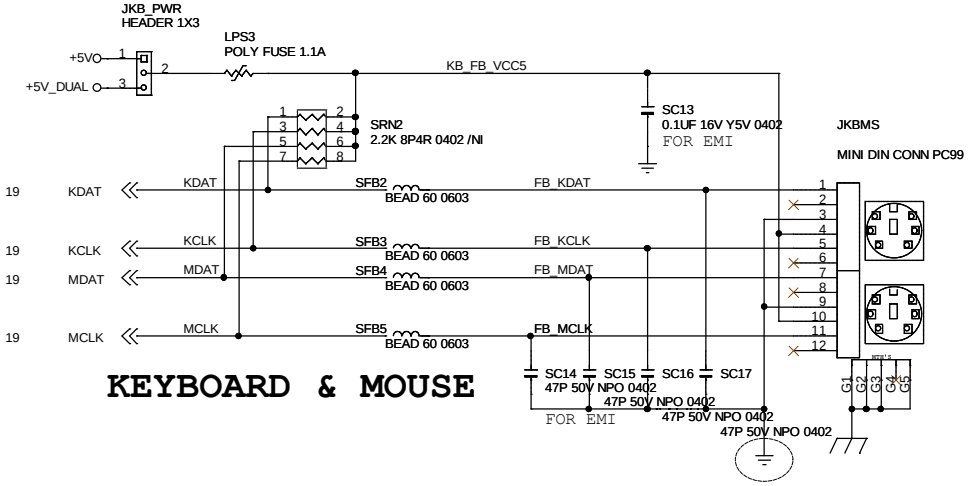


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Title	ATX POWER & FAN CONTROL	
Size B	Document Number N68SC-M3S	Rev 6.1
Date: Tuesday, November 09, 2010	Sheet 23 of 36	

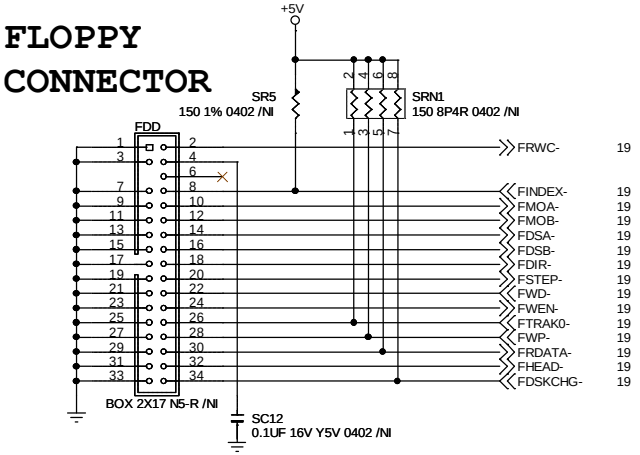






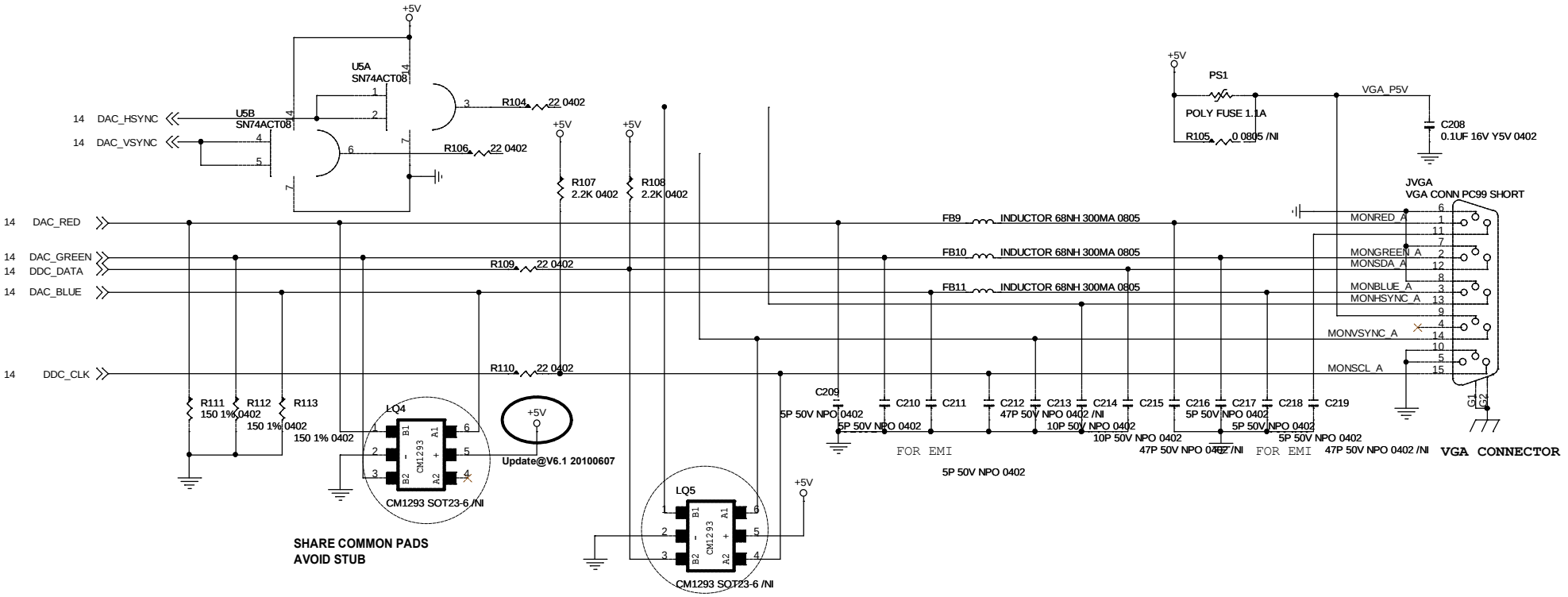
KEYBOARD & MOUSE

FLOPPY CONNECTOR



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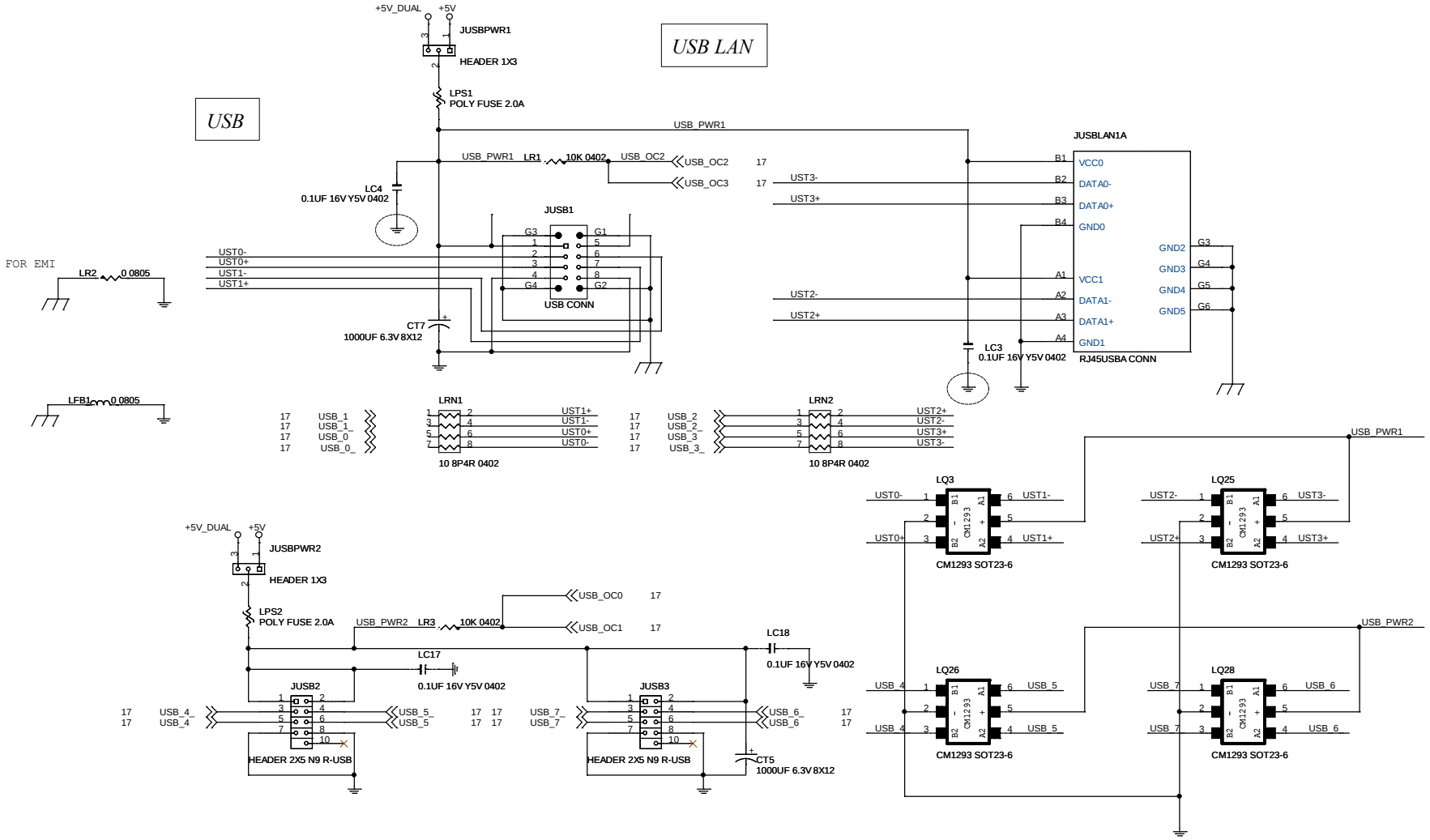
Title	FLOOY ,PS/2 ,CMOS,HW MON	
Size B	Document Number N68SC-M3S	Rev 6.1
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DAC Signal Name	Type	Termination/ Strapping	Description
DDC_CLK/ GPIO17	I/O	33 Ω series resistor and 2.2 kΩ pull-up to +5V (both close to VGA connector). Also, place-holders for a 470 pF cap to GND and ESD protection diodes to +5V and GND.	DDC Clock Clock for DDC interface to VGA. Connect to pin-15 of VGA (DB15) connector. Route S/S. No length restrictions.
	I/O		GPIO17 Can be used as GPIO if DDC_CLK function is not used.
DDC_DATA/ GPIO19	I/O	33 Ω series resistor and 2.2 kΩ pull-up to +5V (both close to VGA connector). Also, a place-holder for a 470 pF cap to GND and ESD protection diodes to +5V and GND.	DDC Data Data for DDC interface to VGA. Connect to pin-12 of VGA (DB15) connector. Route S/S. No length restrictions.
	I/O		GPIO19 Can be used as GPIO if DDC_DATA function is not used.

FB12 0 0805

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Title: VGA CONNECTOR		
Size: B	Document Number: N68SC-M3S	Rev: 6.1
Date: Tuesday, November 09, 2010	Sheet 25 of 36	

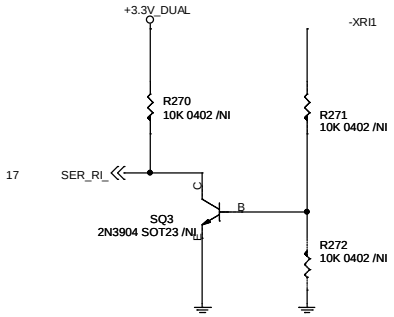


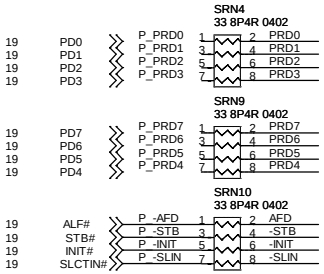
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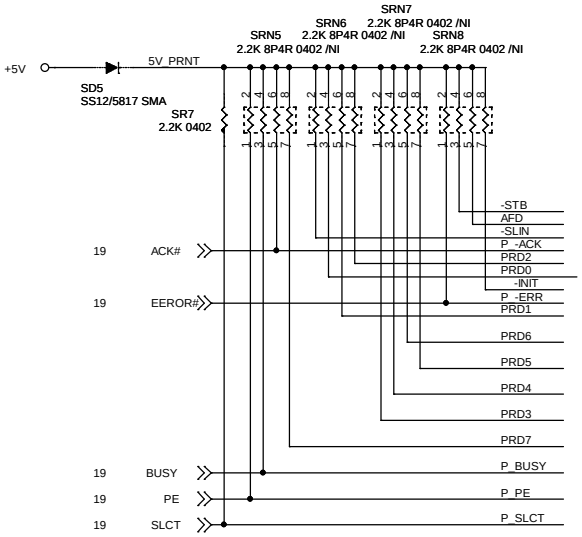
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Size: Custom	Document Number: N68SC-M3S	Rev: 6.1
Date: Tuesday, November 09, 2010	Sheet 26 of 36	

LPT

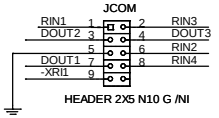
PARALLEL - CONNECTOR



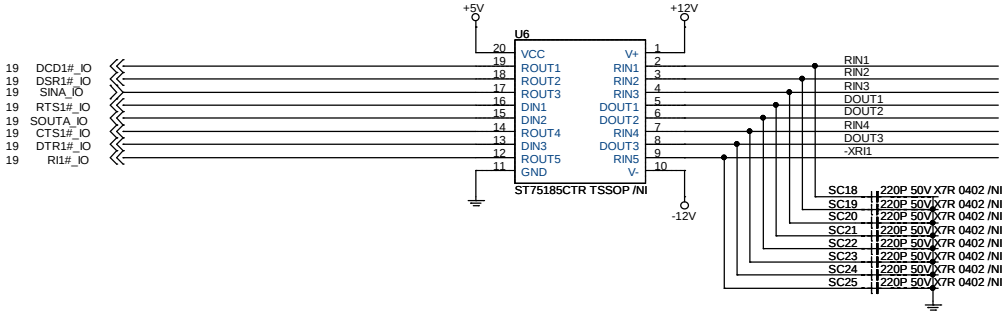


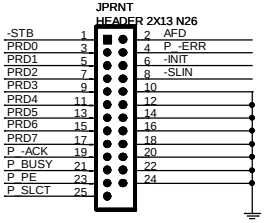


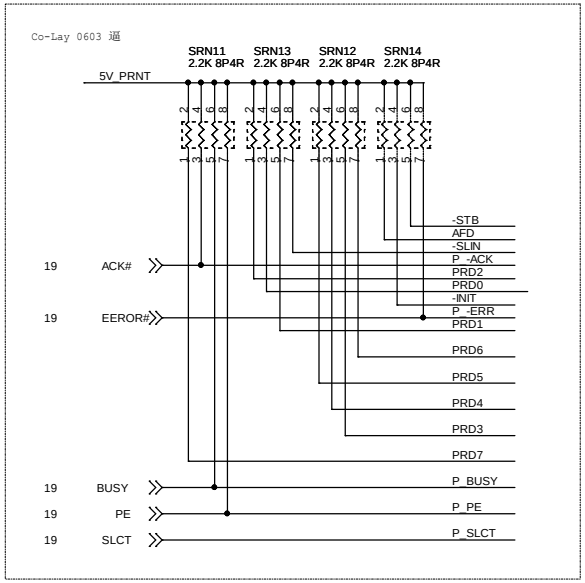
WAKE ON MODEN



COM1



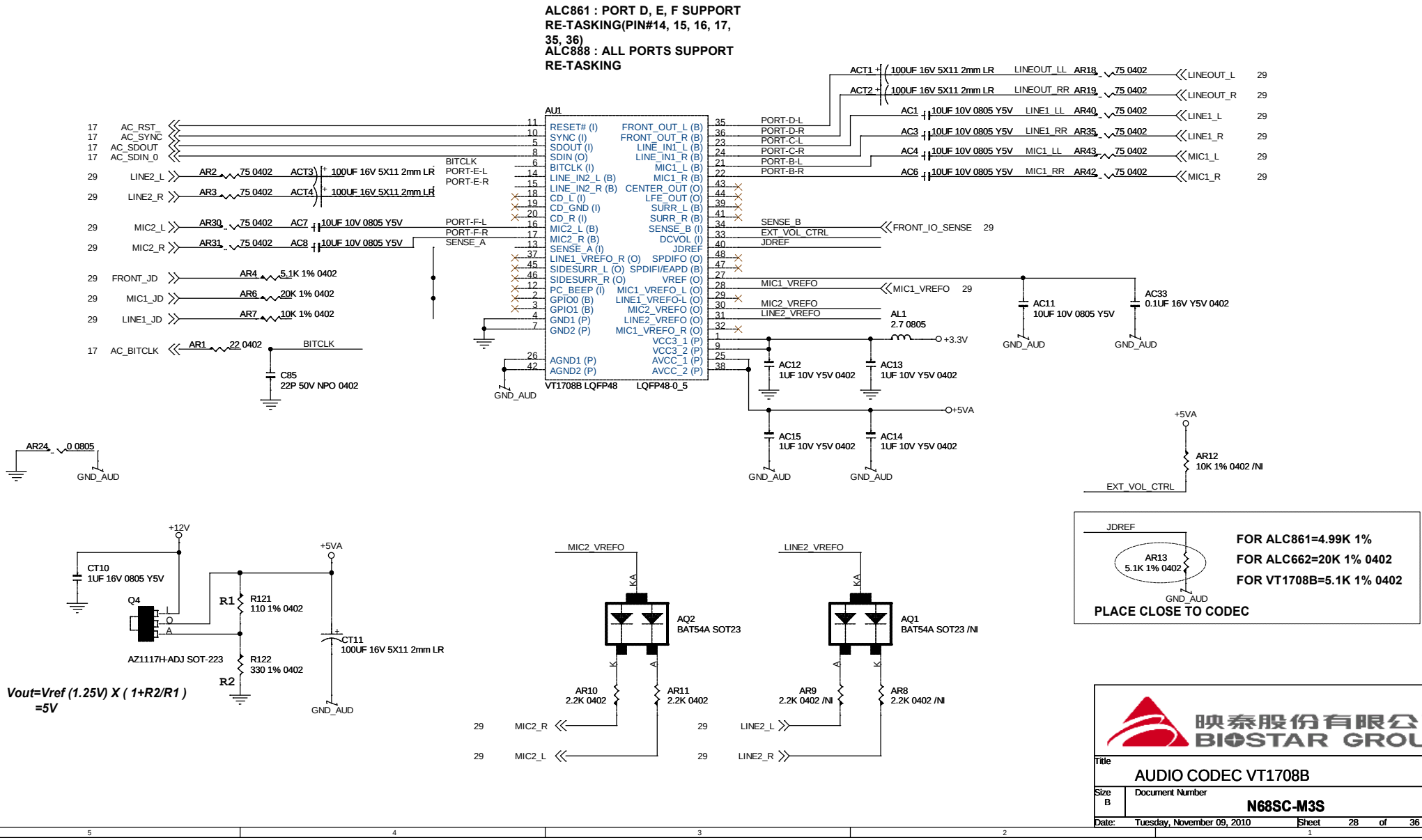




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Title	LPT & COM1	
Size: Custom	Document Number: N68SC-M3S	Rev: 6.1
Date: Tuesday, November 09, 2010	Sheet 27 of 36	

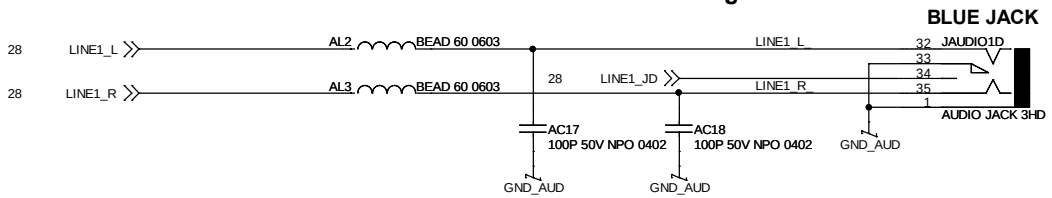
CODEC ALC655/ALC658/ALC861VD/ALC883/VT1708A/ Colay Circuit

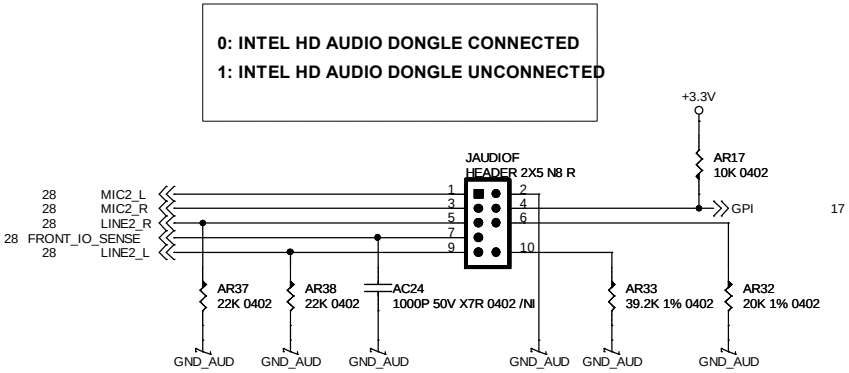


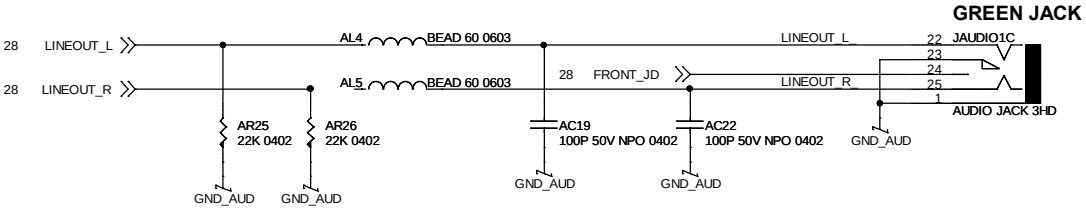
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Size B	Document Number N68SC-M3S	Rev 6.1
Date: Tuesday, November 09, 2010	Sheet 28 of 36	

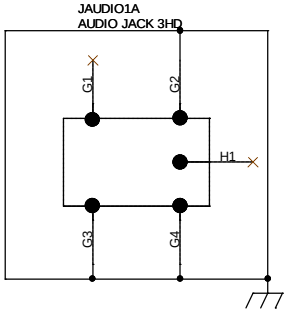
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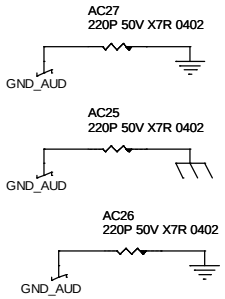
Rear Panel Onboard Analog I/O

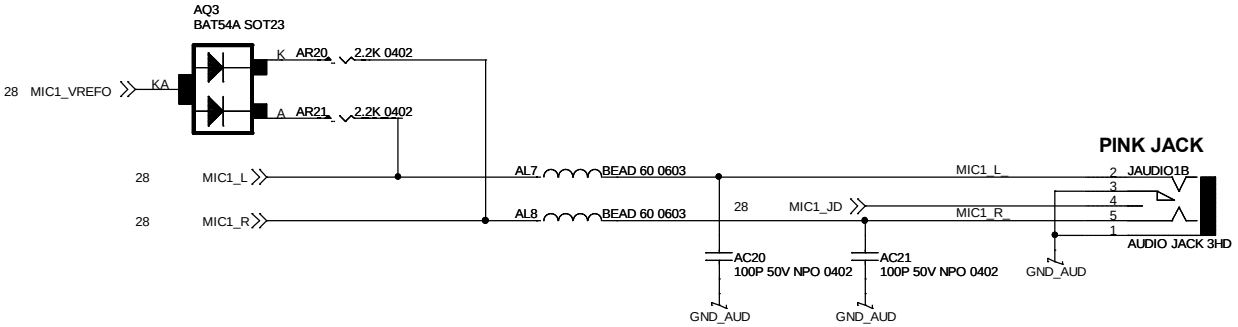






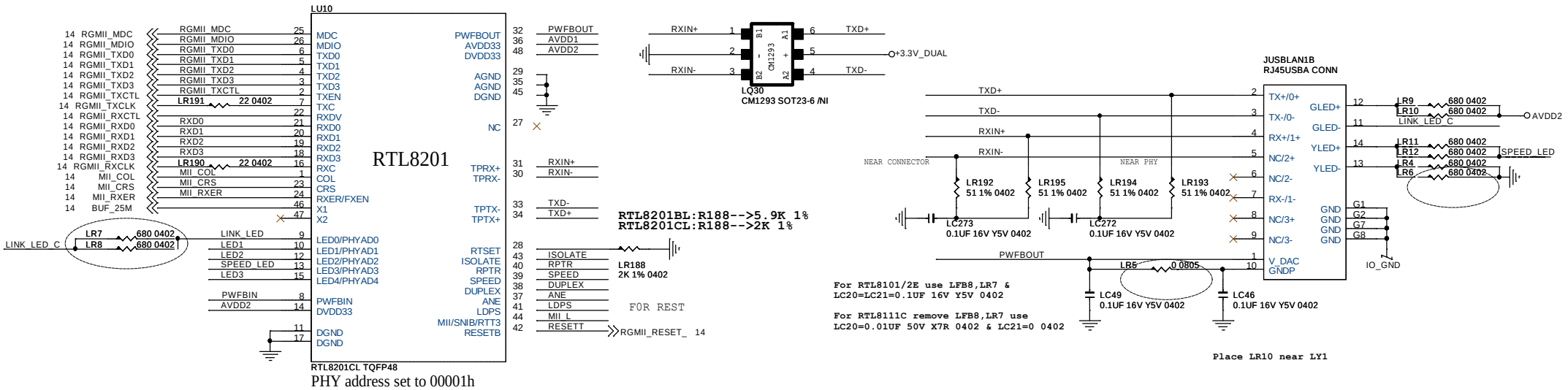


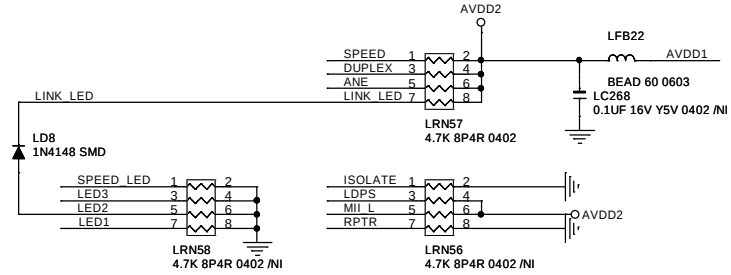


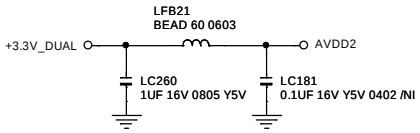


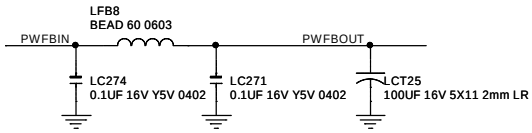
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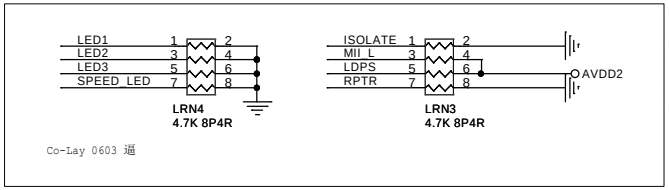


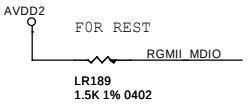


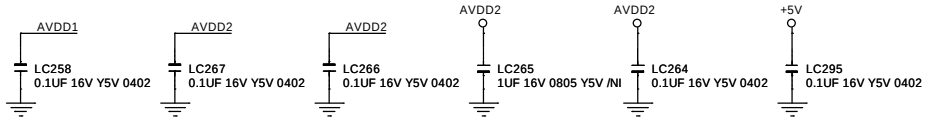
R279 is reserved for 8201CL/CP LED Mode Change to compatible with BL

R280 is reserved for ensuring 8201BL/CL/CP latch to UTP Mode.

R281 is reserved for ensuring 8201CL/CP latch to normal operation mode.

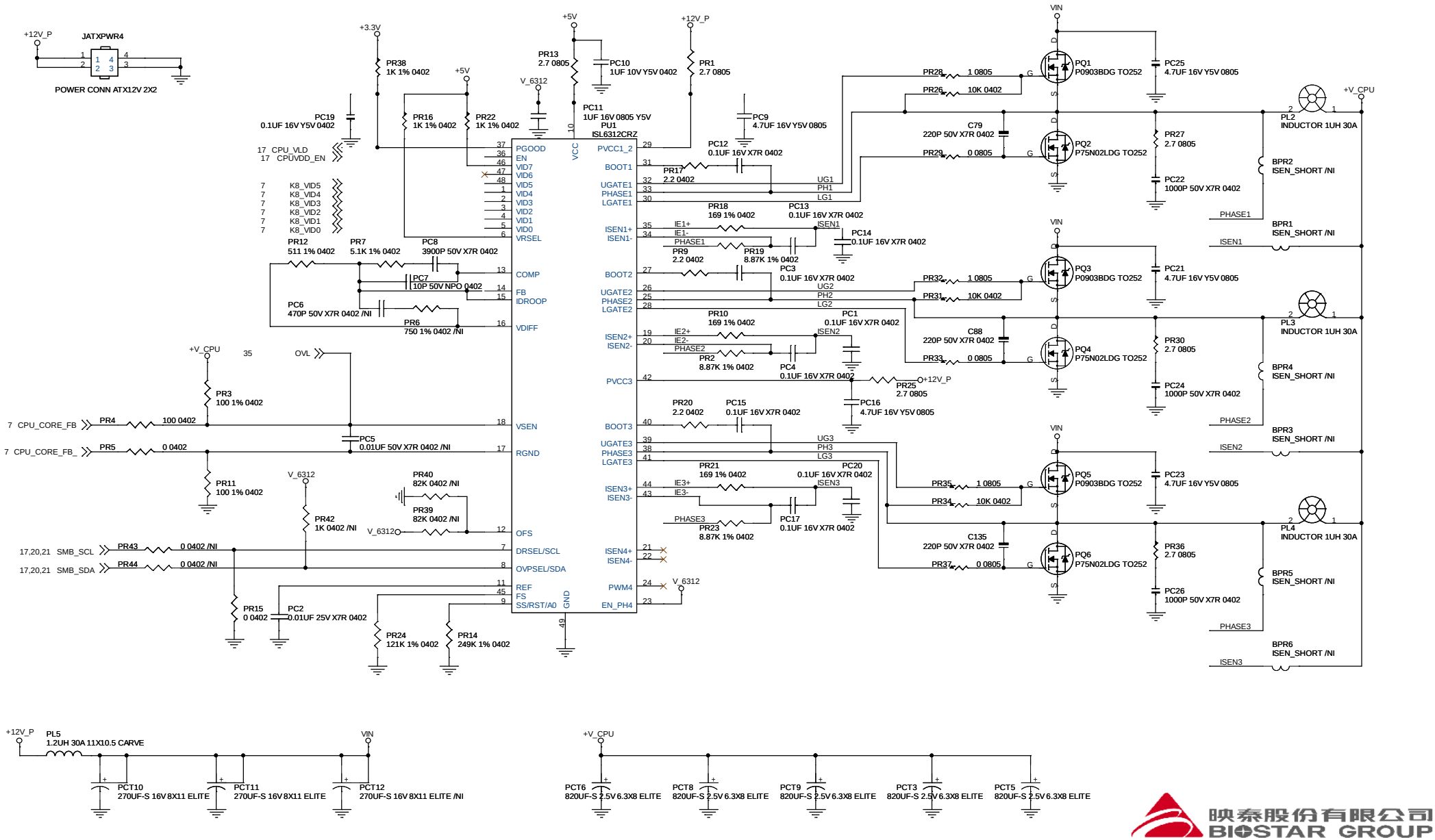




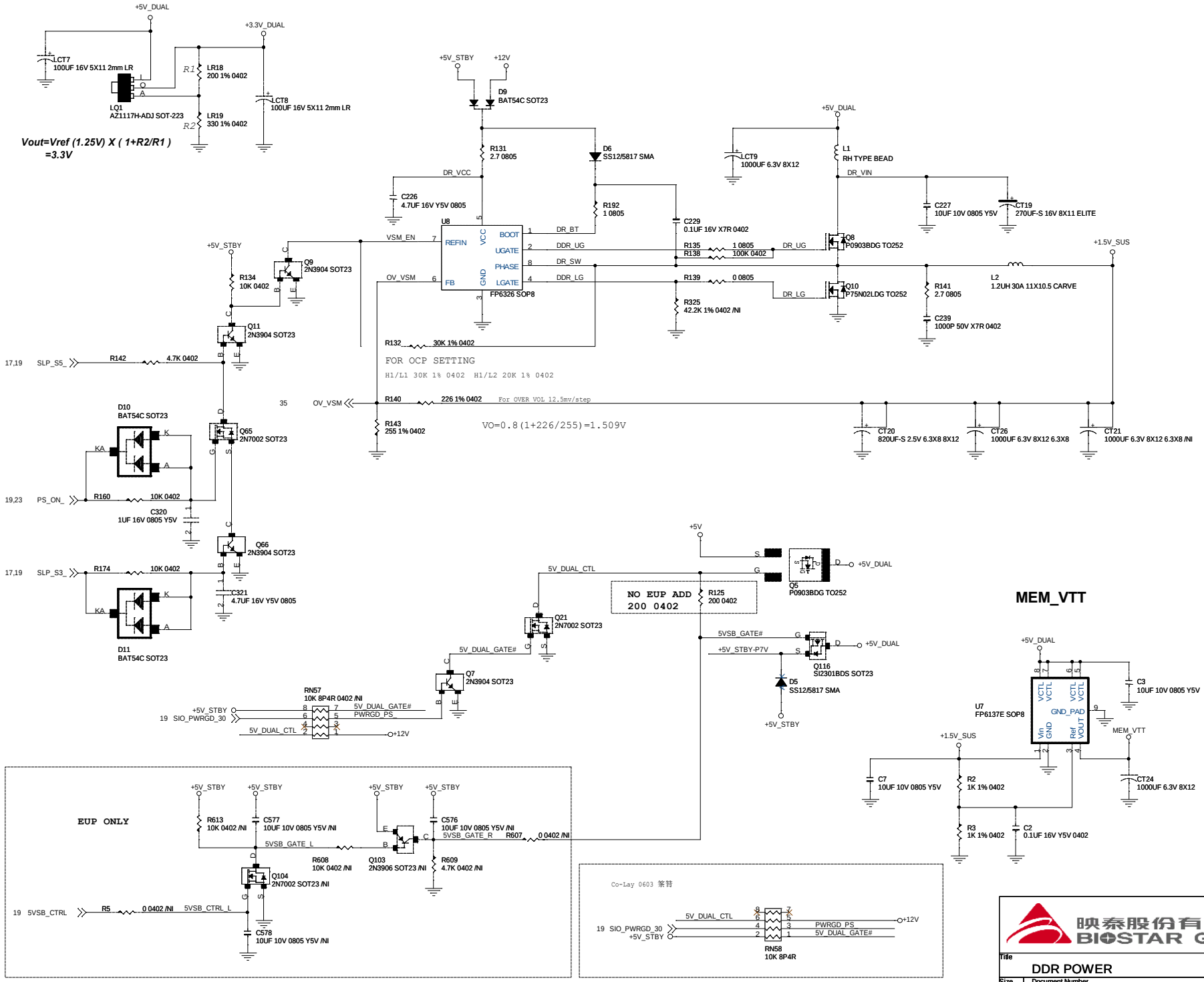


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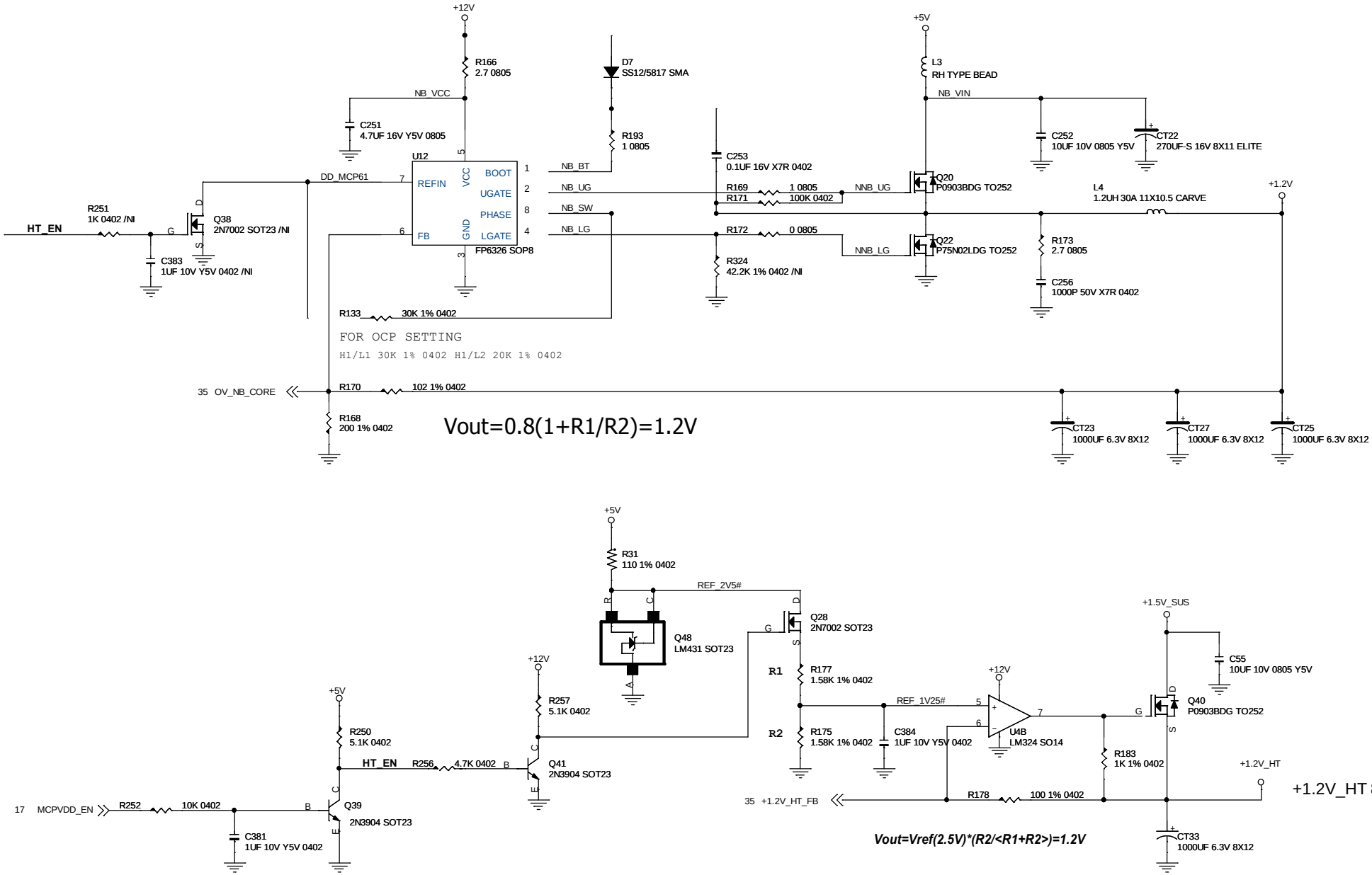
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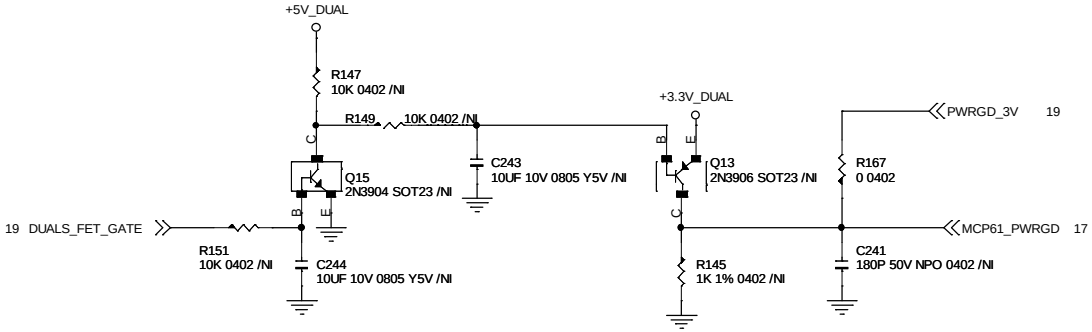
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Size: Custom	Document Number: N68SC-M3S		Rev: 6.1
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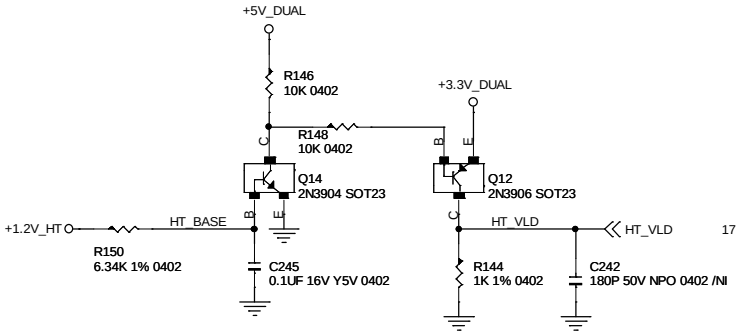


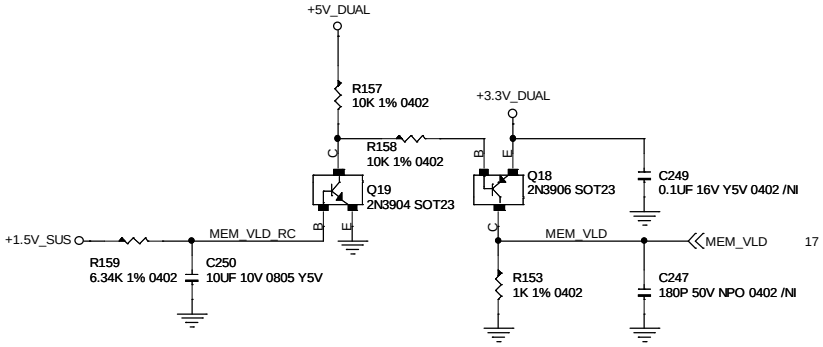
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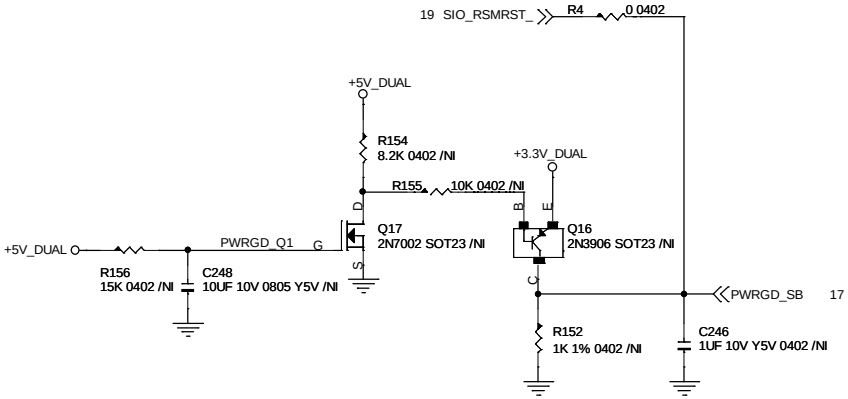
Title	MCP68S CORE	
Size: Custom	Document Number: N68SC-M3S	Rev: 6.1
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POWER SEQUENCING



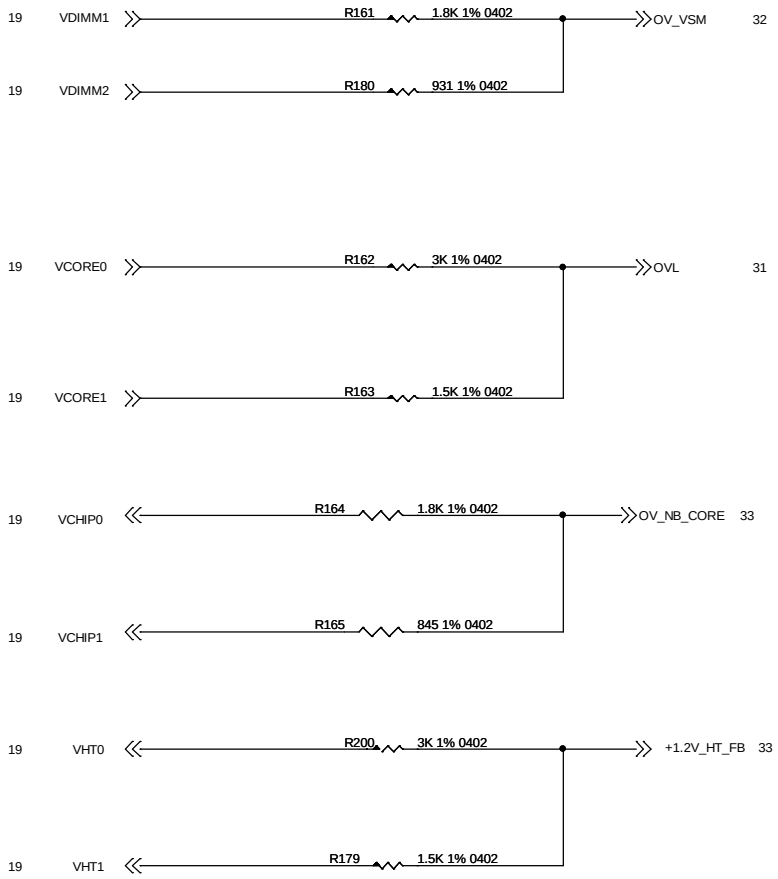






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VDIMM1	VDIMM2	VOLTAGE
HR	HR	+1.5V (Default)
0	HR	+1.6V
HR	0	+1.7V
0	0	+1.8V

VCORE_OVL	VCORE0	VCORE1
Default Vcore	HR	HR
Vcore(1%)	0	HR
Vcore(2%)	HR	0
Vcore(3%)	0	0

+1.2V	VCHIP0	VCHIP1
1.2V	HR	HR
1.25V	0	HR
1.3V	HR	0
1.35V	0	0

+1.2V_HT	VHT0	VHT1
1.25V	HR	HR
1.30V	0	HR
1.35V	HR	0
1.40V	0	0

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JUSBPWR2(1_2)
JUMPER 2P R

JUSBPWR1(1_2)
JUMPER 2P R

JKB_PWR(1_2)
JUMPER 2P R

(X2)
X'TAL WIRE

JCMOS1(1_2)
JUMPER 2P B

(BAT1)

3V BATTERY SONY

(U2)

SPI MX25L8005 DIP

(CPU1)

AM2RM-B

(U1)

NBHS-A74GC

(PCB)

POLON 235X182

New JPANEL1
JPANEL1 2*11

PCB

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